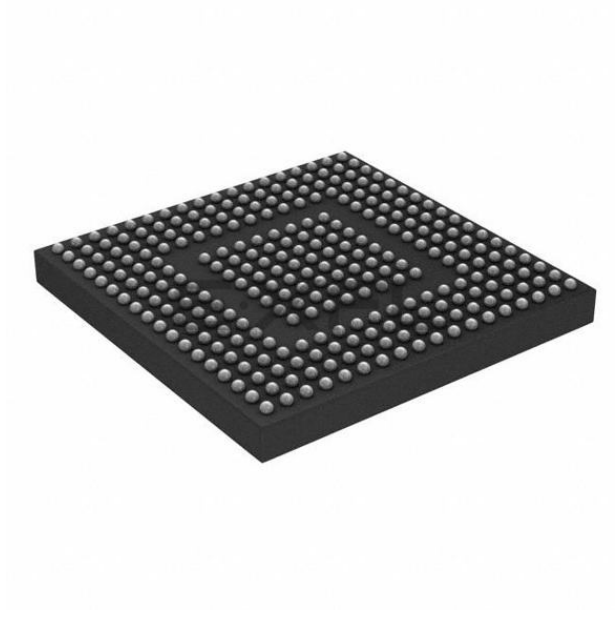
Microchip Technology - PIC32MZ2064DAB288-I/4J Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 45x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	288-LFBGA
Supplier Device Package	288-LFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2064dab288-i-4j

TABLE 1-4: OC1 THROUGH OC9 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
Output Compare						
OC1	PPS	PPS	PPS	O	—	Output Compare Outputs 1-9
OC2	PPS	PPS	PPS	O	—	
OC3	PPS	PPS	PPS	O	—	
OC4	PPS	PPS	PPS	O	—	
OC5	PPS	PPS	PPS	O	—	
OC6	PPS	PPS	PPS	O	—	
OC7	PPS	PPS	PPS	O	—	
OC8	PPS	PPS	PPS	O	—	
OC9	PPS	PPS	PPS	O	—	
OCFA	PPS	PPS	PPS	I	ST	Output Compare Fault A Input
OCFB	PPS	PPS	PPS	I	ST	Output Compare Fault B Input

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-5: EXTERNAL INTERRUPTS PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
External Interrupts						
INT0	C3	42	A6	I	ST	External Interrupt 0
INT1	PPS	PPS	PPS	I	ST	External Interrupt 1
INT2	PPS	PPS	PPS	I	ST	External Interrupt 2
INT3	PPS	PPS	PPS	I	ST	External Interrupt 3
INT4	PPS	PPS	PPS	I	ST	External Interrupt 4

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-21: GRAPHICS LCD (GLCD) CONTROLLER PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
GLCD Controller						
GCLK	G11	148	L17	O	—	Graphics Display Pixel Clock
HSYNC	F12	149	L18	O	—	Graphics Display Horizontal Sync Pulse
VSYNC	F13	150	K18	O	—	Graphics Display Vertical Sync Pulse
GEN	G13	147	L16	O	—	Graphics Display Enable Output
GD0	G12	144	M16	O	—	Graphics Controller Data Output
GD1	L11	127	V17	O	—	
GD2	H1	76	U6	O	—	
GD3	N2	96	V9	O	—	
GD4	M2	95	T8	O	—	
GD5	K3	90	U7	O	—	
GD6	L1	91	V7	O	—	
GD7	J1	80	U5	O	—	
GD8	G10	143	N18	O	—	
GD9	F9	145	M17	O	—	
GD10	G2	74	R6	O	—	
GD11	G3	75	T6	O	—	
GD12	L13	134	R16	O	—	
GD13	H10	133	P15	O	—	
GD14	J10	132	R15	O	—	
GD15	M13	131	T18	O	—	
GD16	K2	89	T7	O	—	
GD17	L3	97	U9	O	—	
GD18	F8	146	M18	O	—	
GD19	M12	130	T17	O	—	
GD20	E8	151	K17	O	—	
GD21	L2	92	V8	O	—	
GD22	J2	81	N4	O	—	
GD23	K12	137	P16	O	—	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

2.3 Master Clear (MCLR) Pin

The MCLR pin provides for two specific device functions:

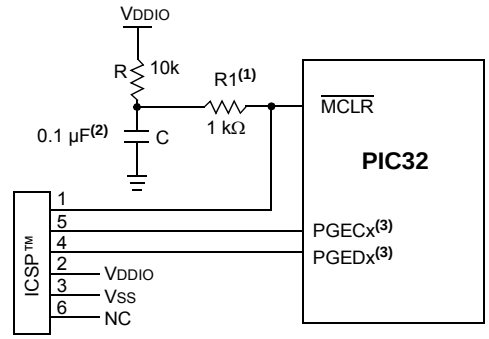
- Device Reset
- Device programming and debugging

Pulling The MCLR pin low generates a device Reset. Figure 2-2 illustrates a typical MCLR circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor C be isolated from the MCLR pin during programming and debugging operations.

Place the components illustrated in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



Note 1: 470Ω ≤ R1 ≤ 1Ω will limit any current flowing into MCLR from the external capacitor C, in the event of MCLR pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the MCLR pin VIH and VIL specifications are met without interfering with the Debug/Programmer tools.

2: The capacitor can be sized to prevent unintentional Resets from brief glitches or to extend the device Reset period during POR.

3: No pull-ups or bypass capacitors are allowed on active debug/program PGECx/PGEDx pins.

2.4 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (VIH) and input low (VIL) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 3 or MPLAB REAL ICE™.

For additional information on ICD 3 and REAL ICE connection requirements, refer to the following documents that are available for download from the Microchip web site, www.microchip.com:

- *"Using MPLAB® ICD 3"* (poster) (DS50001765)
- *"MPLAB® ICD 3 Design Advisory"* (DS50001764)
- *"MPLAB® REAL ICE™ In-Circuit Debugger User's Guide" (*DS50001616)
- *"Using MPLAB® REAL ICE™ Emulator"* (poster) (DS50001749)

2.5 JTAG

The TMS, TDO, TDI and TCK pins are used for testing and debugging according to the Joint Test Action Group (JTAG) standard. It is recommended to keep the trace length between the JTAG connector and the JTAG pins on the device as short as possible. If the JTAG connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the TMS, TDO, TDI and TCK pins are not recommended as they will interfere with the programmer or debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (VIH) and input low (VIL) requirements.

TABLE 4-15: SYSTEM BUS TARGET PROTECTION GROUP 5 REGISTER MAP (CONTINUED)

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
94A0	SBT5REG3	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
94B0	SBT5RD3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
94B8	SBT5WR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
94C0	SBT5REG4	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
94D0	SBT5RD4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
94D8	SBT5WR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-8 for the actual reset values.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0270	IPC19	31:16	—	—	—	ADCD20IP<2:0>			ADCD20IS<1:0>		—	—	—	ADCD19IP<2:0>			ADCD19IS<1:0>		0000
		15:0	—	—	—	ADCD18IP<2:0>			ADCD18IS<1:0>		—	—	—	ADCD17IP<2:0>			ADCD17IS<1:0>		0000
0280	IPC20	31:16	—	—	—	ADCD24IP<2:0>			ADCD24IS<1:0>		—	—	—	ADCD23IP<2:0>			ADCD23IS<1:0>		0000
		15:0	—	—	—	ADCD22IP<2:0>			ADCD22IS<1:0>		—	—	—	ADCD21IP<2:0>			ADCD21IS<1:0>		0000
0290	IPC21	31:16	—	—	—	ADCD28IP<2:0>			ADCD28IS<1:0>		—	—	—	ADCD27IP<2:0>			ADCD27IS<1:0>		0000
		15:0	—	—	—	ADCD26IP<2:0>			ADCD26IS<1:0>		—	—	—	ADCD25IP<2:0>			ADCD25IS<1:0>		0000
02A0	IPC22	31:16	—	—	—	ADCD32IP<2:0>			ADCD32IS<1:0>		—	—	—	ADCD31IP<2:0>			ADCD31IS<1:0>		0000
		15:0	—	—	—	ADCD30IP<2:0>			ADCD30IS<1:0>		—	—	—	ADCD29IP<2:0>			ADCD29IS<1:0>		0000
02B0	IPC23	31:16	—	—	—	ADCD36IP<2:0>			ADCD36IS<1:0>		—	—	—	ADCD35IP<2:0>			ADCD35IS<1:0>		0000
		15:0	—	—	—	ADCD34IP<2:0>			ADCD34IS<1:0>		—	—	—	ADCD33IP<2:0>			ADCD33IS<1:0>		0000
02C0	IPC24	31:16	—	—	—	ADCD40IP<2:0>			ADCD40IS<1:0>		—	—	—	ADCD39IP<2:0>			ADCD39IS<1:0>		0000
		15:0	—	—	—	ADCD38IP<2:0>			ADCD38IS<1:0>		—	—	—	ADCD37IP<2:0>			ADCD37IS<1:0>		0000
02D0	IPC25	31:16	—	—	—	USBSRIP<2:0>			USBSRIS<1:0>		—	—	—	ADCD43IP<2:0>			ADCD43IS<1:0>		0000
		15:0	—	—	—	ADCD42IP<2:0>			ADCD42IS<1:0>		—	—	—	ADCD41IP<2:0>			ADCD41IS<1:0>		0000
02E0	IPC26	31:16	—	—	—	CRPTIP<2:0>(2)			CRPTIS<1:0>(2)		—	—	—	SBIP<2:0>			SBIS<1:0>		0000
		15:0	—	—	—	CFDCIP<2:0>			CFDCIS<1:0>		—	—	—	CPCIP<2:0>			CPCIS<1:0>		0000
02F0	IPC27	31:16	—	—	—	SPI1TXIP<2:0>			SPI1TXIS<1:0>		—	—	—	SPI1RXIP<2:0>			SPI1RXIS<1:0>		0000
		15:0	—	—	—	SPI1EIP<2:0>			SPI1EIS<1:0>		—	—	—	—	—	—	—	—	0000
0300	IPC28	31:16	—	—	—	I2C1BIP<2:0>			I2C1BIS<1:0>		—	—	—	U1TXIP<2:0>			U1TXIS<1:0>		0000
		15:0	—	—	—	U1RXIP<2:0>			U1RXIS<1:0>		—	—	—	U1EIP<2:0>			U1EIS<1:0>		0000
0310	IPC29	31:16	—	—	—	CNBIP<2:0>			CNBIS<1:0>		—	—	—	CNAIP<2:0>			CNAIS<1:0>		0000
		15:0	—	—	—	I2C1MIP<2:0>			I2C1MIS<1:0>		—	—	—	I2C1SIP<2:0>			I2C1SIS<1:0>		0000
0320	IPC30	31:16	—	—	—	CNFIP<2:0>			CNFIS<1:0>		—	—	—	CNEIP<2:0>			CNEIS<1:0>		0000
		15:0	—	—	—	CNDIP<2:0>			CNDIS<1:0>		—	—	—	CNCIP<2:0>			CNCIS<1:0>		0000
0330	IPC31	31:16	—	—	—	CNKIP<2:0>			CNKIS<1:0>		—	—	—	CNJIP<2:0>			CNJIS<1:0>		0000
		15:0	—	—	—	CNHIP<2:0>			CNHIS<1:0>		—	—	—	CNGIP<2:0>			CNGIS<1:0>		0000
0340	IPC32	31:16	—	—	—	CMP2IP<2:0>			CMP2IS<1:0>		—	—	—	CMP1IP<2:0>			CMP1IS<1:0>		0000
		15:0	—	—	—	PMPEIP<2:0>			PMPEIS<1:0>		—	—	—	PMPIP<2:0>			PMPIS<1:0>		0000
0350	IPC33	31:16	—	—	—	DMA1IP<2:0>			DMA1IS<1:0>		—	—	—	DMA0IP<2:0>			DMA0IS<1:0>		0000
		15:0	—	—	—	USBDMAIP<2:0>			USBDMAIS<1:0>		—	—	—	USBIP<2:0>			USBIS<1:0>		0000
0360	IPC34	31:16	—	—	—	DMA5IP<2:0>			DMA5IS<1:0>		—	—	—	DMA4IP<2:0>			DMA4IS<1:0>		0000
		15:0	—	—	—	DMA3IP<2:0>			DMA3IS<1:0>		—	—	—	DMA2IP<2:0>			DMA2IS<1:0>		0000
0370	IPC35	31:16	—	—	—	SPI2RXIP<2:0>			SPI2RXIS<1:0>		—	—	—	SPI2EIP<2:0>			SPI2EIS<1:0>		0000
		15:0	—	—	—	DMA7IP<2:0>			DMA7IS<1:0>		—	—	—	DMA6IP<2:0>			DMA6IS<1:0>		0000
0380	IPC36	31:16	—	—	—	U2TXIP<2:0>			U2TXIS<1:0>		—	—	—	U2RXIP<2:0>			U2RXIS<1:0>		0000
		15:0	—	—	—	U2EIP<2:0>			U2EIS<1:0>		—	—	—	SPI2TXIP<2:0>			SPI2TXIS<1:0>		0000
0390	IPC37	31:16	—	—	—	CAN1IP<2:0>			CAN1IS<1:0>		—	—	—	I2C2MIP<2:0>			I2C2MIS<1:0>		0000
		15:0	—	—	—	I2C2SIP<2:0>			I2C2SIS<1:0>		—	—	—	I2C2BIP<2:0>			I2C2BIS<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is only available on devices with a Crypto module.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0630	OFF060	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0634	OFF061	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0638	OFF062	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
063C	OFF063	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0640	OFF064	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0644	OFF065	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0648	OFF066	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
064C	OFF067	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0650	OFF068	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0654	OFF069	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0658	OFF070	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
065C	OFF071	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0660	OFF072	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0664	OFF073	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0668	OFF074	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
066C	OFF075	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0670	OFF076	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0674	OFF077	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0678	OFF078	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is only available on devices with a Crypto module.

REGISTER 10-8: DCHxECON: DMA CHANNEL x EVENT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHAIRQ<7:0>(1)							
15:8	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHSIRQ<7:0>(1)							
7:0	S-0	S-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—

Legend:	S = Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **CHAIRQ<7:0>:** Channel Transfer Abort IRQ bits(1)

11111111 = Interrupt 255 will abort any transfers in progress and set CHAIF flag
•
•
•
00000001 = Interrupt 1 will abort any transfers in progress and set CHAIF flag
00000000 = Interrupt 0 will abort any transfers in progress and set CHAIF flag

bit 15-8 **CHSIRQ<7:0>:** Channel Transfer Start IRQ bits(1)

11111111 = Interrupt 255 will initiate a DMA transfer
•
•
•
00000001 = Interrupt 1 will initiate a DMA transfer
00000000 = Interrupt 0 will initiate a DMA transfer

bit 7 **CFORCE:** DMA Forced Transfer bit

1 = A DMA transfer is forced to begin when this bit is written to a '1'
0 = This bit always reads '0'

bit 6 **CABORT:** DMA Abort Transfer bit

1 = A DMA transfer is aborted when this bit is written to a '1'
0 = This bit always reads '0'

bit 5 **PATEN:** Channel Pattern Match Abort Enable bit

1 = Abort transfer and clear CHEN on pattern match
0 = Pattern match is disabled

bit 4 **SIRQEN:** Channel Start IRQ Enable bit

1 = Start channel cell transfer if an interrupt matching CHSIRQ occurs
0 = Interrupt number CHSIRQ is ignored and does not start a transfer

bit 3 **AIRQEN:** Channel Abort IRQ Enable bit

1 = Channel transfer is aborted if an interrupt matching CHAIRQ occurs
0 = Interrupt number CHAIRQ is ignored and does not terminate a transfer

bit 2-0 **Unimplemented:** Read as '0'

Note 1: See **Table 7-2: "Interrupt IRQ, Vector and Bit Location"** for the list of available interrupt IRQ sources.

NOTES:

REGISTER 11-30: USBCRCON: USB CLOCK/RESET CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R/W-1, HS
	—	—	—	—	—	USBIF	USBRF	USBWKUP
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	r-1	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	USB IDOVEN	USB IDVAL
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PHYIDEN	VBUS MONEN	ASVAL MONEN	BSVAL MONEN	SEND MONEN	USBIE	USBRIE	USB WKUPEN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **USBIF:** USB General Interrupt Flag bit
1 = An event on the USB Bus has occurred
0 = No interrupt from USB module or interrupts have not been enabled

bit 25 **USBRF:** USB Resume Flag bit
1 = Resume from Suspend state. Device wake-up activity can be started.
0 = No Resume activity detected during Suspend, or not in Suspend state

bit 24 **USBWKUP:** USB Activity Status bit
1 = Connect, disconnect, or other activity on USB detected since last cleared
0 = No activity detected on USB

Note: This bit should be cleared just prior to entering sleep, but it should be checked that no activity has already occurred on USB before actually entering sleep.

bit 23-16 **Unimplemented:** Read as '0'

bit 15 **Reserved:** Read as '1'

bit 14-10 **Unimplemented:** Read as '0'

bit 9 **USBIDOVEN:** USB ID Override Enable bit
1 = Enable use of USBIDVAL bit
0 = Disable use of USBIDVAL and instead use the PHY value

bit 8 **USBIDVAL:** USB ID Value bit
1 = ID override value is 1
0 = ID override value is 0

bit 7 **PHYIDEN:** PHY ID Monitoring Enable bit
1 = Enable monitoring of the ID bit from the USB PHY
0 = Disable monitoring of the ID bit from the USB PHY

bit 6 **VBUSMONEN:** VBUS Monitoring for OTG Enable bit
1 = Enable monitoring for VBUS in VBUS Valid range (between 4.4V and 4.75V)
0 = Disable monitoring for VBUS in VBUS Valid range

bit 5 **ASVALMONEN:** A-Device VBUS Monitoring for OTG Enable bit
1 = Enable monitoring for VBUS in Session Valid range for A-device (between 0.8V and 2.0V)
0 = Disable monitoring for VBUS in Session Valid range for A-device

bit 4 **BSVALMONEN:** B-Device VBUS Monitoring for OTG Enable bit
1 = Enable monitoring for VBUS in Session Valid range for B-device (between 0.8V and 4.0V)
0 = Disable monitoring for VBUS in Session Valid range for B-device

REGISTER 14-1: TxCON: TYPE B TIMER CONTROL REGISTER ('x' = 2-9) (CONTINUED)

bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timer Clock Source Select bit(1)
1 = External clock from TxCK pin
0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as '0'

Note 1: While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer1, Timer3, Timer5, Timer7, and Timer9). All timer functions are set through the even numbered timers.

2: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

3: This bit is available only on even numbered timers (Timer2, Timer4, Timer6, and Timer8).

19.0 DEEP SLEEP WATCHDOG TIMER (DSWDT)

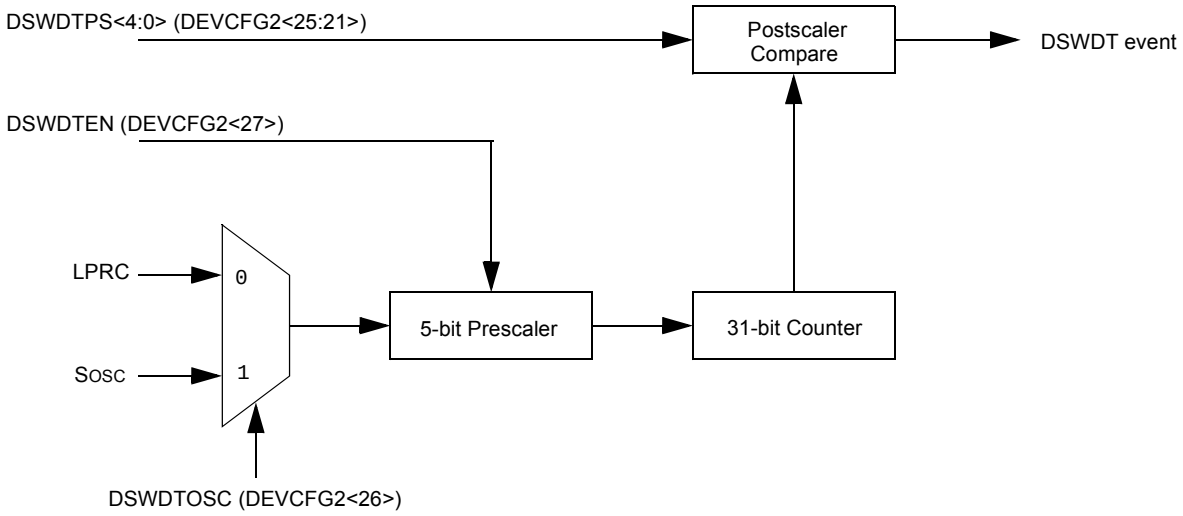
Note: This data sheet summarizes the features of the PIC32MZ Graphics (DA) Family family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9. "Watchdog, Deadman, and Power-up Timers"** (DS60001114), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Deep Sleep Watchdog Timer (DSWDT) is a dedicated Watchdog Timer for Deep Sleep mode operations of the device. The DSWDT is very useful in Battery-powered applications and in Low-Power modes of operations.

The primary function of the DSWDT is to automatically exit Deep Sleep mode after a prescribed amount of time has elapsed.

The DSWDT is controlled through the DEVCFG2 Configuration register at boot time (one-time programmable per POR). When enabled through the DSWDTEN bit in DEVCFG2, the DSWDT operates either from the internal Low-Power RC (LPRC) clock or from the Secondary Oscillator (SOSC). The clock selection for the DSWDT is done through the DSWDTOSC bit in the DEVCFG2 register.

FIGURE 19-1: DEEP SLEEP WATCHDOG TIMER BLOCK DIAGRAM



Example: When DSWDTOSC = 1, DSWDTPS<4:0> bits = 00000, and the SOSC is 32 kHz, the Watchdog delay is set to 1 ms.

REGISTER 20-6: ALRMDATE: ALARM DATE VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	MONTH10<3:0>				MONTH01<3:0>			
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	DAY10<1:0>				DAY01<3:0>			
7:0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	—	—	WDAY01<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-20 **MONTH10<3:0>:** Binary Coded Decimal value of months bits, 10 digits; contains a value from 0 to 1

bit 19-16 **MONTH01<3:0>:** Binary Coded Decimal value of months bits, 1 digit; contains a value from 0 to 9

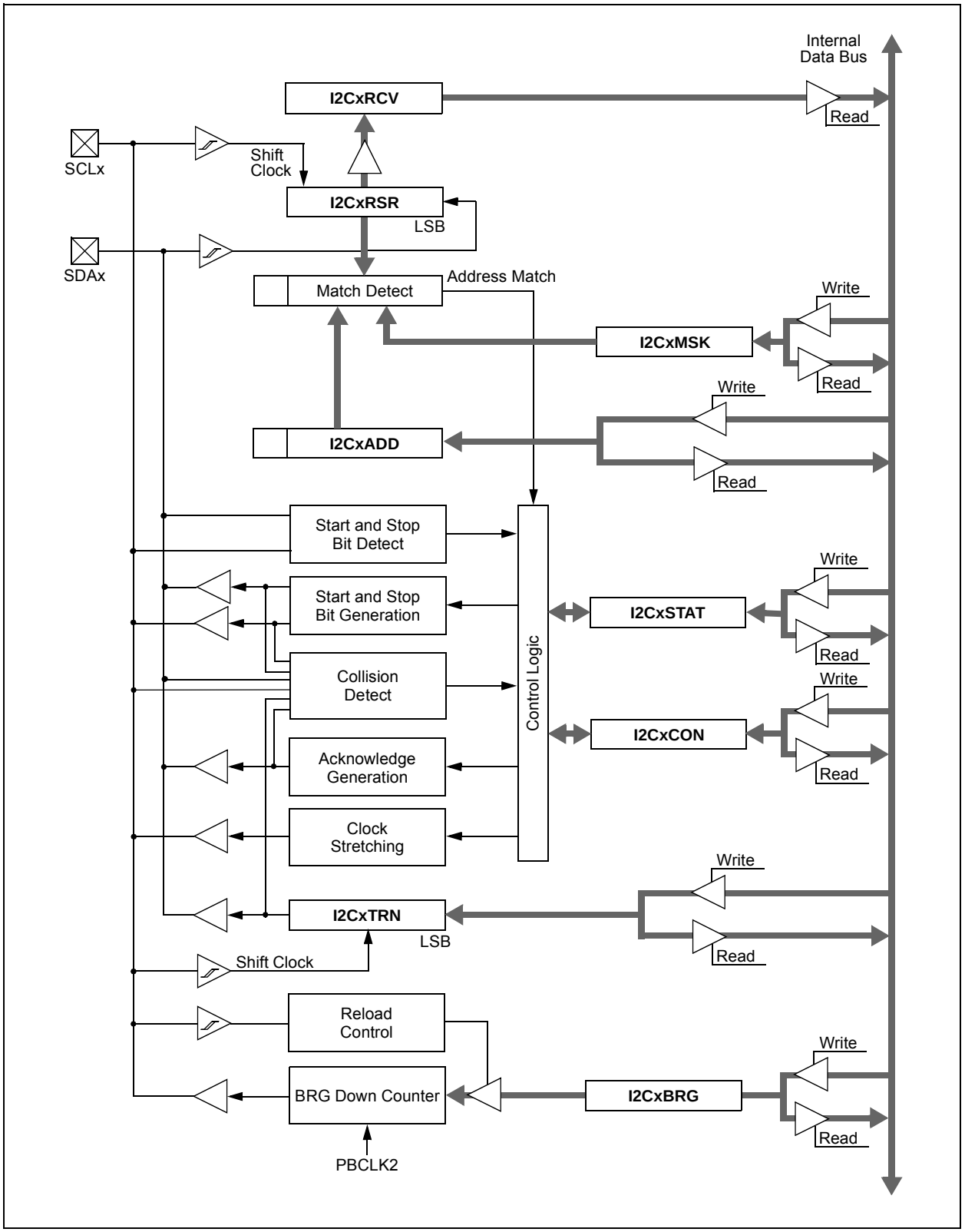
bit 15-12 **DAY10<3:0>:** Binary Coded Decimal value of days bits, 10 digits; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>:** Binary Coded Decimal value of days bits, 1 digit; contains a value from 0 to 9

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **WDAY01<3:0>:** Binary Coded Decimal value of weekdays bits, 1 digit; contains a value from 0 to 6

FIGURE 23-1: I²C BLOCK DIAGRAM



REGISTER 26-3: EBISMTx: EXTERNAL BUS INTERFACE STATIC MEMORY TIMING REGISTER ('x' = 0-2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	RDYMODE	PAGESIZE<1:0>	
23:16	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
	PAGEMODE	TPRC<3:0>(1)				TBTA<2:0>(1)		
15:8	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1
	TWP<5:0>(1)						TWR<1:0>(1)	
7:0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
	TAS<1:0>(1)		TRC<5:0>(1)					

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **RDYMODE:** Data Ready Device Select bit
The device associated with register set 'x' is a data-ready device, and will use the EBIRDYx pin.
1 = EBIRDYx input is used
0 = EBIRDYx input is not used

bit 25-24 **PAGESIZE<1:0>:** Page Size for Page Mode Device bits
11 = 32-word page
10 = 16-word page
01 = 8-word page
00 = 4-word page

bit 23 **PAGEMODE:** Memory Device Page Mode Support bit
1 = Device supports Page mode
0 = Device does not support Page mode

bit 22-19 **TPRC<3:0>:** Page Mode Read Cycle Time bits(1)
Read cycle time is TPRC + 1 clock cycle.

bit 18-16 **TBTA<2:0>:** Data Bus Turnaround Time bits(1)
Clock cycles (0-7) for static memory between read-to-write, write-to-read, and read-to-read when Chip Select changes.

bit 15-10 **TWP<5:0>:** Write Pulse Width bits(1)
Write pulse width is TWP + 1 clock cycle.

bit 9-8 **TWR<1:0>:** Write Address/Data Hold Time bits(1)
Number of clock cycles to hold address or data on the bus.

bit 7-6 **TAS<1:0>:** Write Address Setup Time bits(1)
Clock cycles for address setup time. A value of '0' is only valid in the case of SSRAM.

bit 5-0 **TRC<5:0>:** Read Cycle Time bits(1)
Read cycle time is TRC + 1 clock cycle.

Note 1: Refer to **Section 47. "External Bus Interface (EBI)"** in the *"PIC32 Family Reference Manual"* for the EBI timing diagrams and additional information.

REGISTER 31-12: ETHRXWM: ETHERNET CONTROLLER RECEIVE WATERMARKS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXFWM<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXEWM<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **RXFWM<7:0>:** Receive Full Watermark bits

The software controlled RX Buffer Full Watermark Pointer is compared against the RX BUFCNT to determine the full watermark condition for the FWMARK interrupt and for enabling Flow Control when automatic Flow Control is enabled. The Full Watermark Pointer should always be greater than the Empty Watermark Pointer.

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **RXEWM<7:0>:** Receive Empty Watermark bits

The software controlled RX Buffer Empty Watermark Pointer is compared against the RX BUFCNT to determine the empty watermark condition for the EWMARK interrupt and for disabling Flow Control when automatic Flow Control is enabled. The Empty Watermark Pointer should always be less than the Full Watermark Pointer.

Note: This register is only used for RX operations.

REGISTER 31-19: ETHMCOLFRM: ETHERNET CONTROLLER MULTIPLE COLLISION FRAMES STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MCOLFRMCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MCOLFRMCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **MCOLFRMCNT<15:0>:** Multiple Collision Frame Count bits
Increment count for frames that were successfully transmitted after there was more than one collision.

Note 1: This register is only used for TX operations.
2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.
3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

REGISTER 39-1: SDHCBLKCON: SDHC BLOCK CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BCOUNT<15:8>(1)							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BCOUNT<7:0>(1)							
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	BSIZE<9:8>(2)	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BSIZE<7:0>(2)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **BCOUNT<31:0>:** Blocks Count for Current Transfer bits(1)

These bits represent the number of blocks. The software sets this value between 1 and 65,535 blocks and the SDHC decrements the count after each block transfer and stops when the count reaches zero.
0xFFFF = 65,535 blocks
0x0002 = 2 blocks
0x0001 = 1 block
0x0000 = Stop count Blocks Count for Current Transfer bits

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **BSIZE<9:0>:** Transfer Block Size bits(2)

These bits specify the block size of the data transfer for CMD17, CMD18, CMD24, CMD25, and CMD53.
0x200 = 512 bytes
0x1FF = 511 bytes
•
•
•
0x002 = 2 bytes
0x001 = 1 byte
0x000 = No data transfer

Note 1: These bits are only used when the BCEN bit (SDHCMODE<1>) is set to '1' and is valid only for multiple block transfers. The BCOUNT<15:0> bits need not be set if the BSIZE bit (SDHCMODE<5>) is set to '0'.

2: These bits can only be accessed when no transactions are in progress. Read operations during transfers will return an invalid value and write operations to these bits will be ignored.

NOTES:

FIGURE 44-26: TRANSMIT SIGNAL TIMING RELATIONSHIPS AT THE MII

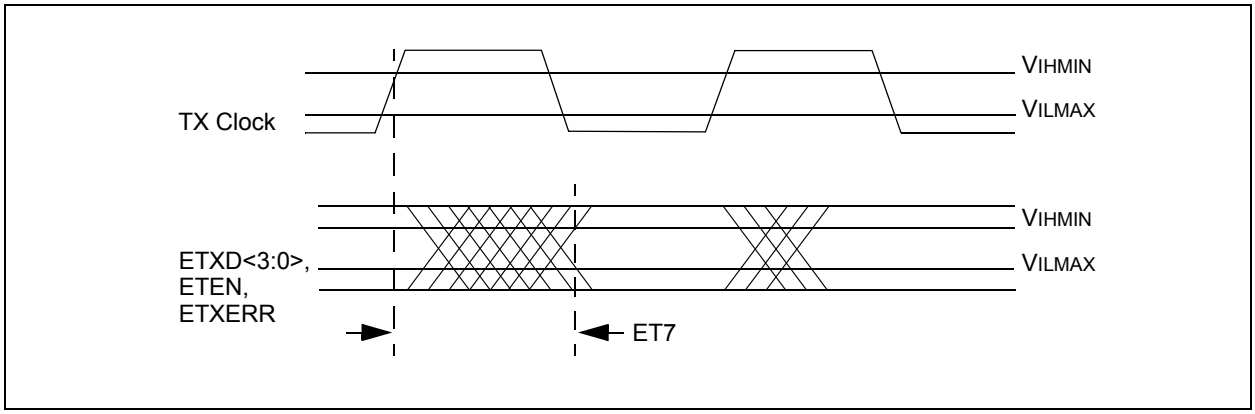
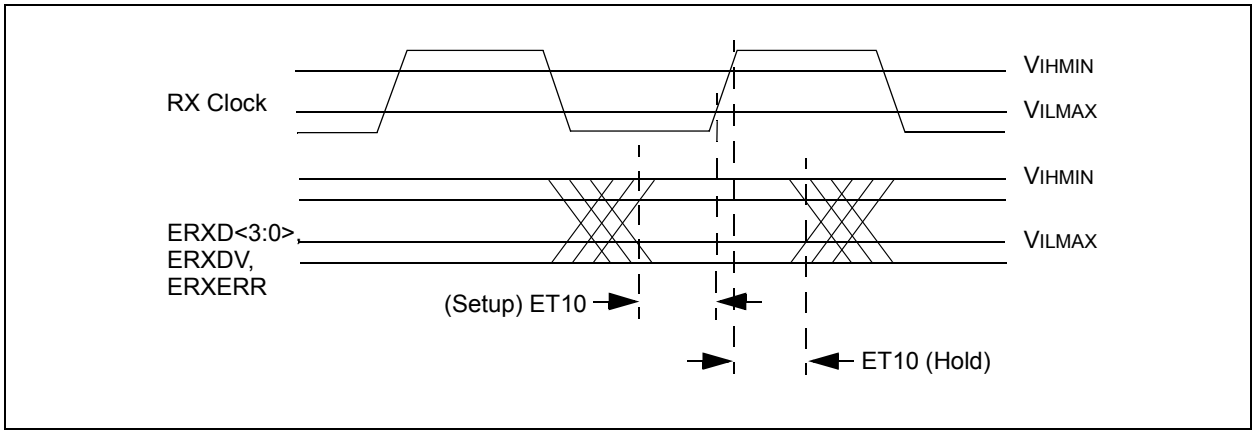


FIGURE 44-27: RECEIVE SIGNAL TIMING RELATIONSHIPS AT THE MII



Revision E (May 2017)

This revision includes the following major changes, which are referenced by their respective chapter in Table A-4.

In addition, minor updates to text and formatting were incorporated throughout the document.

TABLE A-4: MAJOR SECTION UPDATES

Section Name	Update Description
32-bit Graphics Applications MCUs (up to 2 MB Live Update Flash, 640 KB SRAM, and 32 MB DDR2 SDRAM) with XLP Technology	Updated the value of pin 168 from "CVREFOUT/AN5/RPB10/RB10" to "AN5/RPB10/RB10" (see Table 6).
25.0 "Parallel Master Port (PMP)"	The Virtual Address column heading was updated from BF80 to BF82 and the virtual addresses were updated from 70xx to E0xx (see Table 25-1).
36.0 "Graphics LCD (GLCD) Controller"	The resolutions in the key features list were updated.
39.0 "Secure Digital Host Controller (SDHC)"	The eMMC Standard: JESD84-A441 was added to the features list.
44.0 "Electrical Characteristics"	Table 44-7, Table 44-8, Table 44-9, Table 44-10, Table 44-11, Table 44-16, Table 44-18 updated various DC Characteristics parameters. Table 44-27, Table 44-28, Table 44-29 updated various AC Characteristics parameters.