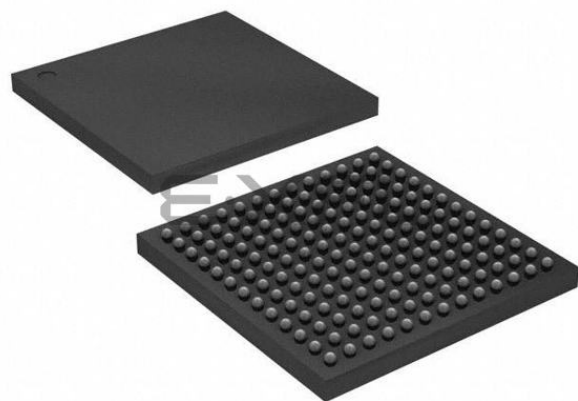




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Details

Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, I ² S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 45x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	169-LFBGA
Supplier Device Package	169-LFBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2064dah169t-i-6j

PIC32MZ Graphics (DA) Family

TABLE 1-16: ETHERNET MII I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
Ethernet						
ERXD0	N7	108	U12	I	ST	Ethernet Receive Data 0
ERXD1	M4	100	U10	I	ST	Ethernet Receive Data 1
ERXD2	N4	101	T10	I	ST	Ethernet Receive Data 2
ERXD3	N6	107	V12	I	ST	Ethernet Receive Data 3
ERXERR	M1	93	U8	I	ST	Ethernet Receive Error Input
ERXDV	M5	104	V11	I	ST	Ethernet Receive Data Valid
ERXCLK	N8	111	U13	I	ST	Ethernet Receive Clock
ETXD0	N9	113	V14	O	—	Ethernet Transmit Data 0
ETXD1	M9	112	T13	O	—	Ethernet Transmit Data 1
ETXD2	M8	110	V13	O	—	Ethernet Transmit Data 2
ETXD3	M7	109	T12	O	—	Ethernet Transmit Data 3
ETXERR	L10	118	V15	O	—	Ethernet Transmit Error
ETXEN	K11	121	V16	O	—	Ethernet Transmit Enable
ETXCLK	M10	120	T15	I	ST	Ethernet Transmit Clock
ECOL	M6	106	T11	I	ST	Ethernet Collision Detect
ECRS	N5	105	U11	I	ST	Ethernet Carrier Sense
EMDC	N10	119	U15	O	—	Ethernet Management Data Clock
EMDIO	K10	114	U14	I/O	—	Ethernet Management Data

Legend: CMOS = CMOS-compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = Transistor-transistor Logic input buffer
Analog = Analog input
O = Output
PPS = Peripheral Pin Select
P = Power
I = Input

TABLE 1-17: ETHERNET RMII PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
Ethernet MII Interface						
ERXD0	N7	108	U12	I	ST	Ethernet Receive Data 0
ERXD1	M4	100	U10	I	ST	Ethernet Receive Data 1
ERXERR	M1	93	U8	I	ST	Ethernet Receive Error Input
ETXD0	N9	113	V14	O	—	Ethernet Transmit Data 0
ETXD1	M9	112	T13	O	—	Ethernet Transmit Data 1
ETXEN	K11	121	V16	O	—	Ethernet Transmit Enable
EMDC	N10	119	U15	O	—	Ethernet Management Data Clock
EMDIO	K10	114	U14	I/O	—	Ethernet Management Data
EREFCLK	N8	111	U13	I	ST	Ethernet Reference Clock
ECRSDV	M5	104	V11	I	ST	Ethernet Carrier Sense Data Valid

Legend: CMOS = CMOS-compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = Transistor-transistor Logic input buffer
Analog = Analog input
O = Output
PPS = Peripheral Pin Select
P = Power
I = Input

PIC32MZ Graphics (DA) Family

TABLE 1-21: GRAPHICS LCD (GLCD) CONTROLLER PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
GLCD Controller						
GCLK	G11	148	L17	O	—	Graphics Display Pixel Clock
HSYNC	F12	149	L18	O	—	Graphics Display Horizontal Sync Pulse
VSYNC	F13	150	K18	O	—	Graphics Display Vertical Sync Pulse
GEN	G13	147	L16	O	—	Graphics Display Enable Output
GD0	G12	144	M16	O	—	Graphics Controller Data Output
GD1	L11	127	V17	O	—	
GD2	H1	76	U6	O	—	
GD3	N2	96	V9	O	—	
GD4	M2	95	T8	O	—	
GD5	K3	90	U7	O	—	
GD6	L1	91	V7	O	—	
GD7	J1	80	U5	O	—	
GD8	G10	143	N18	O	—	
GD9	F9	145	M17	O	—	
GD10	G2	74	R6	O	—	
GD11	G3	75	T6	O	—	
GD12	L13	134	R16	O	—	
GD13	H10	133	P15	O	—	
GD14	J10	132	R15	O	—	
GD15	M13	131	T18	O	—	
GD16	K2	89	T7	O	—	
GD17	L3	97	U9	O	—	
GD18	F8	146	M18	O	—	
GD19	M12	130	T17	O	—	
GD20	E8	151	K17	O	—	
GD21	L2	92	V8	O	—	
GD22	J2	81	N4	O	—	
GD23	K12	137	P16	O	—	

Legend: CMOS = CMOS-compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = Transistor-transistor Logic input buffer

Analog = Analog input
O = Output
PPS = Peripheral Pin Select

P = Power
I = Input

PIC32MZ Graphics (DA) Family

TABLE 1-22: DDR2 SDRAM CONTROLLER PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
DDR2 SDRAM Controller						
DDRCK	DDR Internal to the Package	DDR Internal to the Package	K2	O	SSTL	Differential Clocks
DDRCK			K1	O	SSTL	
DDRCKE			L2	O	SSTL	Clock Enable
DDRC $\overline{\text{S0}}$			N2	O	SSTL	Chip Select 0
DDRRAS			M1	O	SSTL	Row Address Strobe
DDRCAS			P2	O	SSTL	Column Address Strobe
DDRWE			L1	O	SSTL	Write Enable Strobe
DDRLDM			G3	O	SSTL	Lower Data Byte Mask
DDRUDM			A3	O	SSTL	Upper Data Byte Mask
DDRODT			N1	O	SSTL	On-Die Termination
DDRLDQS			E1	I/O	SSTL	Lower Data Byte Qualifier Strobes (Differential)
DDRLDQS			E2	I/O	SSTL	
DDRUDQS			B2	I/O	SSTL	Upper Data Byte Qualifier Strobes (Differential)
DDRUDQS			A2	I/O	SSTL	
DDRBA0			M2	O	SSTL	Bank Address Select 0
DDRBA1			M3	O	SSTL	Bank Address Select 1
DDRBA2			U4	O	SSTL	Bank Address Select 2
DDRA0			R1	O	SSTL	DDR2 Address Bus
DDRA1			L3	O	SSTL	
DDRA2			N3	O	SSTL	
DDRA3			R2	O	SSTL	
DDRA4			P3	O	SSTL	
DDRA5			T1	O	SSTL	
DDRA6			U1	O	SSTL	
DDRA7			T2	O	SSTL	
DDRA8			U2	O	SSTL	
DDRA9			R3	O	SSTL	
DDRA10			P1	O	SSTL	
DDRA11			V2	O	SSTL	
DDRA12			T3	O	SSTL	
DDRA13			U3	O	SSTL	
DDRA14			T4	O	SSTL	
DDRA15			V3	O	SSTL	

Legend: CMOS = CMOS-compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
TTL = Transistor-transistor Logic input buffer PPS = Peripheral Pin Select SSTL = Stub Series Terminated Logic

PIC32MZ Graphics (DA) Family

TABLE 1-23: POWER, GROUND, AND VOLTAGE REFERENCE PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP	288-pin LFBGA			
Power and Ground						
AVDD	D9	3, 4	F13, G13	P	P	Positive supply for analog modules. This pin must be connected at all times.
AVSS	C8, D8	5, 6	F12, G12	P	P	Ground reference for analog modules. This pin must be connected at all times.
VDDIO	B6, G9, H9, J9, K9, L6, L7, L9	19, 38, 86, 102, 117, 124, 155, 156, 165	C16, D15, D16, E15, F11, F15, G11, G15, H11, H12, H13, H15, J10, J15, K10, L11, L12, M12, M13, M15, N12, N13, R9, R10, R12, R13, R14	P	—	Positive supply for peripheral logic and I/O pins. This pin must be connected at all times.
VDDCORE	B4, C9, L8, N1	18, 39, 84, 116	D7, D14, R11, V4	P	—	1.8V positive supply for peripheral logic. This pin must be connected at all times.
VSS	C2, F5, G5, G6, G7, G8, H7, H8, J7, J8, K7, K8	21, 22, 29, 37, 48, 49, 83, 87, 94, 103, 115, 122, 123, 153, 154	A5, B5, C7, D10, D11, D12, D13, F9, F10, G10, H10, J11, J12, J13, K11, K12, K13, K15, L10, L13, L15, M10, M11, N10, N11, R7, R8	P	—	Ground reference for logic, I/O pins, and USB. This pin must be connected at all times.
HLVDIN	B12	173	E16	P	—	Low-voltage detect pin.
VBAT	D10	166	F16	P	—	Positive supply for the battery backed section. It is recommended to connect this pin to VDDIO if VBAT mode is not used (i.e., not connected to the battery).
VDDR1V8	H5, H6, J5, J6, K5, K6 (Note 2)	57, 58, 59, 60, 61, 62, 63, 67, 68, 72, 78 (Note 2)	H6, H7, H8, J6, J7, J8, K6, K7, K8, L6, L7, L8 (Note 2)	P	—	Positive supply for the DDR2 SDRAM memory.

Legend: CMOS = CMOS-compatible input or output Analog = Analog input P = Power
 ST = Schmitt Trigger input with CMOS levels O = Output I = Input
 TTL = Transistor-transistor Logic input buffer PPS = Peripheral Pin Select

- Note 1:** The metal plane at the bottom of the device is internally tied to VSS1V8 and must be connected to 1.8V ground externally.
2: This pin must be tied to Vss through a 20k Ω resistor in devices without DDR.
3: This pin is a No Connect in devices without DDR.

PIC32MZ Graphics (DA) Family

A block diagram of the PIC32MZ DA family processor core is shown in Figure 3-1.

FIGURE 3-1: PIC32MZ DA FAMILY MICROPROCESSOR CORE BLOCK DIAGRAM

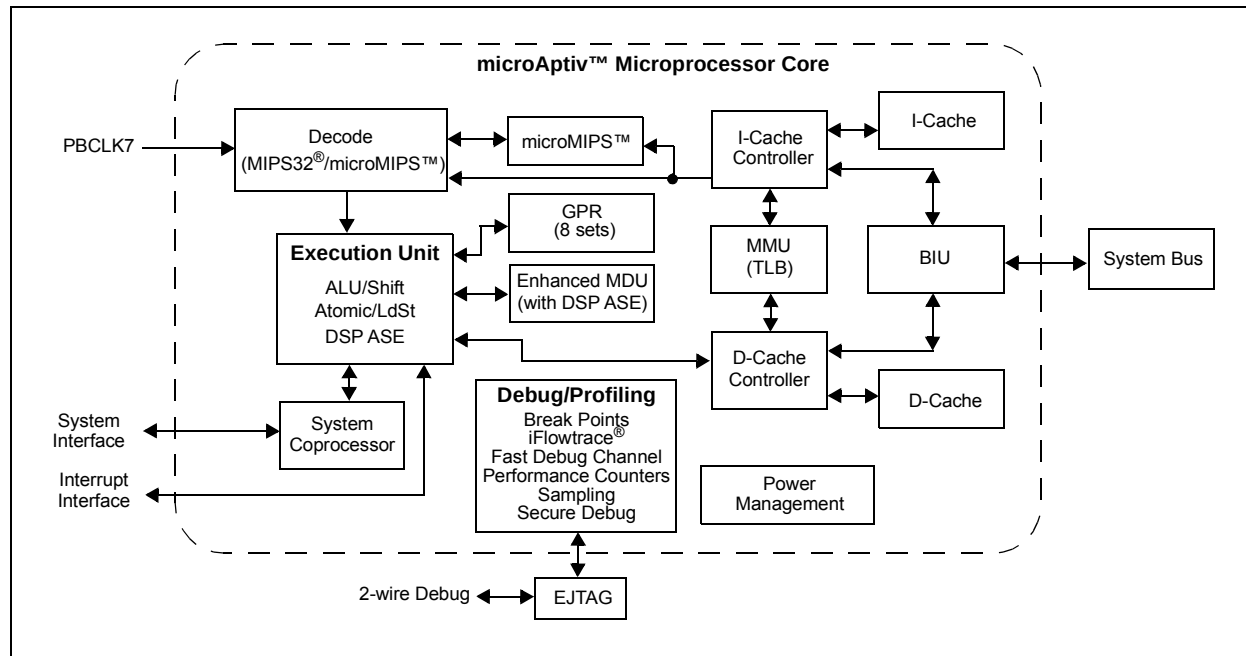


TABLE 4-15: SYSTEM BUS TARGET PROTECTION GROUP 5 REGISTER MAP (CONTINUED)

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
94A0	SBT5REG3	31:16	BASE<21:6>															xxxx
		15:0	BASE<5:0>					PRI	—	SIZE<4:0>					—	—	—	xxxx
94B0	SBT5RD3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0
94B8	SBT5WR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0
94C0	SBT5REG4	31:16	BASE<21:6>															xxxx
		15:0	BASE<5:0>					PRI	—	SIZE<4:0>					—	—	—	xxxx
94D0	SBT5RD4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0
94D8	SBT5WR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-8 for the actual reset values.

TABLE 4-19: SYSTEM BUS TARGET PROTECTION GROUP 9 REGISTER MAP

Virtual Address (BF90_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
8C20	SBT9ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>							REGION<3:0>				—	CMD<2:0>			0000
8C24	SBT9ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8C28	SBT9ECON	31:16	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8C30	SBT9ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8C38	SBT9ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8C40	SBT9REG0	31:16	BASE<21:6>															xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—
8C50	SBT9RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0
8C58	SBT9WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0
8C60	SBT9REG1	31:16	BASE<21:6>															xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—
8C70	SBT9RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0
8C78	SBT9WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-8 for the actual reset values.

PIC32MZ Graphics (DA) Family

REGISTER 7-7: IPCx: INTERRUPT PRIORITY CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP3<2:0>			IS3<1:0>	
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP2<2:0>			IS2<1:0>	
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP1<2:0>			IS1<1:0>	
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP0<2:0>			IS0<1:0>	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **IP3<2:0>:** Interrupt Priority bits

111 = Interrupt priority is 7

.

.

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 25-24 **IS3<1:0>:** Interrupt Sub-priority bits

11 = Interrupt sub-priority is 3

10 = Interrupt sub-priority is 2

01 = Interrupt sub-priority is 1

00 = Interrupt subdirectory is 0

bit 23-21 **Unimplemented:** Read as '0'

bit 20-18 **IP2<2:0>:** Interrupt Priority bits

111 = Interrupt priority is 7

.

.

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 17-16 **IS2<1:0>:** Interrupt Sub-priority bits

11 = Interrupt sub-priority is 3

10 = Interrupt sub-priority is 2

01 = Interrupt sub-priority is 1

00 = Interrupt sub-priority is 0

bit 15-13 **Unimplemented:** Read as '0'

Note: This register represents a generic definition of the IPCx register. Refer to Table 7-2 for the exact bit definitions.

PIC32MZ Graphics (DA) Family

REGISTER 8-2: OSCTUN: FRC TUNING REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	TUN<5:0> ⁽¹⁾					

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits⁽¹⁾

100000 = Center frequency -4%

100001 =

•

•

•

111111 =

000000 = Center frequency; Oscillator runs at nominal frequency (8 MHz)

000001 =

•

•

•

011110 =

011111 = Center frequency +4%

Note 1: OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step size is an approximation, and is neither characterized, nor tested.

Note: Writes to this register require an unlock sequence. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

PIC32MZ Graphics (DA) Family

REGISTER 10-2: DMASTAT: DMA STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	RDWR	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	—	—	—	—	—	DMACH<2:0>		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31 **RDWR:** Read/Write Status bit

1 = Last DMA bus access when an error was detected was a read

0 = Last DMA bus access when an error was detected was a write

bit 30-3 **Unimplemented:** Read as '0'

bit 2-0 **DMACH<2:0>:** DMA Channel bits

These bits contain the value of the most recent active DMA channel when an error was detected.

REGISTER 10-3: DMAADDR: DMA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **DMAADDR<31:0>:** DMA Module Address bits

These bits contain the address of the most recent DMA access when an error was detected.

PIC32MZ Graphics (DA) Family

REGISTER 10-8: DCHxECON: DMA CHANNEL x EVENT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHAIRQ<7:0> ⁽¹⁾							
15:8	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHSIRQ<7:0> ⁽¹⁾							
7:0	S-0	S-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—

Legend:	S = Settable bit
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	U = Unimplemented bit, read as '0'
	'0' = Bit is cleared
	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **CHAIRQ<7:0>:** Channel Transfer Abort IRQ bits⁽¹⁾

11111111 = Interrupt 255 will abort any transfers in progress and set CHAIF flag

•
•
•

00000001 = Interrupt 1 will abort any transfers in progress and set CHAIF flag

00000000 = Interrupt 0 will abort any transfers in progress and set CHAIF flag

bit 15-8 **CHSIRQ<7:0>:** Channel Transfer Start IRQ bits⁽¹⁾

11111111 = Interrupt 255 will initiate a DMA transfer

•
•
•

00000001 = Interrupt 1 will initiate a DMA transfer

00000000 = Interrupt 0 will initiate a DMA transfer

bit 7 **CFORCE:** DMA Forced Transfer bit

1 = A DMA transfer is forced to begin when this bit is written to a '1'

0 = This bit always reads '0'

bit 6 **CABORT:** DMA Abort Transfer bit

1 = A DMA transfer is aborted when this bit is written to a '1'

0 = This bit always reads '0'

bit 5 **PATEN:** Channel Pattern Match Abort Enable bit

1 = Abort transfer and clear CHEN on pattern match

0 = Pattern match is disabled

bit 4 **SIRQEN:** Channel Start IRQ Enable bit

1 = Start channel cell transfer if an interrupt matching CHSIRQ occurs

0 = Interrupt number CHSIRQ is ignored and does not start a transfer

bit 3 **AIRQEN:** Channel Abort IRQ Enable bit

1 = Channel transfer is aborted if an interrupt matching CHAIRQ occurs

0 = Interrupt number CHAIRQ is ignored and does not terminate a transfer

bit 2-0 **Unimplemented:** Read as '0'

Note 1: See Table 7-2: "Interrupt IRQ, Vector and Bit Location" for the list of available interrupt IRQ sources.

REGISTER 11-1: USBCSR0: USB CONTROL STATUS REGISTER 0 (CONTINUED)

- bit 10 **RESUME:** Resume from Suspend control bit
 1 = Generate Resume signaling when the device is in Suspend mode
 0 = Stop Resume signaling
- In *Device mode*, the software should clear this bit after 10 ms (a maximum of 15 ms) to end Resume signaling. In *Host mode*, the software should clear this bit after 20 ms.
- bit 9 **SUSPMODE:** Suspend Mode status bit
 1 = The USB module is in Suspend mode
 0 = The USB module is in Normal operations
- This bit is read-only in Device mode. In Host mode, it can be set by software, and is cleared by hardware.
- bit 8 **SUSPEN:** Suspend Mode Enable bit
 1 = Suspend mode is enabled
 0 = Suspend mode is not enabled
- bit 7 **Unimplemented:** Read as '0'
- bit 6-0 **FUNC<6:0>:** Device Function Address bits
- These bits are only available in *Device mode*. This field is written with the address received through a SET_ADDRESS command, which will then be used for decoding the function address in subsequent token packets.

TABLE 12-10: PORTH REGISTER MAP

Virtual Address (BF86_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0700	ANSELH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	ANSH11	—	—	—	ANSH7	—	—	ANSH4	ANSH3	—	—	—	0898
0710	TRISH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISH15	TRISH14	TRISH13	TRISH12	TRISH11	TRISH10	TRISH9	TRISH8	TRISH7	TRISH6	TRISH5	TRISH4	TRISH3	TRISH2	TRISH1	TRISH0	FFFF
0720	PORTH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RH15	RH14	RH13	RH12	RH11	RH10	RH9	RH8	RH7	RH6	RH5	RH4	RH3	RH2	RH1	RH0	xxxx
0730	LATH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATH15	LATH14	LATH13	LATH12	LATH11	LATH10	LATH9	LATH8	LATH7	LATH6	LATH5	LATH4	LATH3	LATH2	LATH1	LATH0	xxxx
0740	ODCH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCH15	ODCH14	ODCH13	ODCH12	ODCH11	ODCH10	ODCH9	ODCH8	ODCH7	ODCH6	ODCH5	ODCH4	ODCH3	ODCH2	ODCH1	ODCH0	0000
0750	CNPUH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUH15	CNPUH14	CNPUH13	CNPUH12	CNPUH11	CNPUH10	CNPUH9	CNPUH8	CNPUH7	CNPUH6	CNPUH5	CNPUH4	CNPUH3	CNPUH2	CNPUH1	CNPUH0	0000
0760	CNPDH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDH15	CNPDH14	CNPDH13	CNPDH12	CNPDH11	CNPDH10	CNPDH9	CNPDH8	CNPDH7	CNPDH6	CNPDH5	CNPDH4	CNPDH3	CNPDH2	CNPDH1	CNPDH0	0000
0770	CNCONH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0780	CNENH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEH15	CNIEH14	CNIEH13	CNIEH12	CNIEH11	CNIEH10	CNIEH9	CNIEH8	CNIEH7	CNIEH6	CNIEH5	CNIEH4	CNIEH3	CNIEH2	CNIEH1	CNIEH0	0000
0790	CNSTATH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATH15	CN STATH14	CN STATH13	CN STATH12	CN STATH11	CN STATH10	CN STATH9	CN STATH8	CN STATH7	CN STATH6	CN STATH5	CN STATH4	CN STATH3	CN STATH2	CN STATH1	CN STATH0	0000
07A0	CNNEH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEH15	CNNEH14	CNNEH13	CNNEH12	CNNEH11	CNNEH10	CNNEH9	CNNEH8	CNNEH7	CNNEH6	CNNEH5	CNNEH4	CNNEH3	CNNEH2	CNNEH1	CNNEH0	0000
07B0	CNFH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFH15	CNFH14	CNFH13	CNFH12	CNFH11	CNFH10	CNFH9	CNFH8	CNFH7	CNFH6	CNFH5	CNFH4	CNFH3	CNFH2	CNFH1	CNFH0	0000
07C0	SRCON0H	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR1H15	SR1H14	SR1H13	SR1H12	SR1H11	SR1H10	SR1H9	SR1H8	SR1H7	SR1H6	SR1H5	SR1H4	SR1H3	SR1H2	SR1H1	SR1H0	0000
07D0	SRCON1H	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR0H15	SR0H14	SR0H13	SR0H12	SR0H11	SR0H10	SR0H9	SR0H8	SR0H7	SR0H6	SR0H5	SR0H4	SR0H3	SR0H2	SR0H1	SR0H0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

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REGISTER 21-3: SPIxSTAT: SPI STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	RXBUFELM<4:0>				
23:16	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	TXBUFELM<4:0>				
15:8	U-0	U-0	U-0	R/C-0, HS	R-0	U-0	U-0	R-0
	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR
7:0	R-0	R/W-0	R-0	U-0	R-1	U-0	R-0	R-0
	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF

Legend:	C = Clearable bit	HS = Hardware Set
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **RXBUFELM<4:0>**: Receive Buffer Element Count bits (valid only when ENHBUF = 1)

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **TXBUFELM<4:0>**: Transmit Buffer Element Count bits (valid only when ENHBUF = 1)

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **FRMERR**: SPI Frame Error status bit

1 = Frame error detected

0 = No Frame error detected

This bit is only valid when FRMEN = 1.

bit 11 **SPIBUSY**: SPI Activity Status bit

1 = SPI peripheral is currently busy with some transactions

0 = SPI peripheral is currently idle

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **SPITUR**: Transmit Under Run bit

1 = Transmit buffer has encountered an underrun condition

0 = Transmit buffer has no underrun condition

This bit is only valid in Framed Sync mode; the underrun condition must be cleared by disabling/re-enabling the module.

bit 7 **SRMT**: Shift Register Empty bit (valid only when ENHBUF = 1)

1 = When SPI module shift register is empty

0 = When SPI module shift register is not empty

bit 6 **SPIROV**: Receive Overflow Flag bit

1 = A new data is completely received and discarded. The user software has not read the previous data in the SPIxBUF register.

0 = No overflow has occurred

This bit is set in hardware; can only be cleared (= 0) in software.

bit 5 **SPIRBE**: RX FIFO Empty bit (valid only when ENHBUF = 1)

1 = RX FIFO is empty (CRPTR = SWPTR)

0 = RX FIFO is not empty (CRPTR ≠ SWPTR)

bit 4 **Unimplemented:** Read as '0'

22.1 SQI Control Registers

TABLE 22-1: SERIAL QUADRATURE INTERFACE (SQI) REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0		
2000	SQI1 XCON1	31:16	—	—	SDRCMD	DDRDATA	DDR DUMMY	DDR MODE	DDR ADDR	DDRCMD	DUMMYBYTES<2:0>			ADDRBYTES<2:0>			READOPCODE<7:6>		0000	
		15:0	READOPCODE<5:0>							TYPEDATA<1:0>		TYPEDUMMY<1:0>		TYPEMODE<1:0>		TYPEADDR<1:0>		TYPECMD<1:0>		0000
2004	SQI1 XCON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	DEVSEL<1:0>		MODEBYTES<1:0>		MODECODE<7:0>								0000	
2008	SQI1CFG	31:16	—	—	—	—	—	—	CSEN<1:0>		SQIEN	—	DATAEN<1:0>		CON BUFRST	RXBUFST	TXBUFST	RESET	0000	
		15:0	—	—	—	BURSTEN	—	HOLD	WP	—	—	—	LSBF	CPOL	CPHA	MODE<2:0>			0000	
200C	SQI1CON	31:16	—	—	—	—	—	—	—	SCHECK	DDRMODE	DASSERT	DEVSEL<1:0>		LANEMODE<1:0>		CMDINIT<1:0>		0000	
		15:0	TXRXCOUNT<15:0>																	0000
2010	SQI1 CLKCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	CLKDIV<10:8>			0000	
		15:0	CLKDIV<7:0>							—	—	—	—	—	—	—	STABLE	EN	0000	
2014	SQI1 CMDTHR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	TXCMDTHR<5:0>					—	—	RXCMDTHR<5:0>						0000		
2018	SQI1 INTTHR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	TXINTTHR<5:0>						—	—	RXINTTHR<5:0>						0000	
201C	SQI1 INTEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	DMAEIE	PKT COMPIE	BD DONEIE	CON THRIE	CON EMPTYIE	CON FULLIE	RX THRIE	RX FULLIE	RX EMPTYIE	TX THRIE	TX FULLIE	TX EMPTYIE	0000	
2020	SQI1 INTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	DMAEIF	PKT COMPIF	BD DONEIF	CON THRIF	CON EMPTYIF	CON FULLIF	RX THRIF	RX FULLIF	RX EMPTYIF	TX THRIF	TX FULLIF	TX EMPTYIF	0000	
2024	SQI1 TXDATA	31:16	TXDATA<31:16>																	0000
		15:0	TXDATA<15:0>																	0000
2028	SQI1 RXDATA	31:16	RXDATA<31:16>																	0000
		15:0	RXDATA<15:0>																	0000
202C	SQI1 STAT1	31:16	—	—	—	—	—	—	—	—	—	—	TXBUFFREE<5:0>					0000		
		15:0	—	—	—	—	—	—	—	—	—	RXBUFCNT<5:0>					0000			
2030	SQI1 STAT2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CMDSTAT<1:0>		0000	
		15:0	—	—	—	—	—	CONAVAIL<3:0>				SDID3	SDID2	SDID1	SDID0	—	RXUN	TXOV	00x0	
2034	SQI1 BDCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	START	POLLEN	DMAEN	0000	
2038	SQI1BD CURADD	31:16	BDCURRADDR<31:16>																	0000
		15:0	BDCURRADDR<15:0>																	0000
2040	SQI1BD BASEADD	31:16	BDADDR<31:16>																	0000
		15:0	BDADDR<15:0>																	0000

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REGISTER 22-8: SQI1INTEN: SQI INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	DMAEIE	PKTCOMPIE	BDDONEIE	CONTHRIE
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CONEMPTYIE	CONFULLIE	RXTHRIE	RXFULLIE	RXEMPTYIE	TXTHRIE	TXFULLIE	TXEMPTYIE

Legend:	HS = Hardware Set	U = Unimplemented bit, read as '0'
R = Readable bit	W = Writable bit	'0' = Bit is cleared
-n = Value at POR	'1' = Bit is set	x = Bit is unknown

bit 31-12 **Unimplemented:** Read as '0'

bit 11 **DMAEIE:** DMA Bus Error Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 10 **PKTCOMPIE:** DMA Buffer Descriptor Packet Complete Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 9 **BDDONEIE:** DMA Buffer Descriptor Done Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 8 **CONTHRIE:** Control Buffer Threshold Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 7 **CONEMPTYIE:** Control Buffer Empty Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 6 **CONFULLIE:** Control Buffer Full Interrupt Enable bit

This bit enables an interrupt when the receive buffer is full.

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 5 **RXTHRIE:** Receive Buffer Threshold Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 4 **RXFULLIE:** Receive Buffer Full Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 3 **RXEMPTYIE:** Receive Buffer Empty Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 2 **TXTHRIE:** Transmit Threshold Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 1 **TXFULLIE:** Transmit Buffer Full Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 0 **TXEMPTYIE:** Transmit Buffer Empty Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

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26.0 EXTERNAL BUS INTERFACE (EBI)

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DA) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 47. “External Bus Interface (EBI)”**, which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

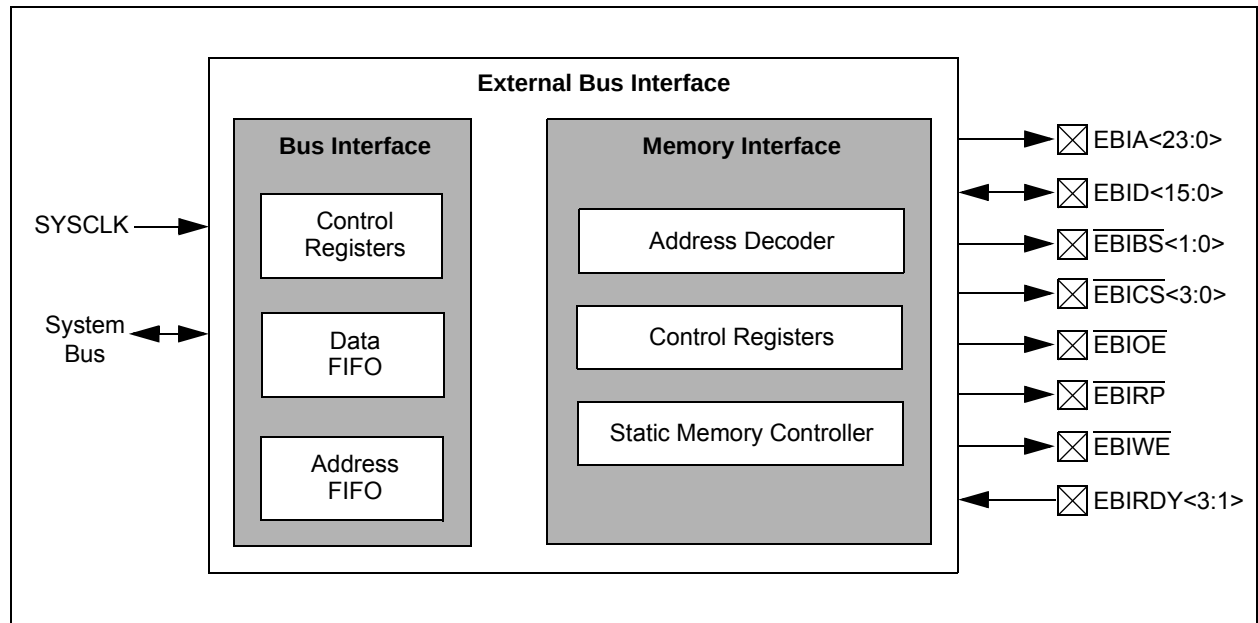
The External Bus Interface (EBI) module provides a high-speed, convenient way to interface external parallel memory devices to the PIC32MZ DA family device.

With the EBI module, it is possible to connect asynchronous SRAM and NOR Flash devices, as well as non-memory devices such as camera sensors and LCDs.

Note 1: Once the EBI module is configured, external devices will be memory mapped and can be access from KSEG2 memory space (see Figure 4-1 through Figure 4-2 in **Section 4.0 “Memory Organization”** for more information). The MMU must be enabled and the TLB must be set up to access this memory (see **Section 50. “CPU for Devices with MIPS32® microAptiv™ and M-Class Cores”** (DS60001192) in the *“PIC32 Family Reference Manual”* for more information).

2: When using the EBI module, Graphics LCD (GLCD) Controller functionality is not available, as most of the I/O between the EBI module and the GLCD is shared.

FIGURE 26-1: EBI SYSTEM BLOCK DIAGRAM



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REGISTER 27-1: CEVER: CRYPTO ENGINE REVISION, VERSION, AND ID REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	REVISION<7:0>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	VERSION<7:0>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	ID<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	ID<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-24 **REVISION<7:0>**: Crypto Engine Revision bits

bit 23-16 **VERSION<7:0>**: Crypto Engine Version bits

bit 15-0 **ID<15:0>**: Crypto Engine Identification bits

29.0 12-BIT HIGH-SPEED SUCCESSIVE APPROXIMATION REGISTER (SAR) ANALOG-TO-DIGITAL CONVERTER (ADC)

Note: This data sheet summarizes the features of the PIC32MZ DA family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 22. “12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)”** (DS60001344) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32).

The 12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) includes the following features:

- 12-bit resolution
- Six ADC modules with dedicated Sample and Hold (S&H) circuits
- Two dedicated ADC modules can be combined in Turbo mode to provide double conversion rate (clock sources for combined ADCs must be synchronous)
- Up to 45 analog input sources, in addition to the internal CTMU, VBAT, internal voltage reference and internal temperature sensor
- Single-ended and/or differential inputs
- Can operate during Sleep mode
- Supports touch sense applications
- Six digital comparators
- Six digital filters supporting two modes:
 - Oversampling mode
 - Averaging mode
- 16-word FIFO on ADC0 through ADC4 for increased throughput
- Early interrupt generation resulting in faster processing of converted data
- Designed for motor control, power conversion, and general purpose applications
- Operation during Sleep and Idle modes

A simplified block diagram of the ADC module is illustrated in Figure 29-1.

The 12-bit HS SAR ADC has up to five dedicated ADC modules (ADC0-ADC4) and one shared ADC module (ADC7). The dedicated ADC modules use a single input (or its alternate) and are intended for high-speed and precise sampling of time-sensitive or transient inputs. The the shared ADC module incorporates a multiplexer on the input to facilitate a larger group of inputs, with slower sampling, and provides flexible automated scanning option through the input scan logic.

For each ADC module, the analog inputs are connected to the S&H capacitor. The clock, sampling time, and output data resolution for each ADC module can be set independently. The ADC module performs the conversion of the input analog signal based on the configurations set in the registers. When conversion is complete, the final result is stored in the result buffer for the specific analog input and is passed to the digital filter and digital comparator if configured to use data from this particular sample. Input to ADCx mapping is illustrated in Figure 29-2.

29.1 Activation Sequence

Step 1: Initialize the ADC calibration values by copying them from the factory programmed DEVADCx Flash locations starting at 0xBFC45000 into the ADCxCFG registers starting at 0xBF887D00. Then, configure the AICPMPEN bit (ADCCON1<12> and the IOANCPEN bit (CFGCON<7>) = 1 if and only if VDD is less than 2.5V. The default is '0', which assumes VDD is greater than or equal to 2.5V.

Step 2: The user writes all the essential ADC configuration SFRs including the ADC control clock and all ADC core clocks setup:

- ADCCON1, keeping the ON bit = 0
- ADCCON2, especially paying attention to ADC-DIV<6:0> and SAMC<9:0>
- ADCANCON, keeping all analog enables ANENx bit = 0, WKUPCLKCNT bit = 0xA
- ADCCON3, keeping all DIGEN5x = 0, especially paying attention to ADCSEL<1:0>, CONCLKDIV<5:0>, and VREFSEL<2:0>
- ADCxTIME, ADCDIVx<6:0>, and SAMCx<9:0>
- ADCTRGMODE, ADCIMCONx, ADCTRGSNS, ADCCSSx, ADCGIRQENx, ADCTRGx, ADC-BASE
- Comparators, filters, and so on

Step 3: The user sets the ANENx bit to '1' for the ADC SAR Cores needed (which internally in the ADC module enables the control clock to generate by division the core clocks for the desired ADC SAR Cores, which in turn enables the bias circuitry for these ADC SAR Cores).

PIC32MZ Graphics (DA) Family

REGISTER 30-5: CiTREC: CAN TRANSMIT/RECEIVE ERROR COUNT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	—	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	TERRCNT<7:0>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RERRCNT<7:0>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31-22 **Unimplemented:** Read as '0'
- bit 21 **TXBO:** Transmitter in Error State Bus OFF ($TERRCNT \geq 256$)
- bit 20 **TXBP:** Transmitter in Error State Bus Passive ($TERRCNT \geq 128$)
- bit 19 **RXBP:** Receiver in Error State Bus Passive ($RERRCNT \geq 128$)
- bit 18 **TXWARN:** Transmitter in Error State Warning ($128 > TERRCNT \geq 96$)
- bit 17 **RXWARN:** Receiver in Error State Warning ($128 > RERRCNT \geq 96$)
- bit 16 **EWARN:** Transmitter or Receiver is in Error State Warning
- bit 15-8 **TERRCNT<7:0>:** Transmit Error Counter
- bit 7-0 **RERRCNT<7:0>:** Receive Error Counter

REGISTER 30-6: CiFSTAT: CAN FIFO STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP31	FIFOIP30	FIFOIP29	FIFOIP28	FIFOIP27	FIFOIP26	FIFOIP25	FIFOIP24
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP23	FIFOIP22	FIFOIP21	FIFOIP20	FIFOIP19	FIFOIP18	FIFOIP17	FIFOIP16
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP15	FIFOIP14	FIFOIP13	FIFOIP12	FIFOIP11	FIFOIP10	FIFOIP9	FIFOIP8
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP7	FIFOIP6	FIFOIP5	FIFOIP4	FIFOIP3	FIFOIP2	FIFOIP1	FIFOIP0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31-0 **FIFOIP<31:0>:** FIFO Interrupt Pending bits
- 1 = One or more enabled FIFO interrupts are pending
- 0 = No FIFO interrupts are pending