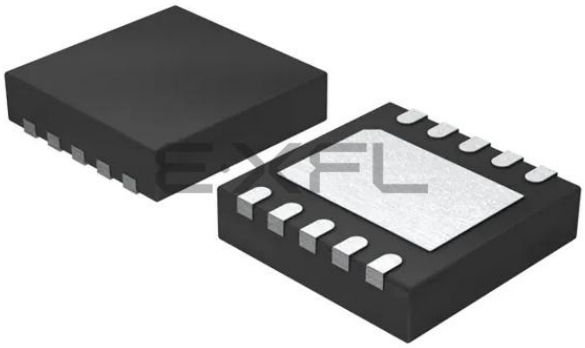

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	6
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	10-VFDFN Exposed Pad
Supplier Device Package	10-DFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f521a-im

Table of Contents

1.1. Ordering Information

The following features are common to all devices in this family:

- 25 MHz system clock and 25 MIPS throughput (peak)
- 256 bytes of internal RAM
- Enhanced SPI peripheral
- Enhanced UART peripheral
- Three Timers
- Three Programmable Counter Array channels
- Internal 24.5 MHz oscillator
- Internal Voltage Regulator
- 12-bit, 200 ksps ADC
- Internal Voltage Reference and Temperature Sensor
- One Analog Comparator

Table 1.1 shows the features that differentiate the devices in this family.

Table 1.1. Product Selection Guide (Recommended for New Designs)

Ordering Part Number	Flash Memory (kB)	Port I/Os	LIN	Package	Ordering Part Number	Flash Memory (kB)	Port I/Os	LIN	Package
C8051F520-C-IM	8	6	✓	DFN-10	C8051F534-C-IM	4	16	—	QFN-20
C8051F521-C-IM	8	6	—	DFN-10	C8051F536-C-IM	2	16	✓	QFN-20
C8051F523-C-IM	4	6	✓	DFN-10	C8051F537-C-IM	2	16	—	QFN-20
C8051F524-C-IM	4	6	—	DFN-10	C8051F530-C-IT	8	16	✓	TSSOP-20
C8051F526-C-IM	2	6	✓	DFN-10	C8051F531-C-IT	8	16	—	TSSOP-20
C8051F527-C-IM	2	6	—	DFN-10	C8051F533-C-IT	4	16	✓	TSSOP-20
C8051F530-C-IM	8	16	✓	QFN-20	C8051F534-C-IT	4	16	—	TSSOP-20
C8051F531-C-IM	8	16	—	QFN-20	C8051F536-C-IT	2	16	✓	TSSOP-20
C8051F533-C-IM	4	16	✓	QFN-20	C8051F537-C-IT	2	16	—	TSSOP-20

All devices in Table 1.1 are also available in an automotive version. For the automotive version, the -I in the ordering part number is replaced with -A. For example, the automotive version of the C8051F520-C-IM is the C8051F520-C-AM.

The -AM and -AT devices receive full automotive quality production status, including AEC-Q100 qualification (fault coverage report available upon request), registration with International Material Data System (IMDS) and Part Production Approval Process (PPAP) documentation. PPAP documentation is available at www.silabs.com with a registered NDA and approved user account. The -AM and -AT devices enable high volume automotive OEM applications with their enhanced testing and processing. Please contact Silicon Labs sales for more information regarding -AM and -AT devices for your automotive project.

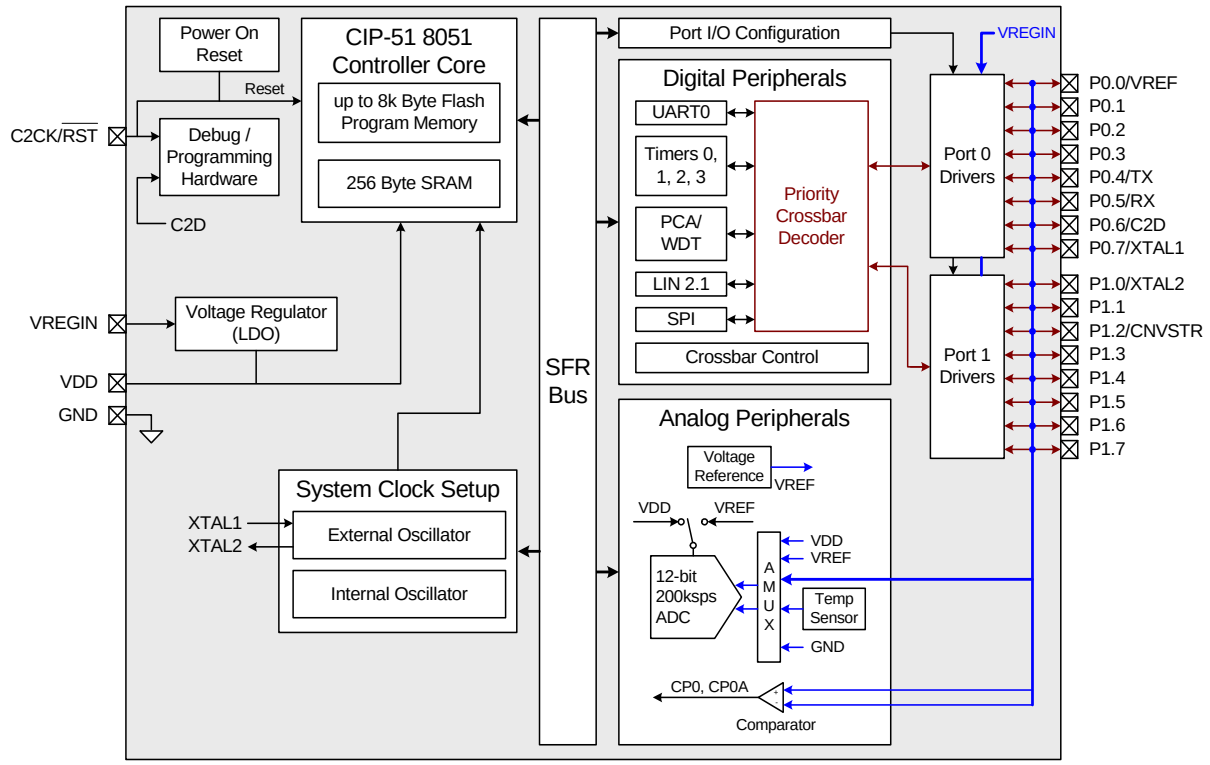

Figure 1.1. C8051F53xA/F53x-C Block Diagram

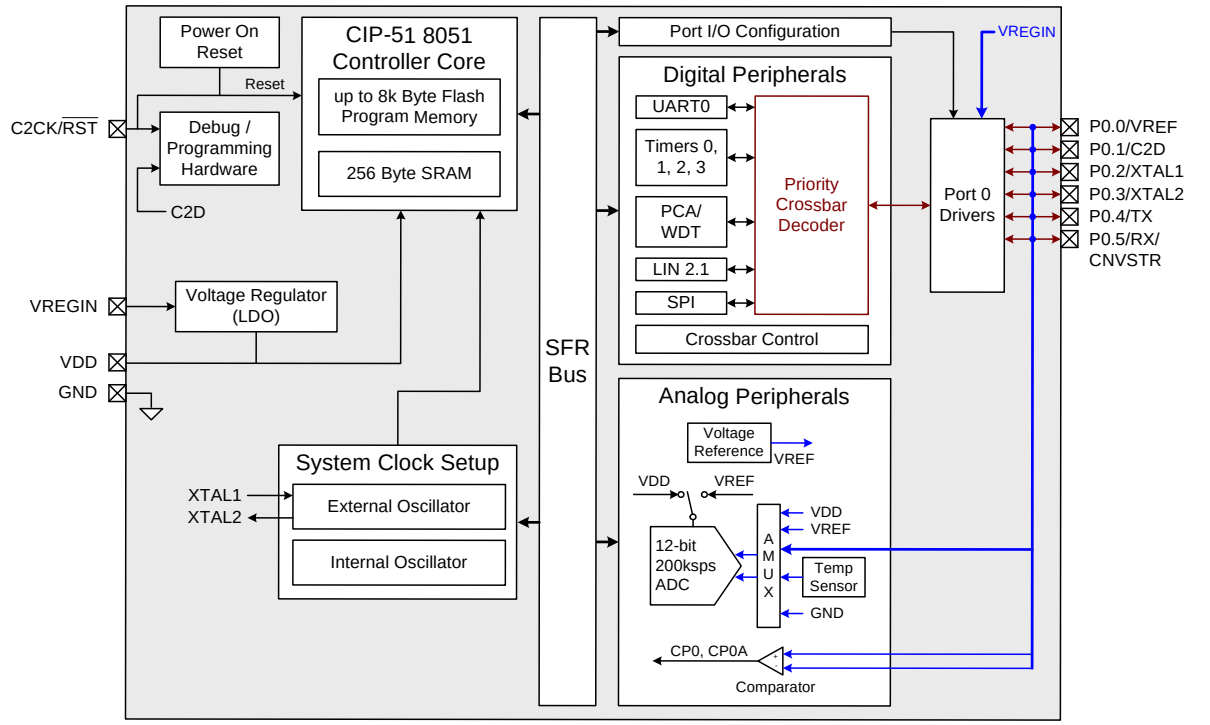

Figure 1.2. C8051F52xA/F52x-C Block Diagram

Table 2.11. Internal Oscillator Electrical Characteristics

V_{DD} = 1.8 to 2.75 V, –40 to +125 °C unless otherwise specified; Using factory-calibrated settings.

Parameter	Conditions	Min	Typ	Max	Units
Oscillator Frequency[1]	IFCN = 111b VDD ≥ VREGMIN[2]	24.5 – 0.5%	24.5[3]	24.5 + 0.5%	MHz
	IFCN = 111b VDD < VREGMIN[2]	24.5 – 1.0%	24.5[3]	24.5 + 1.0%	
Oscillator Supply Current (from V_{DD})	Oscillator On OSCICN[7:6] = 11b	—	800	1100	µA
	Oscillator Suspend OSCICN[7:6] = 00b ZTCEN = 1				
	T = 25 °C	—	67	—	µA
	T = 85 °C	—	77	—	µA
	T = 125 °C	—	117	300	µA
	Oscillator Suspend OSCICN[7:6] = 00b ZTCEN = 0				
	T = 25 °C	—	2	—	µA
	T = 85 °C	—	3	—	µA
	T = 125 °C	—	50	—	µA
Wake-Up Time From Suspend	OSCICN[7:6] = 00b ZTCEN = 0[4]	—	—	1	µs
	OSCICN[7:6] = 00b ZTCEN = 1	—	5	—	Instruction Cycles
Power Supply Sensitivity	Constant Temperature	—	0.10	—	%/V
Temperature Sensitivity[5]	Constant Supply				
	TC_1	—	5.0	—	ppm/°C
	TC_2	—	–0.65	—	ppm/°C^2

Notes:

1. See Section “11.2.1. VDD Monitor Thresholds and Minimum VDD” on page 108 for minimum V_{DD} requirements.
2. VREGMIN is the minimum output of the voltage regulator for its low setting (REG0CN: REG0MD = 0b). See Table 2.6, “Voltage Regulator Electrical Specifications,” on page 30.
3. This is the average frequency across the operating temperature range.
4. See “20.7. Internal Oscillator Suspend Mode” on page 212 for ZTCEN setting in older silicon revisions.
5. Use temperature coefficients TC_1 and TC_2 to calculate the new internal oscillator frequency using the following equation:

$$f(T) = f0 \times (1 + TC_1 \times (T - T0) + TC_2 \times (T - T0)^2)$$

where f0 is the internal oscillator frequency at 25 °C and T0 is 25 °C.

3. Pinout and Package Definitions

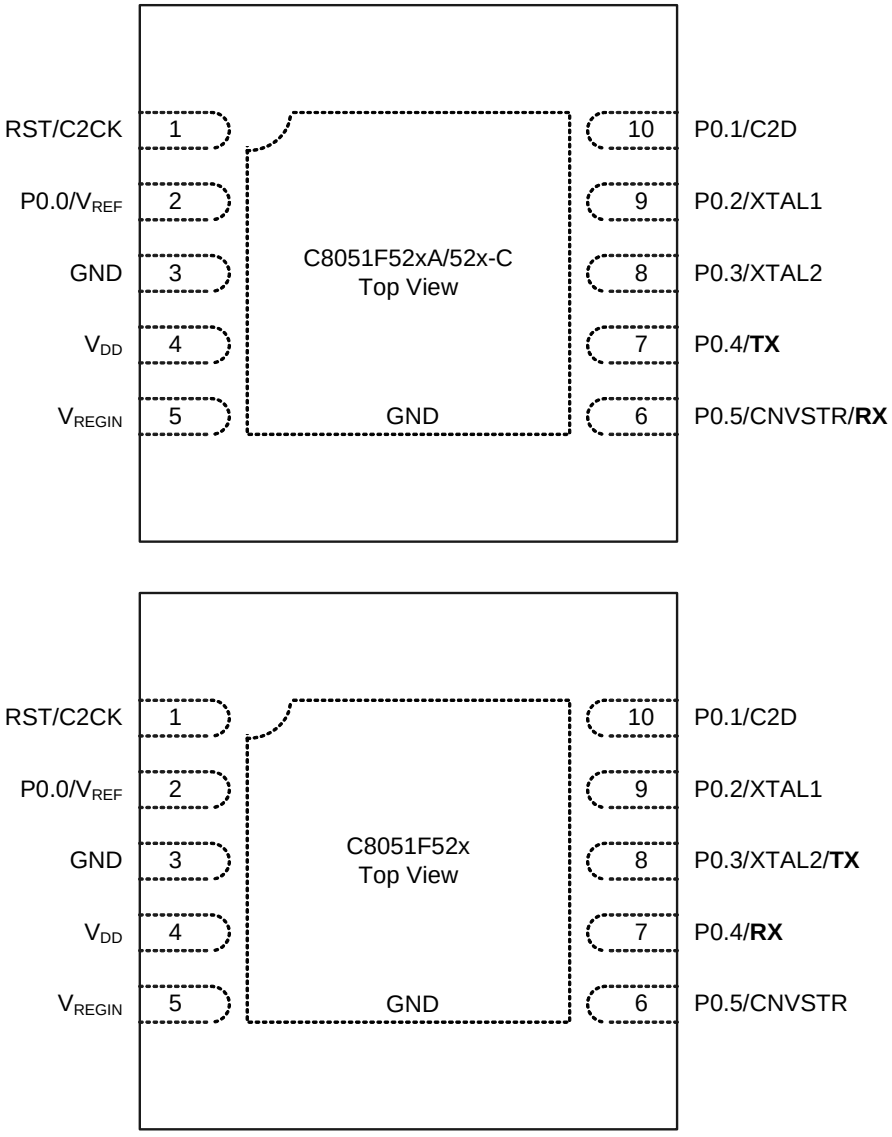

Figure 3.1. DFN-10 Pinout Diagram (Top View)

Table 3.8. QFN-20 Package Diagram Dimensions

Dimension	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D	4.00 BSC.		
D2	2.55	2.70	2.85
e	0.50 BSC.		
E	4.00 BSC.		
E2	2.55	2.70	2.85
L	0.30	0.40	0.50
L1	0.00	—	0.15
aaa	—	—	0.15
bbb	—	—	0.10
ddd	—	—	0.05
eee	—	—	0.08
Z	—	0.43	—
Y	—	0.18	—

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VGGD except for custom features D2, E2, Z, Y, L, and L1, which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

4.2. Temperature Sensor

An on-chip temperature sensor is included on the C8051F52x/F52xA/F53x/F53xA devices which can be directly accessed via the ADC0 multiplexer. To use ADC0 to measure the temperature sensor, the ADC multiplexer channel should be configured to connect to the temperature sensor. The temperature sensor transfer function is shown in Figure 5.2. The output voltage (V_{TEMP}) is the positive ADC input selected by bits AD0MX[4:0] in register ADC0MX. The TEMPE bit in register REF0CN enables/disables the temperature sensor, as described in SFR Definition 5.1. While disabled, the temperature sensor defaults to a high impedance state and any ADC measurements performed on the sensor will result in meaningless data. Refer to Table 5.1 for the slope and offset parameters of the temperature sensor.

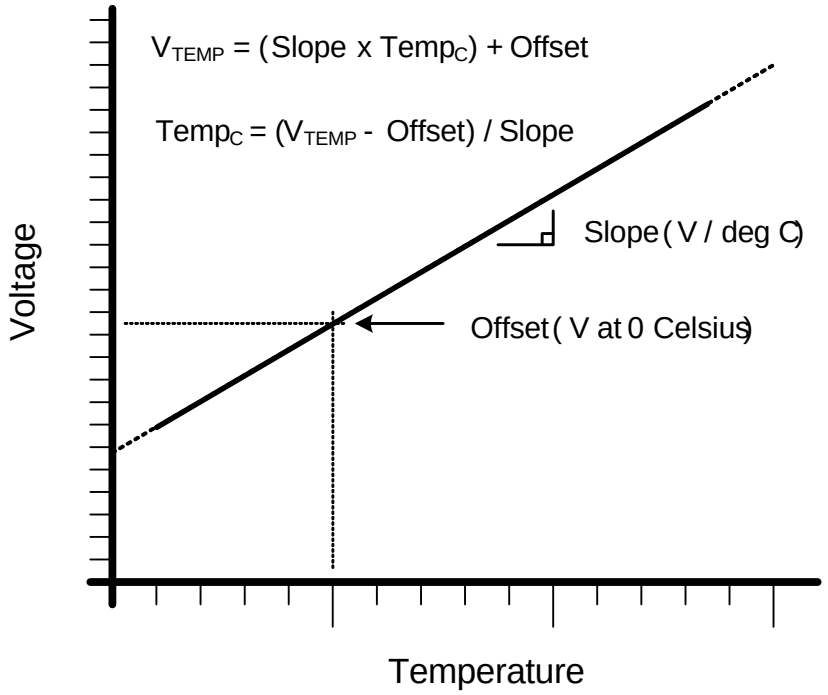

Figure 4.2. Typical Temperature Sensor Transfer Function

SFR Definition 4.6. ADC0H: ADC0 Data Word MSB

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xBE

Bits7–0: ADC0 Data Word High-Order Bits.
For AD0LJST = 0 and AD0RPT as follows:
00: Bits 3–0 are the upper 4 bits of the 12-bit result. Bits 7–4 are 0000b.
01: Bits 4–0 are the upper 5 bits of the 14-bit result. Bits 7–5 are 000b.
10: Bits 5–0 are the upper 6 bits of the 15-bit result. Bits 7–6 are 00b.
11: Bits 7–0 are the upper 8 bits of the 16-bit result.
For AD0LJST = 1 (AD0RPT must be '00'): Bits 7–0 are the most-significant bits of the ADC0 12-bit result.

SFR Definition 4.7. ADC0L: ADC0 Data Word LSB

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xBD

Bits7–0: ADC0 Data Word Low-Order Bits.
For AD0LJST = 0: Bits 7–0 are the lower 8 bits of the ADC0 Accumulated Result.
For AD0LJST = 1 (AD0RPT must be '00'): Bits 7–4 are the lower 4 bits of the 12-bit result. Bits 3–0 are 0000b.

9. Memory Organization and SFRs

The memory organization of the C8051F52x/F52xA/F53x/F53xA is similar to that of a standard 8051. There are two separate memory spaces: program memory and data memory. Program and data memory share the same address space but are accessed via different instruction types. The memory map is shown in Figure 9.1.

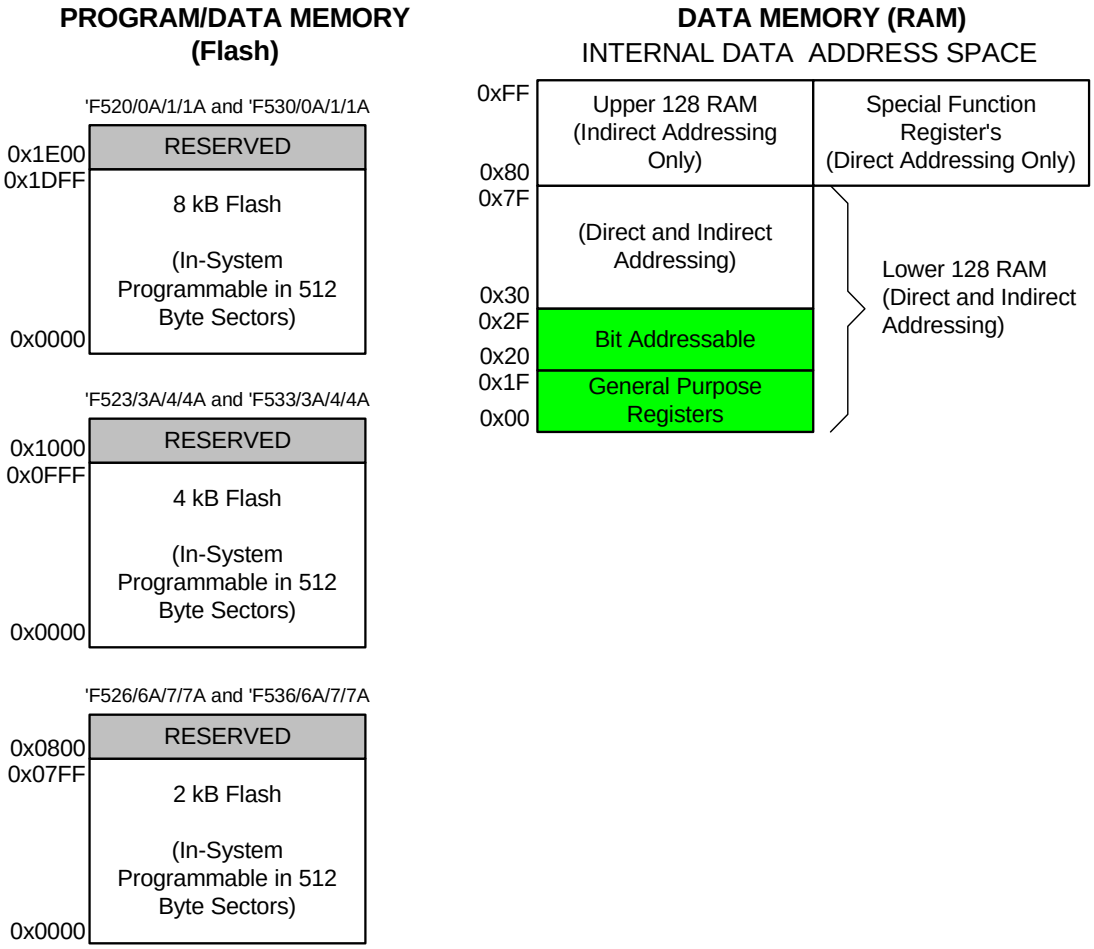

Figure 9.1. Memory Map

9.1. Program Memory

The CIP-51 core has a 64 kB program memory space. The C8051F520/0A/1/1A and C8051F530/0A/1/1A implement 8 kB of this program memory space as in-system, re-programmable Flash memory, organized in a contiguous block from addresses 0x0000 to 0x1FFF. Addresses above 0x1DFF are reserved on the 8 kB devices. The C8051F523/3A/4/4A and C8051F533/3A/4/4A implement 4 kB of Flash from addresses 0x0000 to 0x0FFF. The C8051F526/6A/7/7A and C8051F536/6A/7/7A implement 2 kB of Flash from addresses 0x0000 to 0x07FF.

Program memory is normally assumed to be read-only. However, the C8051F52x/F52xA/F53x/F53xA can write to program memory by setting the Program Store Write Enable bit (PSCTL.0) and using the MOVX write instruction. This feature provides a mechanism for updates to program code and use of the program memory space for non-volatile data storage. Refer to Section “12. Flash Memory” on page 113 for further details.

ramp or during a brownout condition even when V_{DD} is below the specified minimum of 2.0 V. There are two possible ways to handle this transitional period as described below:

If using the on-chip regulator (REG0) at the 2.6 V setting (default), it is recommended that user software set the VDDMON0 threshold to its high setting ($V_{RST-HIGH}$) as soon as possible after reset by setting the VDMLVL bit to 1 in SFR Definition 11.1 (VDDMON). In this typical configuration, no external hardware or additional software routines are necessary to monitor the V_{DD} level.

Note: Please refer to Section “20.5. VDD Monitor (VDDMON0) High Threshold Setting” on page 212 for important notes related to the VDD Monitor high threshold setting in older silicon revisions A and B.

If using the on-chip regulator (REG0) at the 2.1 V setting or if directly driving V_{DD} with REG0 disabled, the user system (software/hardware) should monitor V_{DD} at power-on and also during device operation. The two key parameters that can be affected when V_{DD} < 2.0 V are: internal oscillator frequency (Table 2.11 on page 34) and minimum ADC tracking time (Table 2.3 on page 28).

SFR Definition 11.1. VDDMON: V_{DD} Monitor Control

R/W	R	R/W	R	R	R	R	R	Reset Value
VDMEN	VDDSTAT	VDMLVL	VDM1EN	Reserved	Reserved	Reserved	Reserved	1v010000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xFF

Bit7: **VDMEN**: V_{DD} Monitor Enable (VDDMON0).
This bit turns the V_{DD} monitor circuit on/off. The V_{DD} Monitor cannot generate system resets until it is also selected as a reset source in register RSTSRC (SFR Definition 11.2). The V_{DD} Monitor can be allowed to stabilize before it is selected as a reset source. **Selecting the V_{DD} monitor as a reset source before it has stabilized may generate a system reset.** See Table 2.8 on page 32 for the minimum V_{DD} Monitor turn-on time.
0: V_{DD} Monitor Disabled.
1: V_{DD} Monitor Enabled (default).

Bit6: **VDDSTAT**: V_{DD} Status.
This bit indicates the current power supply status (V_{DD} Monitor output).
0: V_{DD} is at or below the V_{DD} Monitor (VDDMON0) Threshold.
1: V_{DD} is above the V_{DD} Monitor (VDDMON0) Threshold.

Bit5: **VDMLVL**: V_{DD} Level Select.
0: V_{DD} Monitor (VDDMON0) Threshold is set to $V_{RST-LOW}$ (default).
1: V_{DD} Monitor (VDDMON0) Threshold is set to $V_{RST-HIGH}$. This setting is **required** for any system that includes code that writes to and/or erases Flash.

Bit4: **VDM1EN***: Level-sensitive V_{DD} Monitor Enable (VDDMON1).
This bit turns the V_{DD} monitor circuit on/off. If turned on, it is also selected as a reset source, and can generate a system reset.
0: Level-sensitive VDD Monitor Disabled.
1: Level-sensitive VDD Monitor Enabled (default).

Bits3–0: **RESERVED**. Read = Variable. Write = don’t care.

***Note:** Available only on the C8051F52x-C/F53x-C devices

14.3. System Clock Selection

The internal oscillator requires little start-up time and may be selected as the system clock immediately following the OSCICN write that enables the internal oscillator. External crystals and ceramic resonators typically require a start-up time before they are settled and ready for use. The Crystal Valid Flag (XTLVLD in register OSCXCN) is set to 1 by hardware when the external oscillator is settled. **To avoid reading a false XTLVLD in crystal mode, the software should delay at least 1 ms between enabling the external oscillator and checking XTLVLD.** RC and C modes typically require no startup time.

The CLKSL bit in register CLKSEL selects which oscillator source is used as the system clock. CLKSL must be set to 1 for the system clock to run from the external oscillator; however the external oscillator may still clock certain peripherals (timers, PCA) when another oscillator is selected as the system clock. The system clock may be switched on-the-fly between the internal oscillator and external oscillator, as long as the selected clock source is enabled and has settled.

SFR Definition 14.5. CLKSEL: Clock Select

R	R	R/W	R/W	R	R/W	R/W	R/W	Reset Value
-	-	Reserved	Reserved	-	Reserved	Reserved	CLKSL	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
							SFR Address:	0xA9

Bits7–6: Unused. Read = 00b; Write = don't care.
Bits5–4: Reserved. Read = 00b; Must write 00b.
Bit3: Unused. Read = 0b; Write = don't care.
Bits2–1: Reserved. Read = 00b; Must write 00b.
Bit0: **CLKSL**: System Clock Select
0: Internal Oscillator (as determined by the IFCN bits in register OSCICN).
1: External Oscillator.

15.2.2. 9-Bit UART

9-bit UART mode uses a total of eleven bits per data byte: a start bit, 8 data bits (LSB first), a programmable ninth data bit, and a stop bit. The state of the ninth transmit data bit is determined by the value in TB80 (SCON0.3), which is assigned by user software. It can be assigned the value of the parity flag (bit P in register PSW) for error detection, or used in multiprocessor communications. On receive, the ninth data bit goes into RB80 (SCON0.2) and the stop bit is ignored.

Data transmission begins when an instruction writes a data byte to the SBUF0 register. The TI0 Transmit Interrupt Flag (SCON0.1) is set at the end of the transmission (the beginning of the stop-bit time). Data reception can begin any time after the REN0 Receive Enable bit (SCON0.4) is set to 1. After the stop bit is received, the data byte will be loaded into the SBUF0 receive register if the following conditions are met: (1) RI0 must be logic 0, and (2) if MCE0 is logic 1, the 9th bit must be logic 1 (when MCE0 is logic 0, the state of the ninth data bit is unimportant). If these conditions are met, the eight bits of data are stored in SBUF0, the ninth bit is stored in RB80, and the RI0 flag is set to 1. If the above conditions are not met, SBUF0 and RB80 will not be loaded and the RI0 flag will not be set to 1. A UART0 interrupt will occur if enabled when either TI0 or RI0 is set to 1.

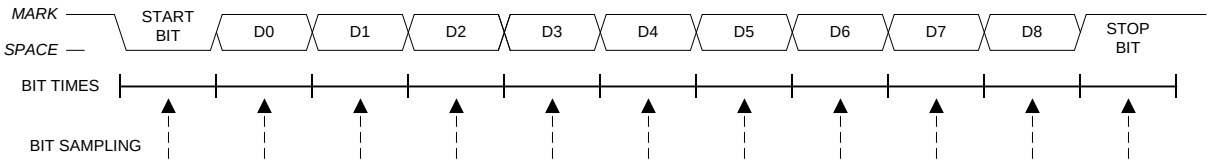

Figure 15.5. 9-Bit UART Timing Diagram

SFR Definition 15.2. SBUF0: Serial (UART0) Port Data Buffer

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x99

Bits7–0: **SBUF0[7:0]**: Serial Data Buffer Bits 7–0 (MSB–LSB)
This SFR accesses two registers; a transmit shift register and a receive latch register. When data is written to SBUF0, it goes to the transmit shift register and is held for serial transmission. Writing a byte to SBUF0 initiates the transmission. A read of SBUF0 returns the contents of the receive latch.

Table 15.1. Timer Settings for Standard Baud Rates Using the Internal Oscillator

	Frequency: 24.5 MHz						
	Target Baud Rate (bps)	**Baud Rate % Error**	**Oscillator Divide Factor**	**Timer Clock Source**	**SCA1–SCA0 (pre-scale select)***	**T1M***	**Timer 1 Reload Value (hex)**
SYSCLK from Internal Osc.	230400	–0.32%	106	SYSCLK	XX	1	0xCB
	115200	–0.32%	212	SYSCLK	XX	1	0x96
	57600	0.15%	426	SYSCLK	XX	1	0x2B
	28800	–0.32%	848	SYSCLK / 4	01	0	0x96
	14400	0.15%	1704	SYSCLK / 12	00	0	0xB9
	9600	–0.32%	2544	SYSCLK / 12	00	0	0x96
	2400	–0.32%	10176	SYSCLK / 48	10	0	0x96
	1200	0.15%	20448	SYSCLK / 48	10	0	0x2B

X = Don't care

Note: SCA1–SCA0 and T1M bit definitions can be found in Section 18.1.

SFR Definition 16.1. SPI0CFG: SPI0 Configuration

R	R/W	R/W	R/W	R	R	R	R	Reset Value
SPIBSY	MSTEN	CKPHA	CKPOL	SLVSEL	NSSIN	SRMT	RXBMT	00000111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xA1

Bit 7: **SPIBSY**: SPI Busy (read only).
This bit is set to logic 1 when a SPI transfer is in progress (Master or Slave Mode).

Bit 6: **MSTEN**: Master Mode Enable.
0: Disable master mode. Operate in slave mode.
1: Enable master mode. Operate as a master.

Bit 5: **CKPHA**: SPI0 Clock Phase.
This bit controls the SPI0 clock phase.
0: Data centered on first edge of SCK period.*
1: Data centered on second edge of SCK period.*

Bit 4: **CKPOL**: SPI0 Clock Polarity.
This bit controls the SPI0 clock polarity.
0: SCK line low in idle state.
1: SCK line high in idle state.

Bit 3: **SLVSEL**: Slave Selected Flag (read only).
This bit is set to logic 1 whenever the NSS pin is low indicating SPI0 is the selected slave. It is cleared to logic 0 when NSS is high (slave not selected). This bit does not indicate the instantaneous value at the NSS pin, but rather a de-glitched version of the pin input.

Bit 2: **NSSIN**: NSS Instantaneous Pin Input (read only).
This bit mimics the instantaneous value that is present on the NSS port pin at the time that the register is read. This input is not de-glitched.

Bit 1: **SRMT**: Shift Register Empty (Valid in Slave Mode, read only).
This bit will be set to logic 1 when all data has been transferred in/out of the shift register, and there is no new information available to read from the transmit buffer or write to the receive buffer. It returns to logic 0 when a data byte is transferred to the shift register from the transmit buffer or by a transition on SCK.
NOTE: SRMT = 1 when in Master Mode.

Bit 0: **RXBMT**: Receive Buffer Empty (Valid in Slave Mode, read only).
This bit will be set to logic 1 when the receive buffer has been read and contains no new information. If there is new information available in the receive buffer that has not been read, this bit will return to logic 0.
NOTE: RXBMT = 1 when in Master Mode.

Note: See Table 16.1 for timing parameters.

SFR Definition 16.3. SPI0CKR: SPI0 Clock Rate

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
SCR7	SCR6	SCR5	SCR4	SCR3	SCR2	SCR1	SCR0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xA2

Bits7–0: **SCR7–SCR0**: SPI0 Clock Rate.
These bits determine the frequency of the SCK output when the SPI0 module is configured for master mode operation. The SCK clock frequency is a divided version of the system clock, and is given in the following equation, where *SYSCLK* is the system clock frequency and *SPI0CKR* is the 8-bit value held in the SPI0CKR register.

$$f_{SCK} = \frac{SYSCLK}{2 \times (SPI0CKR + 1)}$$

for 0 <= SPI0CKR <= 255

Example: If SYSCLK = 2 MHz and SPI0CKR = 0x04,

$$f_{SCK} = \frac{2000000}{2 \times (4 + 1)}$$

$$f_{SCK} = 200kHz$$

in progress. The same applies to changes in the LIN interface mode from slave mode to master mode and from master mode to slave mode.

17.5. Sleep Mode and Wake-Up

To reduce the system's power consumption, the LIN Protocol Specification defines a Sleep Mode. The message used to broadcast a Sleep Mode request must be transmitted by the LIN master application in the same way as a normal transmit message. The LIN slave application must decode the Sleep Mode Frame from the Identifier and data bytes. After that, the LIN slave node must be put into the Sleep Mode by setting the SLEEP bit (LIN0CTRL.6).

If the SLEEP bit (LIN0CTRL.6) of the LIN slave application is not set and there is no bus activity for four seconds (specified bus idle timeout), the IDLTOUT bit (LIN0ST.6) is set and an interrupt request is generated. After that the application may assume that the LIN bus is in Sleep Mode and set the SLEEP bit (LIN0CTRL.6).

Sending a Wakeup signal from the master or any slave node terminates the Sleep Mode of the LIN bus. To send a Wakeup signal, the application has to set the WUPREQ bit (LIN0CTRL.1). After successful transmission of the wakeup signal, the DONE bit (LIN0ST.0) of the master node is set and an interrupt request is generated. The LIN slave does not generate an interrupt request after successful transmission of the Wakeup signal but it generates an interrupt request if the master does not respond to the Wakeup signal within 150 milliseconds. In that case, the ERROR bit (LIN0ST.2) and TOUT bit (LIN0ERR.2) are set. The application then has to decide whether or not to transmit another Wakeup signal.

All LIN nodes that detect a wakeup signal will set the WAKEUP (LIN0ST.1) and DONE bits (LIN0ST.0) and generate an interrupt request. After that, the application has to clear the SLEEP bit (LIN0CTRL.6) in the LIN slave.

17.6. Error Detection and Handling

The LIN peripheral generates an interrupt request and stops the processing of the current frame if it detects an error. The application has to check the type of error by processing LIN0ERR. After that, it has to reset the error register and the ERROR bit (LIN0ST.2) by writing a 1 to the RSTERR bit (LIN0CTRL.2). Starting a new message with the LIN peripheral selected as master or sending a Wakeup signal with the LIN peripheral selected as a master or slave is possible only if ERROR bit (LIN0ST.2) is set to 0.

17.7.2. LIN Indirect Access SFR Registers Definition

Table 17.4. LIN Registers* (Indirectly Addressable)

Name	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LIN0DT1	0x00	DATA1[7:0]							
LIN0DT2	0x01	DATA2[7:0]							
LIN0DT3	0x02	DATA3[7:0]							
LIN0DT4	0x03	DATA4[7:0]							
LIN0DT5	0x04	DATA5[7:0]							
LIN0DT6	0x05	DATA6[7:0]							
LIN0DT7	0x06	DATA7[7:0]							
LIN0DT8	0x07	DATA8[7:0]							
LIN0CTRL	0x08	STOP(s)	SLEEP(s)	TXRX	DTACK(s)	RSTINT	RSTERR	WUPREQ	STREQ(m)
LIN0ST	0x09	ACTIVE	IDLTOUT	ABORT(s)	DTREQ(s)	LININT	ERROR	WAKEUP	DONE
LIN0ERR	0x0A				SYNCH(s)	PRTY(s)	TOUT	CHK	BITERR
LIN0SIZE	0x0B	ENHCHK				LINSIZE[3:0]			
LIN0DIV	0x0C	DIVLSB[7:0]							
LIN0MUL	0x0D	PRESCL[1:0]		LINMUL[4:0]					DIV9
LIN0ID	0x0E			ID[5:0]					

*These registers are used in both master and slave mode. The register bits marked with (m) are accessible only in Master mode while the register bits marked with (s) are accessible only in slave mode. All other registers are accessible in both modes.

SFR Definition 17.4. LIN0DT1: LIN0 Data Byte 1

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Address: 0x00 (indirect)

Bit7–0: **LIN0DT1**: LIN Data Byte 1.
Serial Data Byte 1 that is received or transmitted across the LIN interface.

19.2.1. Edge-triggered Capture Mode

In this mode, a valid transition on the CEXn pin causes the PCA to capture the value of the PCA counter/timer and load it into the corresponding module's 16-bit capture/compare register (PCA0CPLn and PCA0CPHn). The CAPPn and CAPNn bits in the PCA0CPMn register are used to select the type of transition that triggers the capture: low-to-high transition (positive edge), high-to-low transition (negative edge), or either transition (positive or negative edge). When a capture occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1 and an interrupt request is generated if CCF interrupts are enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. If both CAPPn and CAPNn bits are set to logic 1, then the state of the Port pin associated with CEXn can be read directly to determine whether a rising-edge or falling-edge caused the capture.

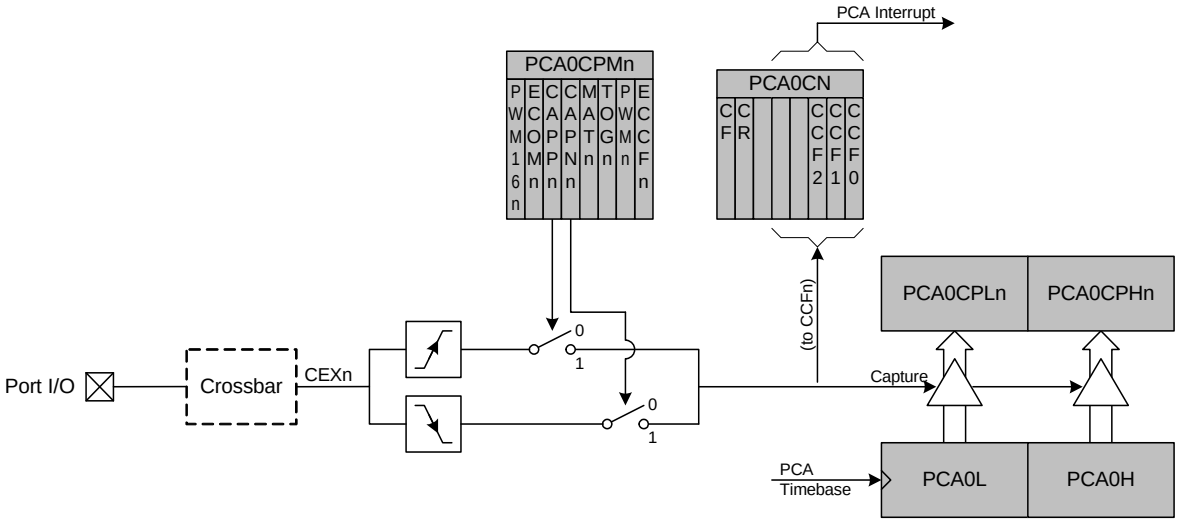

Figure 19.4. PCA Capture Mode Diagram

Note: The CEXn input signal must remain high or low for at least 2 system clock cycles to be recognized by the hardware.

SFR Definition 19.3. PCA0CPMn: PCA Capture/Compare Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
PWM16n	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: PCA0CPM0: 0xDA, PCA0CPM1: 0xDB, PCA0CPM2: 0xDC

Bit7: **PWM16n**: 16-bit Pulse Width Modulation Enable.
This bit selects 16-bit mode when Pulse Width Modulation mode is enabled (PWMn = 1).
0: 8-bit PWM selected.
1: 16-bit PWM selected.

Bit6: **ECOMn**: Comparator Function Enable.
This bit enables/disables the comparator function for PCA module n.
0: Disabled.
1: Enabled.

Bit5: **CAPPn**: Capture Positive Function Enable.
This bit enables/disables the positive edge capture for PCA module n.
0: Disabled.
1: Enabled.

Bit4: **CAPNn**: Capture Negative Function Enable.
This bit enables/disables the negative edge capture for PCA module n.
0: Disabled.
1: Enabled.

Bit3: **MATn**: Match Function Enable.
This bit enables/disables the match function for PCA module n. When enabled, matches of the PCA counter with a module's capture/compare register cause the CCFn bit in PCA0MD register to be set to logic 1.
0: Disabled.
1: Enabled.

Bit2: **TOGn**: Toggle Function Enable.
This bit enables/disables the toggle function for PCA module n. When enabled, matches of the PCA counter with a module's capture/compare register cause the logic level on the CEXn pin to toggle. If the PWMn bit is also set to logic 1, the module operates in Frequency Output Mode.
0: Disabled.
1: Enabled.

Bit1: **PWMn**: Pulse Width Modulation Mode Enable.
This bit enables/disables the PWM function for PCA module n. When enabled, a pulse width modulated signal is output on the CEXn pin. 8-bit PWM is used if PWM16n is cleared; 16-bit mode is used if PWM16n is set to logic 1. If the TOGn bit is also set, the module operates in Frequency Output Mode.
0: Disabled.
1: Enabled.

Bit0: **ECCFn**: Capture/Compare Flag Interrupt Enable.
This bit sets the masking of the Capture/Compare Flag (CCFn) interrupt.
0: Disable CCFn interrupts.
1: Enable a Capture/Compare Flag interrupt request when CCFn is set.