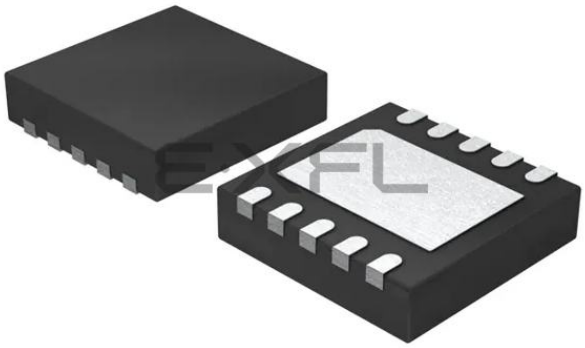

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Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	6
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.25V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	10-VFDFN Exposed Pad
Supplier Device Package	10-DFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f524-c-imr

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Table 2.4. Temperature Sensor Electrical Characteristics

V_{DD} = 2.1 V, V_{REF} = 1.5 V (REFSL=0), –40 to +125 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Linearity[1]		—	0.1	—	°C
Gain[1]		—	3.33	—	mV/°C
Gain Error[2]		—	±100	—	µV/°C
Offset[1]	Temp = 0 °C	—	890	—	mV
Offset Error[2]	Temp = 0 °C	—	±15	—	mV
Tracking Time		12	—	—	µs
Power Supply Current		—	17	—	µA

Notes:
1. Includes ADC offset, gain, and linearity variations.
2. Represents one standard deviation from the mean.

Table 2.5. Voltage Reference Electrical Characteristics

V_{DD} = 2.1 V; –40 to +125 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Internal Reference (REFBE = 1)					
Output Voltage	I_{DD} ≈ 1 mA; No load on VREF pin and all other GPIO pins. 25 °C ambient (REFLV = 0) 25 °C ambient (REFLV = 1), V_{DD} = 2.6 V	 1.45 2.15	 1.5 2.2	 1.55 2.25	 V
V_{REF} Short-Circuit Current		—	2.5	—	mA
V_{REF} Temperature Coefficient		—	33	—	ppm/°C
Load Regulation	Load = 0 to 200 µA to GND	—	10	—	ppm/µA
V_{REF} Turn-on Time 1	4.7 µF, 0.1 µF bypass	—	21	—	ms
V_{REF} Turn-on Time 2	0.1 µF bypass	—	230	—	µs
Power Supply Rejection		—	2.1	—	mV/V
External Reference (REFBE = 0)					
Input Voltage Range		0	—	V_{DD}	V
Input Current	Sample Rate = 200 ksps; V_{REF} = 1.5 V	—	2.4	—	µA
Bias Generators					
ADC Bias Generator	BIASE = 1	—	22	—	µA
Power Consumption (Internal)		—	35	—	µA

4.3.4. Burst Mode

Burst Mode is a power saving feature that allows ADC0 to remain in a very low power state between conversions. When Burst Mode is enabled, ADC0 wakes from a very low power state, accumulates 1, 4, 8, or 16 samples using an internal Burst Mode Oscillator, then re-enters a very low power state. Since the Burst Mode clock is independent of the system clock, ADC0 can perform multiple conversions then enter a very low power state within a single system clock cycle, even if the system clock is slow (e.g. 32.768 kHz), or suspended.

Burst Mode is enabled by setting BURSTEN to logic 1. When in Burst Mode, AD0EN controls the ADC0 idle power state (i.e., the state ADC0 enters when not tracking or performing conversions). If AD0EN is set to logic 0, ADC0 is powered down after each burst. If AD0EN is set to logic 1, ADC0 remains enabled after each burst. On each convert start signal, ADC0 is awakened from its Idle Power State. If ADC0 is powered down, it will automatically power up and wait the programmable Power-Up Time controlled by the AD0PWR bits. Otherwise, ADC0 will start tracking and converting immediately. Figure 4.5 shows an example of Burst Mode Operation with a slow system clock and a repeat count of 4.

Important Note: When Burst Mode is enabled, only Post-Tracking and Dual-Tracking modes can be used.

When Burst Mode is enabled, a single convert start will initiate a number of conversions equal to the repeat count. When Burst Mode is disabled, a convert start is required to initiate each conversion. In both modes, the ADC0 End of Conversion Interrupt Flag (AD0INT) will be set after “repeat count” conversions have been accumulated. Similarly, the Window Comparator will not compare the result to the greater-than and less-than registers until “repeat count” conversions have been accumulated.

Note: When using Burst Mode, care must be taken to issue a convert start signal no faster than once every four SYSCLK periods. This includes external convert start signals.

Gain Register Definition 4.1. ADC0GNH: ADC0 Selectable Gain High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
GAINH[7:0]								11111100
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Address:
								0x04

Bits7–0: High byte of Selectable Gain Word.

Gain Register Definition 4.2. ADC0GNL: ADC0 Selectable Gain Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
GAINL[3:0]				Reserved	Reserved	Reserved	Reserved	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Address:
								0x07

Bits7–4: Lower 4 bits of the Selectable Gain Word.
Bits3–0: **Reserved**. Must Write 0000b.

Gain Register Definition 4.3. ADC0GNA: ADC0 Additional Selectable Gain

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	GAINADD	00000001
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Address:
								0x08

Bits7–1: **Reserved**. Must Write 0000000b.
Bit0: **GAINADD**: Additional Gain Bit.
Setting this bit adds 1/64 (0.016) gain to the gain value in the ADC0GNH and ADC0GNL registers.

SFR Definition 4.9. ADC0TK: ADC0 Tracking Mode Select

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
AD0PWR				AD0TM		AD0TK		11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
							(bit addressable)	0xBA

Bits7–4: **AD0PWR3–0**: ADC0 Burst Power-Up Time.
For BURSTEN = 0:
ADC0 power state controlled by AD0EN.
For BURSTEN = 1 and AD0EN = 1;
ADC0 remains enabled and does not enter the very low power state.
For BURSTEN = 1 and AD0EN = 0:
ADC0 enters the very low power state as specified in Table 2.3 on page 28 and is enabled after each convert start signal. The Power Up time is programmed according to the following equation:

$$AD0PWR = \frac{Tstartup}{200ns} - 1 \quad \text{or} \quad Tstartup = (AD0PWR + 1)200ns$$

Bits3–2: **AD0TM1–0**: ADC0 Tracking Mode Select Bits.
00: Reserved.
01: ADC0 is configured to Post-Tracking Mode.
10: ADC0 is configured to Pre-Tracking Mode.
11: ADC0 is configured to Dual-Tracking Mode (default).

Bits1–0: **AD0TK1–0**: ADC0 Post-Track Time.
Post-Tracking time is controlled by AD0TK as follows:
00: Post-Tracking time is equal to 2 SAR clock cycles + 2 FCLK cycles.
01: Post-Tracking time is equal to 4 SAR clock cycles + 2 FCLK cycles.
10: Post-Tracking time is equal to 8 SAR clock cycles + 2 FCLK cycles.
11: Post-Tracking time is equal to 16 SAR clock cycles + 2 FCLK cycles.

Table 8.1. CIP-51 Instruction Set Summary (Continued)

Mnemonic	Description	Bytes	Clock Cycles
ORL direct, #data	OR immediate to direct byte	3	3
XRL A, Rn	Exclusive-OR Register to A	1	1
XRL A, direct	Exclusive-OR direct byte to A	2	2
XRL A, @Ri	Exclusive-OR indirect RAM to A	1	2
XRL A, #data	Exclusive-OR immediate to A	2	2
XRL direct, A	Exclusive-OR A to direct byte	2	2
XRL direct, #data	Exclusive-OR immediate to direct byte	3	3
CLR A	Clear A	1	1
CPL A	Complement A	1	2
RL A	Rotate A left	1	1
RLC A	Rotate A left through Carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through Carry	1	1
SWAP A	Swap nibbles of A	1	1
Data Transfer			
MOV A, Rn	Move Register to A	1	1
MOV A, direct	Move direct byte to A	2	2
MOV A, @Ri	Move indirect RAM to A	1	2
MOV A, #data	Move immediate to A	2	2
MOV Rn, A	Move A to Register	1	1
MOV Rn, direct	Move direct byte to Register	2	2
MOV Rn, #data	Move immediate to Register	2	2
MOV direct, A	Move A to direct byte	2	2
MOV direct, Rn	Move Register to direct byte	2	2
MOV direct, direct	Move direct byte to direct byte	3	3
MOV direct, @Ri	Move indirect RAM to direct byte	2	2
MOV direct, #data	Move immediate to direct byte	3	3
MOV @Ri, A	Move A to indirect RAM	1	2
MOV @Ri, direct	Move direct byte to indirect RAM	2	2
MOV @Ri, #data	Move immediate to indirect RAM	2	2
MOV DPTR, #data16	Load DPTR with 16-bit constant	3	3
MOVC A, @A+DPTR	Move code byte relative DPTR to A	1	3
MOVC A, @A+PC	Move code byte relative PC to A	1	3
MOVX A, @Ri	Move external data (8-bit address) to A	1	3
MOVX @Ri, A	Move A to external data (8-bit address)	1	3
MOVX A, @DPTR	Move external data (16-bit address) to A	1	3
MOVX @DPTR, A	Move A to external data (16-bit address)	1	3
PUSH direct	Push direct byte onto stack	2	2
POP direct	Pop direct byte from stack	2	2
XCH A, Rn	Exchange Register with A	1	1
XCH A, direct	Exchange direct byte with A	2	2
XCH A, @Ri	Exchange indirect RAM with A	1	2
XCHD A, @Ri	Exchange low nibble of indirect RAM with A	1	2

9.2. Data Memory

The C8051F52x/F52xA/F53x/F53xAincludes 256 bytes of internal RAM mapped into the data memory space from 0x00 through 0xFF. The lower 128 bytes of data memory are used for general purpose registers and scratch pad memory. Either direct or indirect addressing may be used to access the lower 128 bytes of data memory. Locations 0x00 through 0x1F are addressable as four banks of general purpose registers, each bank consisting of eight byte-wide registers. The next 16 bytes, locations 0x20 through 0x2F, may either be addressed as bytes or as 128 bit locations accessible with the direct addressing mode.

The upper 128 bytes of data memory are accessible only by indirect addressing. This region occupies the same address space as the Special Function Registers (SFRs) but is physically separate from the SFR space. The addressing mode used by an instruction when accessing locations above 0x7F determines whether the CPU accesses the upper 128 bytes of data memory space or the SFRs. Instructions that use direct addressing will access the SFR space. Instructions using indirect addressing above 0x7F access the upper 128 bytes of data memory. Figure 9.1 illustrates the data memory organization of the C8051F52x/F52xA/F53x/F53xA.

9.3. General Purpose Registers

The lower 32 bytes of data memory (locations 0x00 through 0x1F) may be addressed as four banks of general-purpose registers. Each bank consists of eight byte-wide registers designated R0 through R7. Only one of these banks may be enabled at a time. Two bits in the program status word, RS0 (PSW.3) and RS1 (PSW.4), select the active register bank (see description of the PSW in SFR Definition 8.4. PSW: Program Status Word). This allows fast context switching when entering subroutines and interrupt service routines. Indirect addressing modes use registers R0 and R1 as index registers.

9.4. Bit Addressable Locations

In addition to direct access to data memory organized as bytes, the sixteen data memory locations at 0x20 through 0x2F are also accessible as 128 individually addressable bits. Each bit has a bit address from 0x00 to 0x7F. Bit 0 of the byte at 0x20 has bit address 0x00 while bit 7 of the byte at 0x20 has bit address 0x07. Bit 7 of the byte at 0x2F has bit address 0x7F. A bit access is distinguished from a full byte access by the type of instruction used (bit source or destination operands as opposed to a byte source or destination).

The MCS-51™ assembly language allows an alternate notation for bit addressing of the form XX.B where XX is the byte address and B is the bit position within the byte. For example, the instruction:

```
MOV    C, 22.3h
```

moves the Boolean value at 0x13 (bit 3 of the byte at location 0x22) into the Carry flag.

9.5. Stack

A programmer's stack can be located anywhere in the 256-byte data memory. The stack area is designated using the Stack Pointer (SP, 0x81) SFR. The SP will point to the last location used. The next value pushed on the stack is placed at SP+1 and then SP is incremented. A reset initializes the stack pointer to location 0x07. Therefore, the first value pushed on the stack is placed at location 0x08, which is also the first register (R0) of register bank 1. Thus, if more than one register bank is to be used, the SP should be initialized to a location in the data memory not being used for data storage. The stack depth can extend up to 256 bytes.

9.6. Special Function Registers

The direct-access data memory locations from 0x80 to 0xFF constitute the special function registers (SFRs). The SFRs provide control and data exchange with the CIP-51's resources and peripherals. The CIP-51 duplicates the SFRs found in a typical 8051 implementation as well as implementing additional

Table 9.2. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Description	Page
OSCICN	0xB2	Internal Oscillator Control	137
OSCXCN	0xB1	External Oscillator Control	142
P0	0x80	Port 0 Latch	129
P0MASK	0xC7	Port 0 Mask	131
P0MAT	0xD7	Port 0 Match	131
P0MDIN	0xF1	Port 0 Input Mode Configuration	129
P0MDOUT	0xA4	Port 0 Output Mode Configuration	130
P0SKIP	0xD4	Port 0 Skip	130
P1	0x90	Port 1 Latch	132
P1MASK	0xBF	Port 1 Mask	134
P1MAT	0xCF	Port 1 Match	134
P1MDIN	0xF2	Port 1 Input Mode Configuration	132
P1MDOUT	0xA5	Port 1 Output Mode Configuration	133
P1SKIP	0xD5	Port 1 Skip	133
PCA0CN	0xD8	PCA Control	206
PCA0CPH0	0xFC	PCA Capture 0 High	209
PCA0CPH1	0xEA	PCA Capture 1 High	209
PCA0CPH2	0xEC	PCA Capture 2 High	209
PCA0CPL0	0xFB	PCA Capture 0 Low	209
PCA0CPL1	0xE9	PCA Capture 1 Low	209
PCA0CPL2	0xEB	PCA Capture 2 Low	209
PCA0CPM0	0xDA	PCA Module 0 Mode	208
PCA0CPM1	0xDB	PCA Module 1 Mode	208
PCA0CPM2	0xDC	PCA Module 2 Mode	208
PCA0H	0xFA	PCA Counter High	209
PCA0L	0xF9	PCA Counter Low	209
PCA0MD	0xD9	PCA Mode	207
PCON	0x87	Power Control	91
PSCTL	0x8F	Program Store R/W Control	119
PSW	0xD0	Program Status Word	88

10.5. External Interrupts

The $\overline{INT0}$ and $\overline{INT0}$ external interrupt sources are configurable as active high or low, edge or level sensitive. The IN0PL ($\overline{INT0}$ Polarity) and IN1PL ($\overline{INT0}$ Polarity) bits in the IT01CF register select active high or active low; the IT0 and IT1 bits in TCON (Section “18.1. Timer 0 and Timer 1” on page 182) select level or edge sensitive. The table below lists the possible configurations.

IT0	IN0PL	$\overline{INT0}$ Interrupt
1	0	Active low, edge sensitive
1	1	Active high, edge sensitive
0	0	Active low, level sensitive
0	1	Active high, level sensitive

IT1	IN1PL	$\overline{INT1}$ Interrupt
1	0	Active low, edge sensitive
1	1	Active high, edge sensitive
0	0	Active low, level sensitive
0	1	Active high, level sensitive

$\overline{INT0}$ and $\overline{INT0}$ are assigned to Port pins as defined in the IT01CF register (see SFR Definition 10.5). Note that $\overline{INT0}$ and $\overline{INT0}$ Port pin assignments are independent of any Crossbar assignments. $\overline{INT0}$ and $\overline{INT0}$ will monitor their assigned Port pins without disturbing the peripheral that was assigned the Port pin via the Crossbar. To assign a Port pin only to $\overline{INT0}$ and/or $\overline{INT0}$, configure the Crossbar to skip the selected pin(s). This is accomplished by setting the associated bit in register XBR0 (see Section “13.1. Priority Crossbar Decoder” on page 122 for complete details on configuring the Crossbar).

In the typical configuration, the external interrupt pins should be skipped in the crossbar and configured as open-drain with the pin latch set to 1. See Section “13. Port Input/Output” on page 120 for more information.

IE0 (TCON.1) and IE1 (TCON.3) serve as the interrupt-pending flags for the $\overline{INT0}$ and $\overline{INT0}$ external interrupts, respectively. If an $\overline{INT0}$ or $\overline{INT0}$ external interrupt is configured as edge-sensitive, the corresponding interrupt-pending flag is automatically cleared by the hardware when the CPU vectors to the ISR. When configured as level sensitive, the interrupt-pending flag remains logic 1 while the input is active as defined by the corresponding polarity bit (IN0PL or IN1PL); the flag remains logic 0 while the input is inactive. The external interrupt source must hold the input active until the interrupt request is recognized. It must then deactivate the interrupt request before execution of the ISR completes or another interrupt request will be generated.

14.1.1. Internal Oscillator Suspend Mode

When software writes a logic 1 to SUSPEND (OSCICN.5), the internal oscillator is suspended. If the system clock is derived from the internal oscillator, the input clock to the peripheral or CIP-51 will be stopped until one of the following events occur:

- Port 0 Match Event.
- Port 1 Match Event.
- Comparator 0 enabled and output is logic 0.

When one of the internal oscillator awakening events occur, the internal oscillator, CIP-51, and affected peripherals resume normal operation, regardless of whether the event also causes an interrupt. The CPU resumes execution at the instruction following the write to SUSPEND.

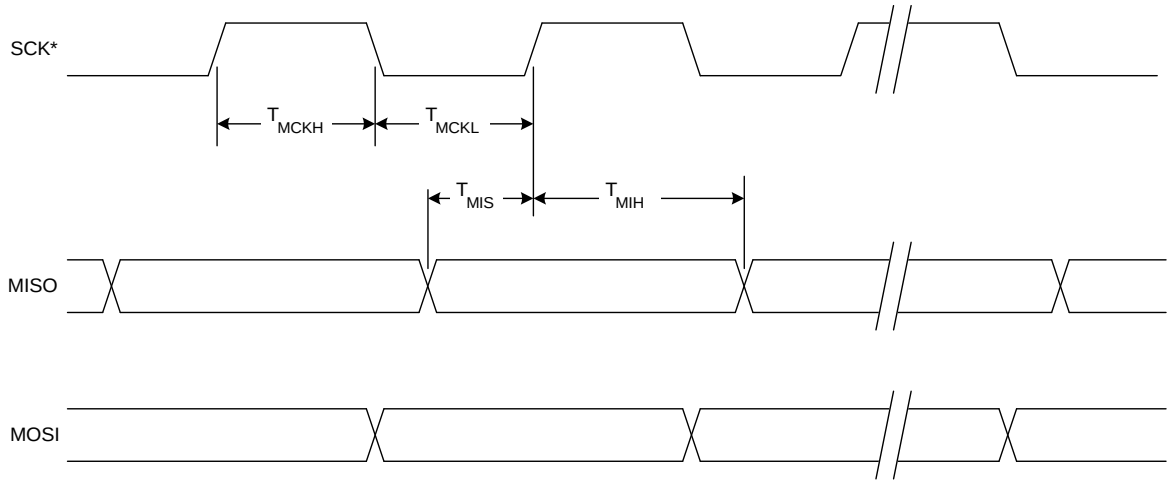
Note: Please refer to Section “20.7. Internal Oscillator Suspend Mode” on page 212 for a note about suspend mode in older silicon revisions.

SFR Definition 16.4. SPI0DAT: SPI0 Data

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

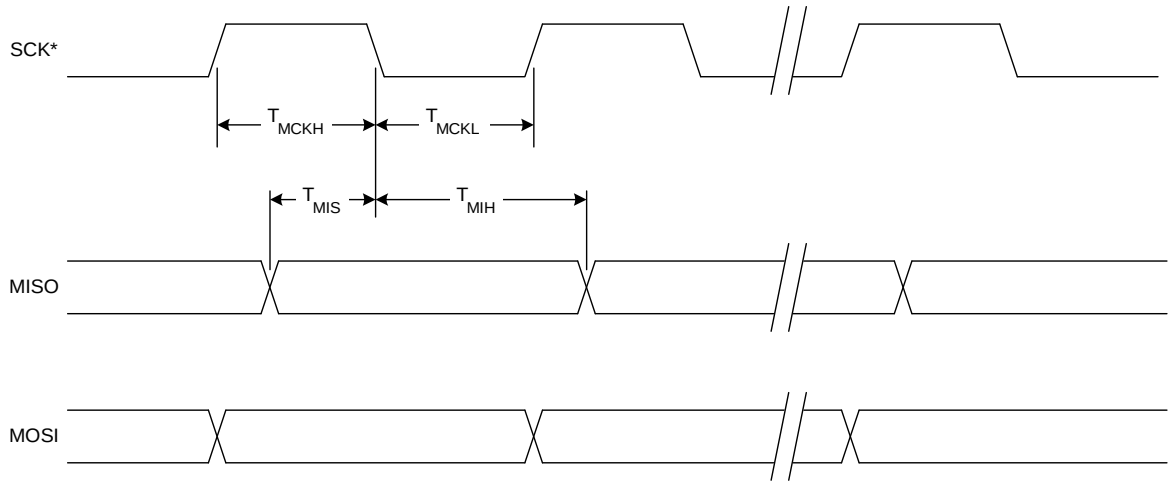
SFR Address: 0xA3

Bits7–0: **SPI0DAT**: SPI0 Transmit and Receive Data.
The SPI0DAT register is used to transmit and receive SPI0 data. Writing data to SPI0DAT places the data into the transmit buffer and initiates a transfer when in Master Mode. A read of SPI0DAT returns the contents of the receive buffer.



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 16.6. SPI Master Timing (CKPHA = 0)



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 16.7. SPI Master Timing (CKPHA = 1)

The following code programs the interface in Master mode, using the Enhanced Checksum and enables the interface to operate at 19200 bits/sec using a 24 MHz system clock.

```
LIN0CF     = 0x80;// Activate the interface
LIN0CF    |= 0x40;// Set the node as a Master

LINADDR   = 0x0D;// Point to the LIN0MUL register
// Initialize the register (prescaler, multiplier and bit 8 of divider)
LINDATA   = ( 0x01 << 6 ) + ( 0x00 << 1 ) + ( ( 0x13F & 0x0100 ) >> 8 );
LINADDR   = 0x0C;// Point to the LIN0DIV register
LINDATA   = (unsigned char)_0x13F;// Initialize LIN0DIV

LINADDR   = 0x0B;// Point to the LIN0SIZE register
LINDATA  |= 0x80;// Initialize the checksum as Enhanced

LINADDR   = 0x08;// Point to LIN0CTRL register
LINDATA   = 0x0C;// Reset any error and the interrupt
```

Table 17.2 includes the configuration values required for the typical system clocks and baud rates:

Table 17.2. Manual Baud Rate Parameters Examples

	Baud (bits / sec)														
	20 K			19.2 K			9.6 K			4.8 K			1 K		
SYSCLK (MHz)	Mult.	Pres.	Div.	Mult.	Pres.	Div.	Mult.	Pres.	Div.	Mult.	Pres.	Div.	Mult.	Pres.	Div.
25	0	1	312	0	1	325	1	1	325	3	1	325	19	1	312
24.5	0	1	306	0	1	319	1	1	319	3	1	319	19	1	306
24	0	1	300	0	1	312	1	1	312	3	1	312	19	1	300
22.1184	0	1	276	0	1	288	1	1	288	3	1	288	19	1	276
16	0	1	200	0	1	208	1	1	208	3	1	208	19	1	200
12.25	0	0	306	0	0	319	1	0	319	3	0	319	19	0	306
12	0	0	300	0	0	312	1	0	312	3	0	312	19	0	300
11.0592	0	0	276	0	0	288	1	0	288	3	0	288	19	0	276
8	0	0	200	0	0	208	1	0	208	3	0	208	19	0	200

SFR Definition 17.17. LIN0MUL: LIN0 Multiplier Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
PRESCL[1:0]		LINMUL[4:0]					DIV9	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Address: 0x0D (indirect)

Bit7–6: **PRESCL1–0**: LIN Baud Rate Prescaler Bits.
These bits are the baud rate prescaler bits.

Bit5–1: **LINMUL4–0**: LIN Baud Rate Multiplier Bits.
These bits are the baud rate multiplier bits. These bits are not used in slave mode.

Bit0: **DIV9**: LIN Baud Rate Divider Most Significant Bit.
The most significant bit of the baud rate divider. The 8 least significant bits are in LIN0DIV.
The valid range for the divider is 200 to 511.

SFR Definition 17.18. LIN0ID: LIN0 ID Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
		ID[5:0]						00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Address: 0x0E (indirect)

Bit7–6: **UNUSED**. Read = 00b. Write = don't care.

Bit5–0: **ID5–0**: LIN Identifier Bits.
These bits form the data identifier.

If the LINSIZE bits (LIN0SIZE[3:0]) are 1111b, bits ID[5:4] are used to determine the data size and are interpreted as follows:
00: 2 bytes
01: 2 bytes
10: 4 bytes
11: 8 bytes

SFR Definition 18.1. TCON: Timer Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable
							SFR Address:	0x88

Bit7: **TF1**: Timer 1 Overflow Flag.
Set by hardware when Timer 1 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 1 interrupt service routine.
0: No Timer 1 overflow detected.
1: Timer 1 has overflowed.

Bit6: **TR1**: Timer 1 Run Control.
0: Timer 1 disabled.
1: Timer 1 enabled.

Bit5: **TF0**: Timer 0 Overflow Flag.
Set by hardware when Timer 0 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 0 interrupt service routine.
0: No Timer 0 overflow detected.
1: Timer 0 has overflowed.

Bit4: **TR0**: Timer 0 Run Control.
0: Timer 0 disabled.
1: Timer 0 enabled.

Bit3: **IE1**: External Interrupt 1.
This flag is set by hardware when an edge/level of type defined by IT1 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 1 service routine if IT1 = 1. When IT1 = 0, this flag is set to 1 when $\overline{INT0}$ is active as defined by bit IN1PL in register IT01CF (see SFR Definition 10.5. "IT01CF: INT0/INT1 Configuration" on page 105).

Bit2: **IT1**: Interrupt 1 Type Select.
This bit selects whether the configured $\overline{INT0}$ interrupt will be edge or level sensitive. $\overline{INT0}$ is configured active low or high by the IN1PL bit in the IT01CF register (see SFR Definition 10.5. "IT01CF: INT0/INT1 Configuration" on page 105).
0: $\overline{INT0}$ is level triggered.
1: $\overline{INT0}$ is edge triggered.

Bit1: **IE0**: External Interrupt 0.
This flag is set by hardware when an edge/level of type defined by IT0 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 0 service routine if IT0 = 1. When IT0 = 0, this flag is set to 1 when $\overline{INT0}$ is active as defined by bit IN0PL in register IT01CF (see SFR Definition 10.5. "IT01CF: INT0/INT1 Configuration" on page 105).

Bit0: **IT0**: Interrupt 0 Type Select.
This bit selects whether the configured $\overline{INT0}$ interrupt will be edge or level sensitive. $\overline{INT0}$ is configured active low or high by the IN0PL bit in register IT01CF (see SFR Definition 10.5. "IT01CF: INT0/INT1 Configuration" on page 105).
0: $\overline{INT0}$ is level triggered.
1: $\overline{INT0}$ is edge triggered.

SFR Definition 18.2. TMOD: Timer Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
GATE1	C/T1	T1M1	T1M0	GATE0	C/T0	T0M1	T0M0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
							SFR Address:	0x89

Bit7: **GATE1**: Timer 1 Gate Control.
0: Timer 1 enabled when TR1 = 1 irrespective of $\overline{\text{INT0}}$ logic level.
1: Timer 1 enabled only when TR1 = 1 AND $\overline{\text{INT0}}$ is active as defined by bit IN1PL in register IT01CF (see SFR Definition 10.5. “IT01CF: INT0/INT1 Configuration” on page 105).

Bit6: **C/T1**: Counter/Timer 1 Select.
0: Timer Function: Timer 1 incremented by clock defined by T1M bit (CKCON.4).
1: Counter Function: Timer 1 incremented by high-to-low transitions on external input pin (T1).

Bits5–4: **T1M1–T1M0**: Timer 1 Mode Select.
These bits select the Timer 1 operation mode.

T1M1	T1M0	Mode
0	0	Mode 0: 13-bit counter/timer
0	1	Mode 1: 16-bit counter/timer
1	0	Mode 2: 8-bit counter/timer with auto-reload
1	1	Mode 3: Timer 1 inactive

Bit3: **GATE0**: Timer 0 Gate Control.
0: Timer 0 enabled when TR0 = 1 irrespective of $\overline{\text{INT0}}$ logic level.
1: Timer 0 enabled only when TR0 = 1 AND $\overline{\text{INT0}}$ is active as defined by bit IN0PL in register IT01CF (see SFR Definition 10.5. “IT01CF: INT0/INT1 Configuration” on page 105).

Bit2: **C/T0**: Counter/Timer Select.
0: Timer Function: Timer 0 incremented by clock defined by T0M bit (CKCON.3).
1: Counter Function: Timer 0 incremented by high-to-low transitions on external input pin (T0).

Bits1–0: **T0M1–T0M0**: Timer 0 Mode Select.
These bits select the Timer 0 operation mode.

T0M1	T0M0	Mode
0	0	Mode 0: 13-bit counter/timer
0	1	Mode 1: 16-bit counter/timer
1	0	Mode 2: 8-bit counter/timer with auto-reload
1	1	Mode 3: Two 8-bit counter/timers

SFR Definition 18.4. TL0: Timer 0 Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x8A

Bits 7–0: **TL0**: Timer 0 Low Byte.
The TL0 register is the low byte of the 16-bit Timer 0.

SFR Definition 18.5. TL1: Timer 1 Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x8B

Bits 7–0: **TL1**: Timer 1 Low Byte.
The TL1 register is the low byte of the 16-bit Timer 1.

SFR Definition 18.6. TH0: Timer 0 High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x8C

Bits 7–0: **TH0**: Timer 0 High Byte.
The TH0 register is the high byte of the 16-bit Timer 0.

SFR Definition 18.7. TH1: Timer 1 High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x8D

Bits 7–0: **TH1**: Timer 1 High Byte.
The TH1 register is the high byte of the 16-bit Timer 1.

18.2.2. 8-bit Timers with Auto-Reload

When T2SPLIT is set, Timer 2 operates as two 8-bit timers (TMR2H and TMR2L). Both 8-bit timers operate in auto-reload mode as shown in Figure 18.5. TMR2RLL holds the reload value for TMR2L; TMR2RLH holds the reload value for TMR2H. The TR2 bit in TMR2CN handles the run control for TMR2H. TMR2L is always running when configured for 8-bit Mode.

Each 8-bit timer may be configured to use SYSCLK, SYSCLK divided by 12, or the external oscillator clock source divided by 8. The Timer 2 Clock Select bits (T2MH and T2ML in CKCON) select either SYSCLK or the clock defined by the Timer 2 External Clock Select bit (T2XCLK in TMR2CN), as follows:

T2MH	T2XCLK	TMR2H Clock Source
0	0	SYSCLK / 12
0	1	External Clock / 8
1	X	SYSCLK

T2ML	T2XCLK	TMR2L Clock Source
0	0	SYSCLK / 12
0	1	External Clock / 8
1	X	SYSCLK

The TF2H bit is set when TMR2H overflows from 0xFF to 0x00; the TF2L bit is set when TMR2L overflows from 0xFF to 0x00. When Timer 2 interrupts are enabled (IE.5), an interrupt is generated each time TMR2H overflows. If Timer 2 interrupts are enabled and TF2LEN (TMR2CN.5) is set, an interrupt is generated each time either TMR2L or TMR2H overflows. When TF2LEN is enabled, software must check the TF2H and TF2L flags to determine the source of the Timer 2 interrupt. The TF2H and TF2L interrupt flags are not cleared by hardware and must be manually cleared by software.

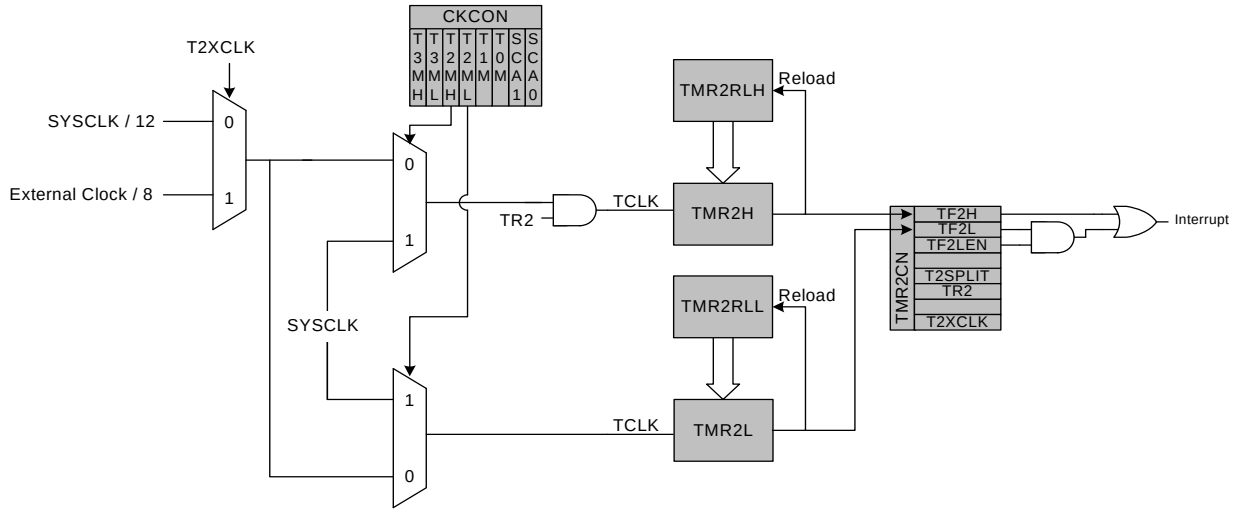


Figure 18.5. Timer 2 8-Bit Mode Block Diagram

18.2.3. External Capture Mode

Capture Mode allows the external oscillator to be measured against the system clock. Timer 2 can be clocked from the system clock, or the system clock divided by 12, depending on the T2ML (CKCON.4) and T2XCLK bits. When a capture event is generated, the contents of Timer 2 (TMR2H:TMR2L) are loaded into the Timer 2 reload registers (TMR2RLH:TMR2RLL) and the TF2H flag is set. A capture event is generated by the falling edge of the clock source being measured, which is the external oscillator/8. By recording the difference between two successive timer capture values, the external oscillator frequency can be determined with respect to the Timer 2 clock. The Timer 2 clock should be much faster than the capture clock to achieve an accurate reading. Timer 2 should be in 16-bit auto-reload mode when using Capture Mode.

For example, if T2ML = 1b and TF2CEN = 1b, Timer 2 will clock every SYSCLK and capture every external clock divided by 8. If the SYSCLK is 24.5 MHz and the difference between two successive captures is 5984, then the external clock frequency is:

$$\frac{24.5\ \text{MHz}}{(5984/8)} = 0.032754\ \text{MHz or } 32.754\ \text{kHz}$$

This mode allows software to determine the external oscillator frequency when an RC network or capacitor is used to generate the clock source.

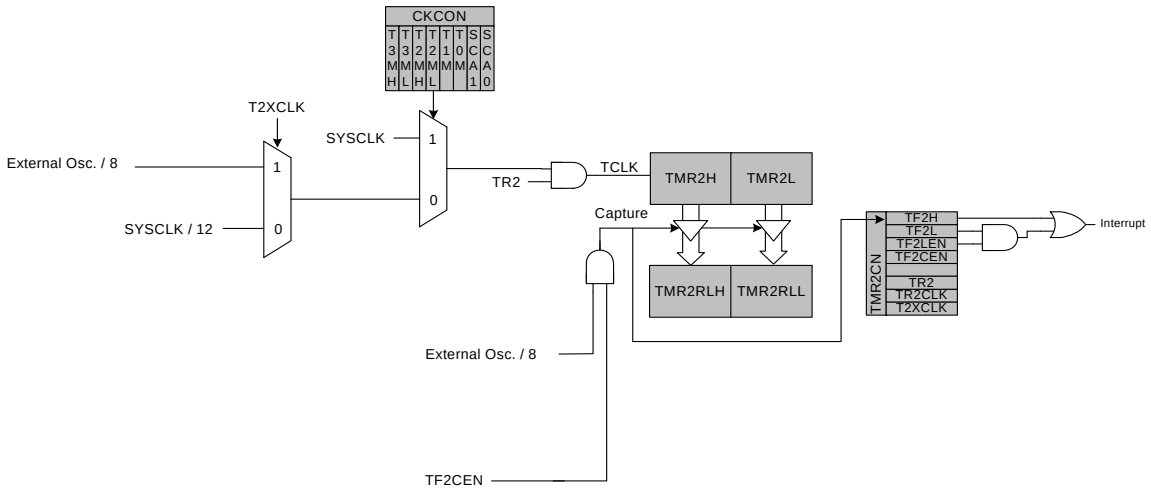


Figure 18.6. Timer 2 Capture Mode Block Diagram

19.3.2. Watchdog Timer Usage

To configure the WDT, perform the following tasks:

- Disable the WDT by writing a 0 to the WDTE bit.
- Select the desired PCA clock source (with the CPS2-CPS0 bits).
- Load PCA0CPL2 with the desired WDT update offset value.
- Configure the PCA Idle mode (set CIDL if the WDT should be suspended while the CPU is in Idle mode).
- Enable the WDT by setting the WDTE bit to 1.

The PCA clock source and Idle mode select cannot be changed while the WDT is enabled. The watchdog timer is enabled by setting the WDTE or WDLCK bits in the PCA0MD register. When WDLCK is set, the WDT cannot be disabled until the next system reset. If WDLCK is not set, the WDT is disabled by clearing the WDTE bit.

The WDT is enabled following any reset. The PCA0 counter clock defaults to the system clock divided by 12, PCA0L defaults to 0x00, and PCA0CPL2 defaults to 0x00. Using Equation 19.4, this results in a WDT timeout interval of 3072 system clock cycles. Table 19.3 lists some example timeout intervals for typical system clocks.

Table 19.3. Watchdog Timer Timeout Intervals[1]

System Clock (Hz)	PCA0CPL2	Timeout Interval (ms)
24,500,000	255	32.1
24,500,000	128	16.2
24,500,000	32	4.1
18,432,000	255	42.7
18,432,000	128	21.5
18,432,000	32	5.5
11,059,200	255	71.1
11,059,200	128	35.8
11,059,200	32	9.2
3,062,500	255	257
3,062,500	128	129.5
3,062,500	32	33.1
191,406[2]	255	4109
191,406[2]	128	2070
191,406[2]	32	530
32,000	255	24576
32,000	128	12384
32,000	32	3168

Notes:
1. Assumes SYSCLK / 12 as the PCA clock source, and a PCA0L value of 0x00 at the update time.
2. Internal oscillator reset frequency.