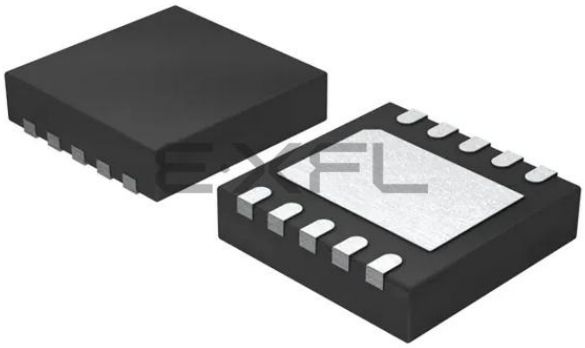

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	6
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	10-VFDFN Exposed Pad
Supplier Device Package	10-DFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f524a-imr

Table 2.7. Comparator Electrical Characteristics

V_{REGIN} = 2.7–5.25 V, –40 to +125 °C unless otherwise noted.
All specifications apply to both Comparator0 and Comparator1 unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
Response Time: Mode 0, Vcm[1] = 1.5 V	CP0+ – CP0– = 100 mV	—	780	—	ns
	CP0+ – CP0– = –100 mV	—	980	—	ns
Response Time: Mode 1, Vcm[1] = 1.5 V	CP0+ – CP0– = 100 mV	—	850	—	ns
	CP0+ – CP0– = –100 mV	—	1120	—	ns
Response Time: Mode 2, Vcm[1] = 1.5 V	CP0+ – CP0– = 100 mV	—	870	—	ns
	CP0+ – CP0– = –100 mV	—	1310	—	ns
Response Time: Mode 3, Vcm[1] = 1.5 V	CP0+ – CP0– = 100 mV	—	1980	—	ns
	CP0+ – CP0– = –100 mV	—	4770	—	ns
Common-Mode Rejection Ratio		—	3	9	mV/V
Positive Hysteresis 1	CP0HYP1-0 = 00	—	0.7	2	mV
Positive Hysteresis 2	CP0HYP1-0 = 01	2	5	10	mV
Positive Hysteresis 3	CP0HYP1-0 = 10	5	10	20	mV
Positive Hysteresis 4	CP0HYP1-0 = 11	13	20	40	mV
Negative Hysteresis 1	CP0HYN1-0 = 00	—	0.7	2	mV
Negative Hysteresis 2	CP0HYN1-0 = 01	2	5	10	mV
Negative Hysteresis 3	CP0HYN1-0 = 10	5	10	20	mV
Negative Hysteresis 4	CP0HYN1-0 = 11	13	20	40	mV
Inverting or Non-Inverting Input Voltage Range[2]		–0.25	—	V_{DD} + 0.25	V
Input Capacitance[2]		—	4	—	pF
Input Bias Current		—	0.5	—	nA
Input Offset Voltage		–15	—	15	mV
Input Impedance		—	1.5	—	kΩ
Power Supply					
Power Supply Rejection[2]		—	0.2	4	mV/V
Power-up Time		—	2.3	—	µs
Supply Current at DC	Mode 0	—	6	30	µA
	Mode 1	—	3	15	µA
	Mode 2	—	2	7.5	µA
	Mode 3	—	0.3	3.8	µA

Notes:
1. Vcm is the common-mode voltage on CP0+ and CP0–.
2. Guaranteed by design and/or characterization.

Table 2.9. Flash Electrical Characteristics

V_{DD} = 1.8 to 2.75 V; –40 to +125 ºC unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Flash Size	’F520/0A/1/1A and ’F530/0A/1/1A ’F523/3A/4/4A and ’F533/3A/4/4A ’F526/6A/7/7A and ’F536/6A/7/7A	7680 4096 2048	—	—	bytes
Endurance[2]	$V_{DD} \geq V_{RST\text{-}HIGH}$[1]	20 k	150 k	—	Erase/Write
Erase Cycle Time		27	32	38	ms
Write Cycle Time		57	65	74	µs
V_{DD}	Write/Erase Operations	$V_{RST\text{-}HIGH}$[1]	—	—	V

Notes:

1. See Table 2.8 on page 32 for the $V_{RST\text{-}HIGH}$ specification.
2. For –I (industrial Grade) parts, flash should be programmed (erase/write) at a minimum temperature of 0 °C for reliable flash operation across the entire temperature range of –40 to +125 °C. This minimum programming temperature does not apply to –A (Automotive Grade) parts.

Table 2.10. Port I/O DC Electrical Characteristics

V_{REGIN} = 2.7 to 5.25 V, –40 to +125 °C unless otherwise specified

Parameters	Conditions	Min	Typ	Max	Units
Output High Voltage	I_{OH} = –3 mA, Port I/O push-pull I_{OH} = –10 µA, Port I/O push-pull I_{OH} = –10 mA, Port I/O push-pull	V_{REGIN} – 0.4 V_{REGIN} – 0.02 —	— — V_{REGIN} – 0.7	— — —	V
Output Low Voltage	**V_{REGIN} = 2.7 V:** I_{OL} = 70 µA I_{OL} = 8.5 mA **V_{REGIN} = 5.25 V:** I_{OL} = 70 µA I_{OL} = 8.5 mA	 — — — —	 — — — —	 45 550 40 400	mV
Input High Voltage		V_{REGIN} x 0.7	—	—	V
Input Low Voltage		—	—	V_{REGIN} x 0.3	V
Input Leakage Current	Weak Pullup Off **C8051F52xA/53xA:** Weak Pullup On, V_{IN} = 0 V; V_{REGIN} = 1.8 V **C8051F52x/52xA/53x/53xA:** Weak Pullup On, V_{IN} = 0 V; V_{REGIN} = 2.7 V Weak Pullup On, V_{IN} = 0 V; V_{REGIN} = 5.25 V	— — — —	— 5 20 65	±2 15 50 115	µA

Table 3.4. Pin Definitions for the C8051F53x and C805153xA (TSSOP 20) (Continued)

Name	Pin Numbers		Type	Description
	'F53xA 'F53x-C	'F53x		
P0.4/TX*	19	—	D I/O or A In	Port 0.4. See Port I/O Section for a complete description.
P0.4/RX*	—	19	D I/O or A In	Port 0.4. See Port I/O Section for a complete description.
P0.3	20	—	D I/O or A In	Port 0.3. See Port I/O Section for a complete description.
P0.3/TX*	—	20	D I/O or A In	Port 0.3. See Port I/O Section for a complete description.
***Note:** Please refer to Section "20. Device Specific Behavior" on page 210.				

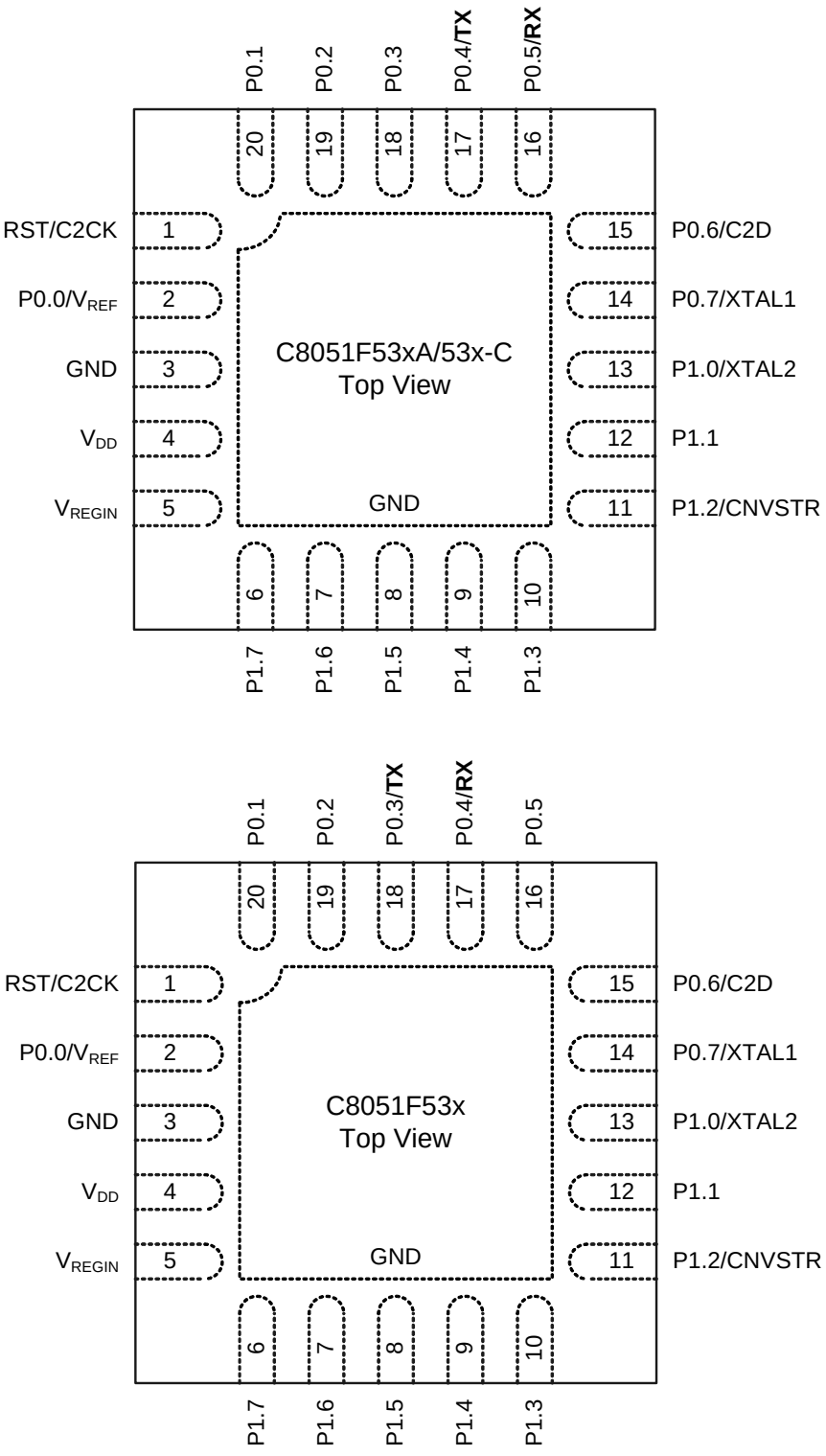

Figure 3.7. QFN-20 Pinout Diagram (Top View)

Post-Tracking Mode is selected when AD0TM is set to 01b. A programmable tracking time based on AD0TK is started immediately following the convert start signal. Conversions are started after the programmed tracking time ends. After a conversion is complete, ADC0 does not track the input. Rather, the sampling capacitor remains disconnected from the input making the input pin high-impedance until the next convert start signal.

Dual-Tracking Mode is selected when AD0TM is set to 11b. A programmable tracking time based on AD0TK is started immediately following the convert start signal. Conversions are started after the programmed tracking time ends. After a conversion is complete, ADC0 tracks continuously until the next conversion is started.

Depending on the output connected to the ADC input, additional tracking time, more than is specified in Table 2.3 on page 28, may be required after changing MUX settings. See the settling time requirements described in Section “4.3.6. Settling Time Requirements” on page 60.

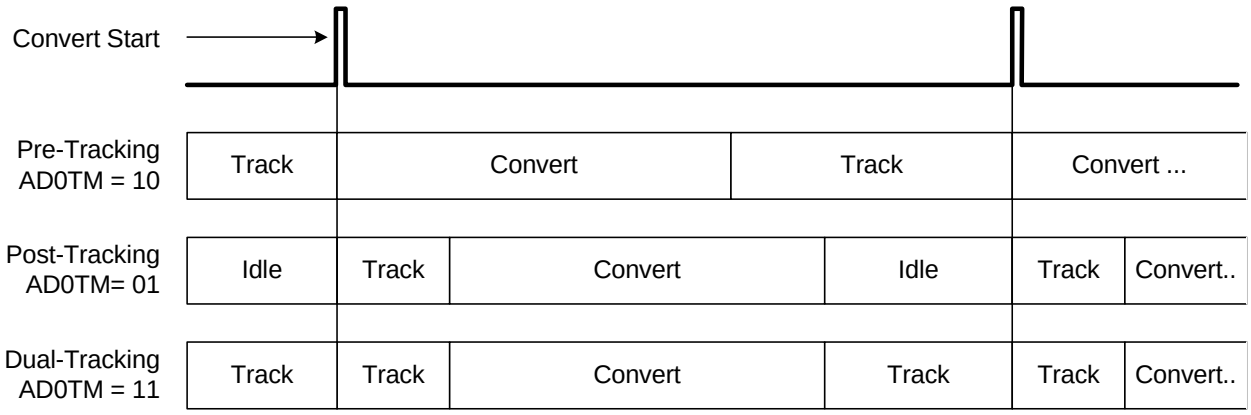

Figure 4.3. ADC0 Tracking Modes

4.3.3. Timing

ADC0 has a maximum conversion speed specified in Table 2.3 on page 28. ADC0 is clocked from the ADC0 Subsystem Clock (FCLK). The source of FCLK is selected based on the BURSTEN bit. When BURSTEN is logic 0, FCLK is derived from the current system clock. When BURSTEN is logic 1, FCLK is derived from the Burst Mode Oscillator, which is an independent clock source whose maximum frequency is specified in Table 2.3 on page 28.

When ADC0 is performing a conversion, it requires a clock source that is typically slower than FCLK. The ADC0 SAR conversion clock (SAR clock) is a divided version of FCLK. The divide ratio can be configured using the AD0SC bits in the ADC0CF register. The maximum SAR clock frequency is listed in Table 2.3 on page 28.

ADC0 can be in one of three states at any given time: tracking, converting, or idle. Tracking time depends on the tracking mode selected. For Pre-Tracking Mode, tracking is managed by software and ADC0 starts conversions immediately following the convert start signal. For Post-Tracking and Dual-Tracking Modes, the tracking time after the convert start signal is equal to the value determined by the AD0TK bits plus 2 FCLK cycles. Tracking is immediately followed by a conversion. The ADC0 conversion time is always 13 SAR clock cycles plus an additional 2 FCLK cycles to start and complete a conversion. Figure 4.4 shows timing diagrams for a conversion in Pre-Tracking Mode and tracking plus conversion in Post-Tracking or Dual-Tracking Mode. In this example, repeat count is set to one.

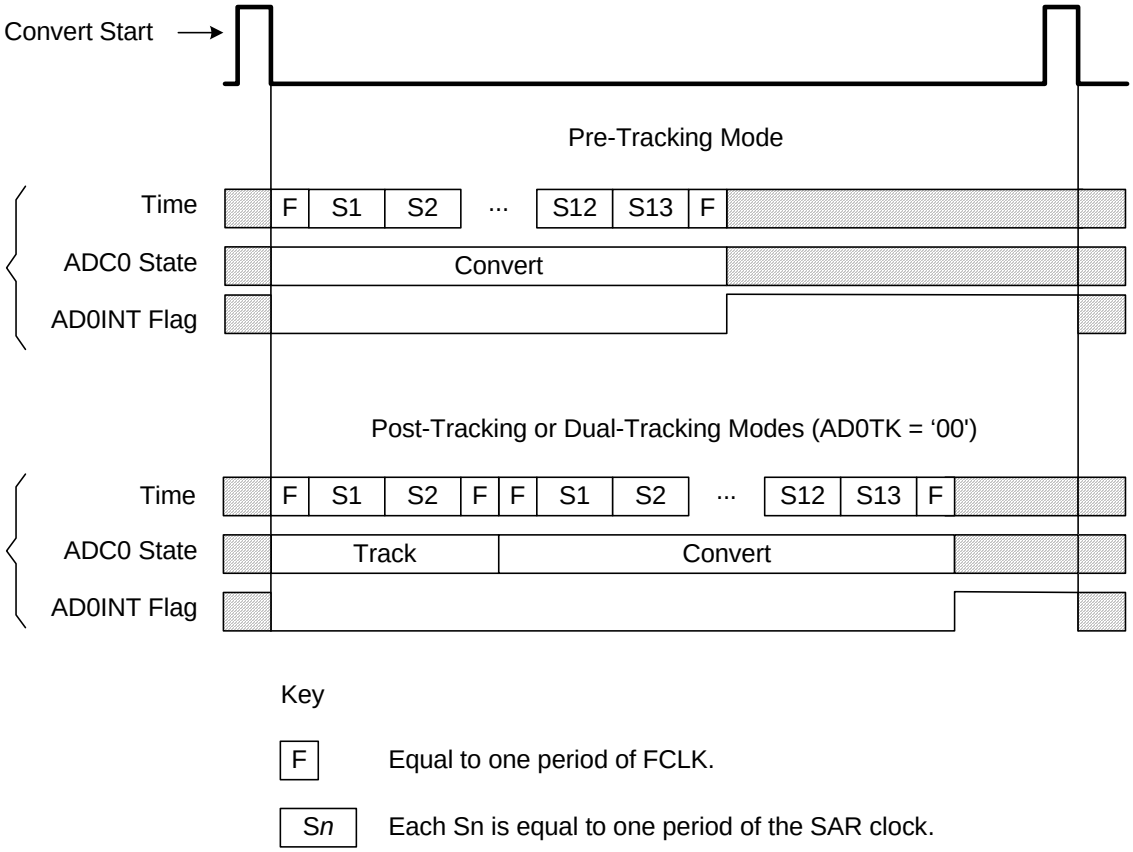

Figure 4.4. 12-Bit ADC Tracking Mode Example

Gain Register Definition 4.1. ADC0GNH: ADC0 Selectable Gain High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
GAINH[7:0]								11111100
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Address:
								0x04

Bits7–0: High byte of Selectable Gain Word.

Gain Register Definition 4.2. ADC0GNL: ADC0 Selectable Gain Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
GAINL[3:0]				Reserved	Reserved	Reserved	Reserved	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Address:
								0x07

Bits7–4: Lower 4 bits of the Selectable Gain Word.
Bits3–0: **Reserved**. Must Write 0000b.

Gain Register Definition 4.3. ADC0GNA: ADC0 Additional Selectable Gain

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	GAINADD	00000001
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Address:
								0x08

Bits7–1: **Reserved**. Must Write 0000000b.
Bit0: **GAINADD**: Additional Gain Bit.
Setting this bit adds 1/64 (0.016) gain to the gain value in the ADC0GNH and ADC0GNL registers.

SFR Definition 4.12. ADC0LTH: ADC0 Less-Than Data High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xC6

Bits7–0: High byte of ADC0 Less-Than Data Word.

SFR Definition 4.13. ADC0LTL: ADC0 Less-Than Data Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xC5

Bits7–0: Low byte of ADC0 Less-Than Data Word.

8. CIP-51 Microcontroller

The MCU system controller core is the CIP-51 microcontroller. The CIP-51 is fully compatible with the MCS-51™ instruction set. Standard 803x/805x assemblers and compilers can be used to develop software. The C8051F52x/F52xA/F53x/F53xA family has a superset of all the peripherals included with a standard 8051. See Section “1. System Overview” on page 13 for more information about the available peripherals. The CIP-51 includes on-chip debug hardware which interfaces directly with the analog and digital subsystems, providing a complete data acquisition or control-system solution in a single integrated circuit.

The CIP-51 Microcontroller core implements the standard 8051 organization and peripherals as well as additional custom peripherals and functions to extend its capability (see Figure 8.1 for a block diagram). The CIP-51 core includes the following features:

- Fully Compatible with MCS-51 Instruction Set
- 25 MIPS Peak Throughput
- 256 Bytes of Internal RAM
- Extended Interrupt Handler
- Reset Input
- Power Management Modes
- Integrated Debug Logic
- Program and Data Memory Security

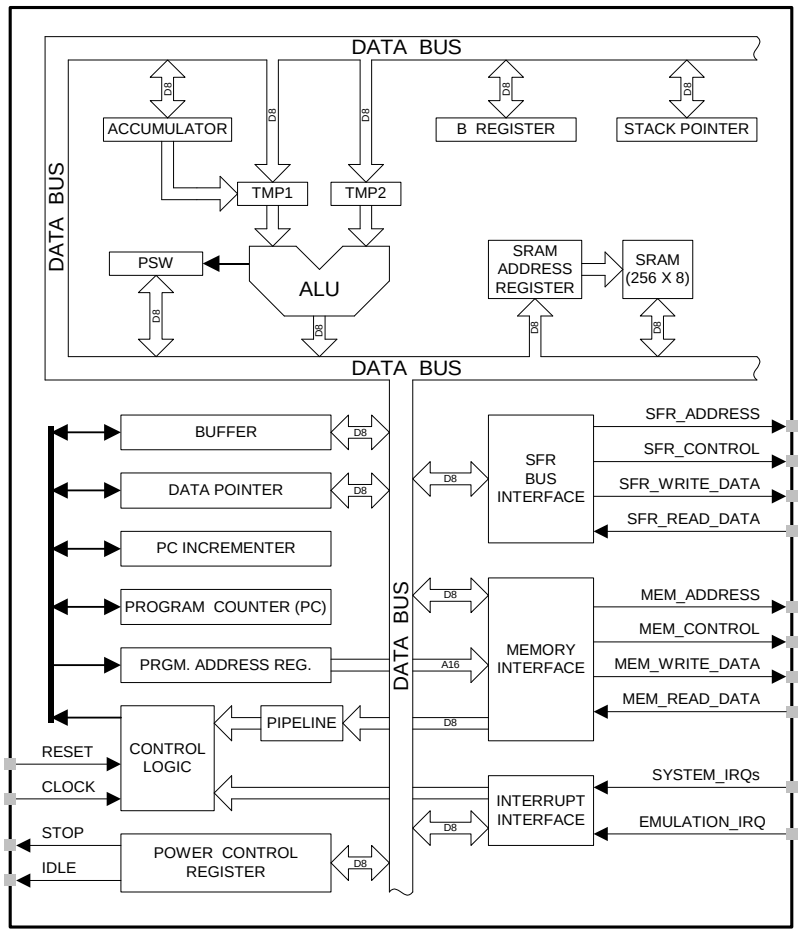

Figure 8.1. CIP-51 Block Diagram

Table 9.2. Special Function Registers

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Description	Page
ACC	0xE0	Accumulator	89
ADC0CF	0xBC	ADC0 Configuration	65
ADC0CN	0xE8	ADC0 Control	67
ADC0H	0xBE	ADC0	66
ADC0L	0xBD	ADC0	66
ADC0GTH	0xC4	ADC0 Greater-Than Data High Byte	69
ADC0GTL	0xC3	ADC0 Greater-Than Data Low Byte	69
ADC0LTH	0xC6	ADC0 Less-Than Data High Byte	70
ADC0LTL	0xC5	ADC0 Less-Than Data Low Byte	70
ADC0MX	0xBB	ADC0 Channel Select	64
ADC0TK	0xBA	ADC0 Tracking Mode Select	68
B	0xF0	B Register	89
CKCON	0x8E	Clock Control	188
CLKSEL	0xA9	Clock Select	143
CPT0CN	0x9B	Comparator0 Control	78
CPT0MD	0x9D	Comparator0 Mode Selection	80
CPT0MX	0x9F	Comparator0 MUX Selection	79
DPH	0x83	Data Pointer High	87
DPL	0x82	Data Pointer Low	87
EIE1	0xE6	Extended Interrupt Enable 1	102
EIP1	0xF6	Extended Interrupt Priority 1	103
FLKEY	0xB7	Flash Lock and Key	119
IE	0xA8	Interrupt Enable	100
IP	0xB8	Interrupt Priority	101
IT01CF	0xE4	INT0/INT1 Configuration	105
LINADDR	0x92	LIN indirect address pointer	172
LINCF	0x95	LIN master-slave and automatic baud rate selection	173
LINDATA	0x93	LIN indirect data buffer	172
OSCICL	0xB3	Internal Oscillator Calibration	138

SFR Definition 10.2. IP: Interrupt Priority

R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	PSPI0	PT2	PS0	PT1	PX1	PT0	PX0	10000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable
							SFR Address:	0xB8

Bit7: **UNUSED**. Read = 1b; Write = don't care.
Bit6: **PSPI0**: Serial Peripheral Interface (SPI0) Interrupt Priority Control.
This bit sets the priority of the SPI0 interrupt.
0: SPI0 interrupt set to low priority level.
1: SPI0 interrupt set to high priority level.
Bit5: **PT2**: Timer 2 Interrupt Priority Control.
This bit sets the priority of the Timer 2 interrupt.
0: Timer 2 interrupt set to low priority level.
1: Timer 2 interrupt set to high priority level.
Bit4: **PS0**: UART0 Interrupt Priority Control.
This bit sets the priority of the UART0 interrupt.
0: UART0 interrupt set to low priority level.
1: UART0 interrupt set to high priority level.
Bit3: **PT1**: Timer 1 Interrupt Priority Control.
This bit sets the priority of the Timer 1 interrupt.
0: Timer 1 interrupt set to low priority level.
1: Timer 1 interrupt set to high priority level.
Bit2: **PX1**: External Interrupt 0 Priority Control.
This bit sets the priority of the external interrupt 1.
0: INT1 interrupt set to low priority level.
1: INT1 interrupt set to high priority level.
Bit1: **PT0**: Timer 0 Interrupt Priority Control.
This bit sets the priority of the Timer 0 interrupt.
0: Timer 0 interrupt set to low priority level.
1: Timer 0 interrupt set to high priority level.
Bit0: **PX0**: External Interrupt 0 Priority Control.
This bit sets the priority of the external interrupt 0.
0: INT0 interrupt set to low priority level.
1: INT0 interrupt set to high priority level.

12.3. Non-volatile Data Storage

The Flash memory can be used for non-volatile data storage as well as program code. This allows data such as calibration coefficients to be calculated and stored at run time. Data is written using the MOVX write instruction and read using the MOVC instruction. Note: MOVX read instructions always target XRAM.

Note: See Section “12.1. Programming The Flash Memory” on page 113 for minimum V_{DD} and temperature requirements for flash erase and write operations.

12.4. Security Options

The CIP-51 provides security options to protect the Flash memory from inadvertent modification by software as well as to prevent the viewing of proprietary program code and constants. The Program Store Write Enable (bit PSWE in register PSCTL) and the Program Store Erase Enable (bit PSEE in register PSCTL) bits protect the Flash memory from accidental modification by software. PSWE must be explicitly set to 1 before software can modify the Flash memory; both PSWE and PSEE must be set to 1 before software can erase Flash memory. Additional security features prevent proprietary program code and data constants from being read or altered across the C2 interface.

A Security Lock Byte located at the last byte of Flash user space offers protection of the Flash program memory from access (reads, writes, or erases) by unprotected code or the C2 interface. The Flash security mechanism allows the user to lock *n* 512-byte Flash pages, starting at page 0 (addresses 0x0000 to 0x01FF), where *n* is the 1’s complement number represented by the Security Lock Byte. **Note that the page containing the Flash Security Lock Byte is unlocked when no other Flash pages are locked (all bits of the Lock Byte are 1) and locked when any other Flash pages are locked (any bit of the Lock Byte is 0).** See example below.

Security Lock Byte:	11111101b
1’s Complement:	00000010b
Flash pages locked:	3 (First two Flash pages + Lock Byte Page)
Addresses locked:	0x0000 to 0x03FF (first two Flash pages) 0x1C00 to 0x1DFF in ’F520/0A/1/1A and ’F530/0A/1/1A 0x0C00 to 0x0FFF in ’F523/3A/4/4A and ’F533/3A/4/4A and 0x0600 to 0x07FF in ’F526/6A/7/7A and ’F536/6A/7/7A

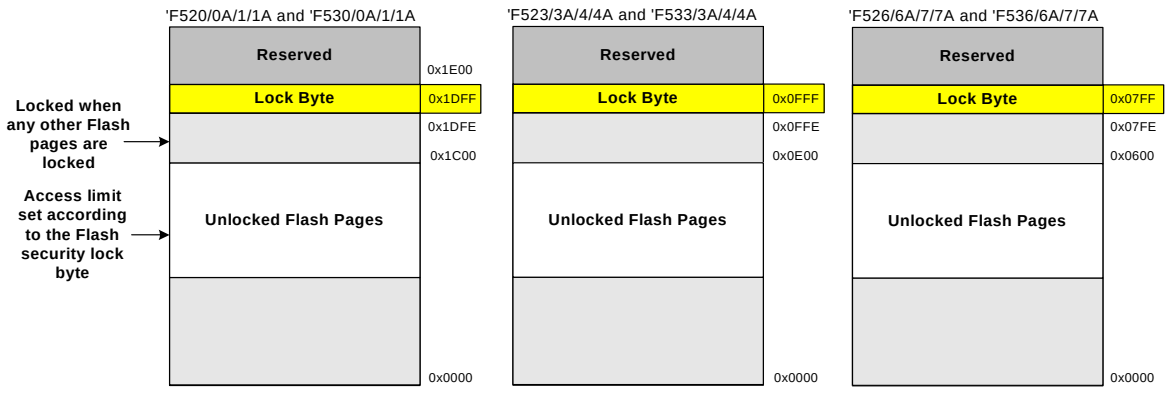

Figure 12.1. Flash Program Memory Map

Note: The load capacitance depends upon the crystal and the manufacturer. Please refer to the crystal data sheet when completing these calculations.

The equation for determining the load capacitance for two capacitors is:

$$C_L = \frac{C_A \times C_B}{C_A + C_B} + C_S$$

Where:
C_A and C_B are the capacitors connected to the crystal leads.
C_S is the total stray capacitance of the PCB.
The stray capacitance for a typical layout where the crystal is as close as possible to the pins is 2–5 pF per pin.

If C_A and C_B are the same (C), then the equation becomes:

$$C_L = \frac{C}{2} + C_S$$

For example, a tuning-fork crystal of 32 kHz with a recommended load capacitance of 12.5 pF should use the configuration shown in Figure 14.1, Option 1. With a stray capacitance of 3 pF per pin (6 pF total), the 13 pF capacitors yield an equivalent capacitance of 12.5 pF across the crystal, as shown in Figure 14.2.

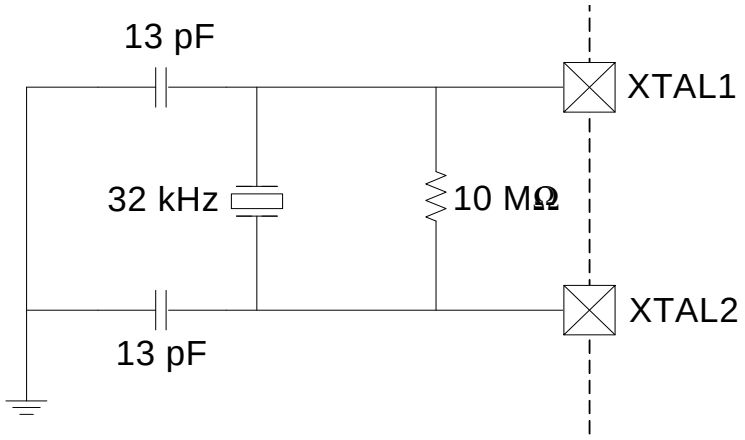

Figure 14.2. 32 kHz External Crystal Example

Important Note on External Crystals: Crystal oscillator circuits are quite sensitive to PCB layout. The crystal should be placed as close as possible to the XTAL pins on the device. The traces should be as short as possible and shielded with ground plane from any other traces which could introduce noise or interference.

15.2.2. 9-Bit UART

9-bit UART mode uses a total of eleven bits per data byte: a start bit, 8 data bits (LSB first), a programmable ninth data bit, and a stop bit. The state of the ninth transmit data bit is determined by the value in TB80 (SCON0.3), which is assigned by user software. It can be assigned the value of the parity flag (bit P in register PSW) for error detection, or used in multiprocessor communications. On receive, the ninth data bit goes into RB80 (SCON0.2) and the stop bit is ignored.

Data transmission begins when an instruction writes a data byte to the SBUF0 register. The TI0 Transmit Interrupt Flag (SCON0.1) is set at the end of the transmission (the beginning of the stop-bit time). Data reception can begin any time after the REN0 Receive Enable bit (SCON0.4) is set to 1. After the stop bit is received, the data byte will be loaded into the SBUF0 receive register if the following conditions are met: (1) RI0 must be logic 0, and (2) if MCE0 is logic 1, the 9th bit must be logic 1 (when MCE0 is logic 0, the state of the ninth data bit is unimportant). If these conditions are met, the eight bits of data are stored in SBUF0, the ninth bit is stored in RB80, and the RI0 flag is set to 1. If the above conditions are not met, SBUF0 and RB80 will not be loaded and the RI0 flag will not be set to 1. A UART0 interrupt will occur if enabled when either TI0 or RI0 is set to 1.

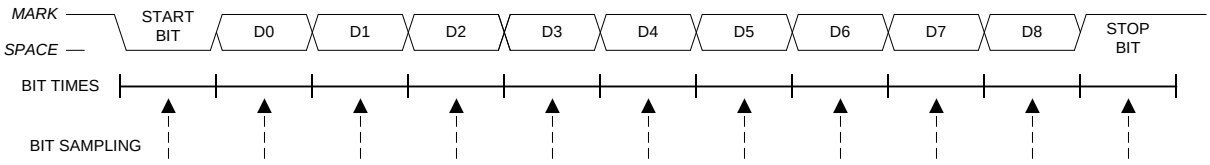

Figure 15.5. 9-Bit UART Timing Diagram

The shift register contents are locked after the slave detects the first edge of SCK. Writes to SPI0DAT that occur after the first SCK edge will be held in the TX latch until the end of the current transfer.

When configured as a slave, SPI0 can be configured for 4-wire or 3-wire operation. The default, 4-wire slave mode, is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 1. In 4-wire mode, the NSS signal is routed to a port pin and configured as a digital input. SPI0 is enabled when NSS is logic 0, and disabled when NSS is logic 1. The bit counter is reset on a falling edge of NSS. Note that the NSS signal must be driven low at least 2 system clocks before the first active edge of SCK for each byte transfer. Figure 16.4 shows a connection diagram between two slave devices in 4-wire slave mode and a master device.

3-wire slave mode is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 0. NSS is not used in this mode, and is not mapped to an external port pin through the crossbar. Since there is not a way of uniquely addressing the device in 3-wire slave mode, SPI0 must be the only slave device present on the bus. It is important to note that in 3-wire slave mode there is no external means of resetting the bit counter that determines when a full byte has been received. The bit counter can only be reset by disabling and re-enabling SPI0 with the SPIEN bit. Figure 16.3 shows a connection diagram between a slave device in 3-wire slave mode and a master device.

16.4. SPI0 Interrupt Sources

When SPI0 interrupts are enabled, the following four flags will generate an interrupt when they are set to logic 1:

Note that all of the following interrupt bits must be cleared by software.

1. The SPI Interrupt Flag, SPIF (SPI0CN.7) is set to logic 1 at the end of each byte transfer. This flag can occur in all SPI0 modes.
2. The Write Collision Flag, WCOL (SPI0CN.6) is set to logic 1 if a write to SPI0DAT is attempted when the transmit buffer has not been emptied to the SPI shift register. When this occurs, the write to SPI0DAT will be ignored, and the transmit buffer will not be written.This flag can occur in all SPI0 modes.
3. The Mode Fault Flag MODF (SPI0CN.5) is set to logic 1 when SPI0 is configured as a master in multi-master mode and the NSS pin is pulled low. When a Mode Fault occurs, the MSTEN and SPIEN bits in SPI0CN are set to logic 0 to disable SPI0 and allow another master device to access the bus.
4. The Receive Overrun Flag RXOVRN (SPI0CN.4) is set to logic 1 when configured as a slave, and a transfer is completed while the receive buffer still holds an unread byte from a previous transfer. The new byte is not transferred to the receive buffer, allowing the previously received data byte to be read. The data byte which caused the overrun is lost.

Table 16.1. SPI Slave Timing Parameters

Parameter	Description	Min	Max	Units
Master Mode Timing* (See Figure 16.6 and Figure 16.7)				
T_{MCKH}	SCK High Time	1 x T_{SYSCLK}	—	ns
T_{MCKL}	SCK Low Time	1 x T_{SYSCLK}	—	ns
T_{MIS}	MISO Valid to SCK Sample Edge	20	—	ns
T_{MIH}	SCK Sample Edge to MISO Change	0	—	ns
Slave Mode Timing* (See Figure 16.8 and Figure 16.9)				
T_{SE}	NSS Falling to First SCK Edge	2 x T_{SYSCLK}	—	ns
T_{SD}	Last SCK Edge to NSS Rising	2 x T_{SYSCLK}	—	ns
T_{SEZ}	NSS Falling to MISO Valid	—	4 x T_{SYSCLK}	ns
T_{SDZ}	NSS Rising to MISO High-Z	—	4 x T_{SYSCLK}	ns
T_{CKH}	SCK High Time	5 x T_{SYSCLK}	—	ns
T_{CKL}	SCK Low Time	5 x T_{SYSCLK}	—	ns
T_{SIS}	MOSI Valid to SCK Sample Edge	2 x T_{SYSCLK}	—	ns
T_{SIH}	SCK Sample Edge to MOSI Change	2 x T_{SYSCLK}	—	ns
T_{SOH}	SCK Shift Edge to MISO Change	—	4 x T_{SYSCLK}	ns

Note: T_{SYSCLK} is equal to one period of the device system clock (SYSCLK) in ns.
The maximum possible frequency of the SPI can be calculated as:
Transmission: SYSCLK/2
Reception: SYSCLK/10

SFR Definition 17.17. LIN0MUL: LIN0 Multiplier Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
PRESCL[1:0]		LINMUL[4:0]					DIV9	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Address: 0x0D (indirect)

Bit7–6: **PRESCL1–0**: LIN Baud Rate Prescaler Bits.
These bits are the baud rate prescaler bits.

Bit5–1: **LINMUL4–0**: LIN Baud Rate Multiplier Bits.
These bits are the baud rate multiplier bits. These bits are not used in slave mode.

Bit0: **DIV9**: LIN Baud Rate Divider Most Significant Bit.
The most significant bit of the baud rate divider. The 8 least significant bits are in LIN0DIV.
The valid range for the divider is 200 to 511.

SFR Definition 17.18. LIN0ID: LIN0 ID Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
		ID[5:0]						00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Address: 0x0E (indirect)

Bit7–6: **UNUSED**. Read = 00b. Write = don't care.

Bit5–0: **ID5–0**: LIN Identifier Bits.
These bits form the data identifier.

If the LINSIZE bits (LIN0SIZE[3:0]) are 1111b, bits ID[5:4] are used to determine the data size and are interpreted as follows:
00: 2 bytes
01: 2 bytes
10: 4 bytes
11: 8 bytes

19.2.5. 8-Bit Pulse Width Modulator Mode

Each module can be used independently to generate a pulse width modulated (PWM) output on its associated CEXn pin. The frequency of the output is dependent on the timebase for the PCA counter/timer. The duty cycle of the PWM output signal is varied using the module's PCA0CPHn capture/compare register. When the value in the low byte of the PCA counter/timer (PCA0L) is equal to the value in PCA0CPLn, the output on the CEXn pin will be set. When the count value in PCA0L overflows, the CEXn output will be reset (see Figure 19.8). Also, when the counter/timer low byte (PCA0L) overflows from 0xFF to 0x00, PCA0CPLn is reloaded automatically with the value stored in the module's capture/compare high byte (PCA0CPHn) without software intervention. Setting the ECOMn and PWMn bits in the PCA0CPMn register enables 8-Bit Pulse Width Modulator mode. The duty cycle for 8-Bit PWM Mode is given by Equation 19.2.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

$$DutyCycle = \frac{(256 - PCA0CPHn)}{256}$$

Equation 19.2. 8-Bit PWM Duty Cycle

Using Equation 19.2, the largest duty cycle is 100% (PCA0CPHn = 0), and the smallest duty cycle is 0.39% (PCA0CPHn = 0xFF). A 0% duty cycle may be generated by clearing the ECOMn bit to 0.

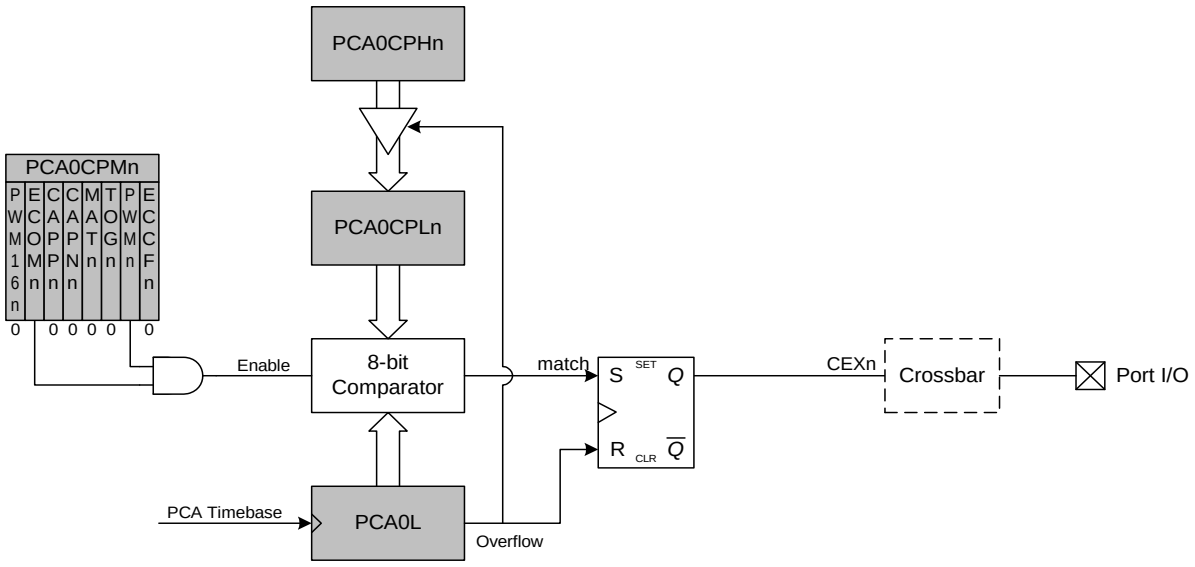

Figure 19.8. PCA 8-Bit PWM Mode Diagram

20. Device Specific Behavior

This chapter contains behavioral differences between the silicon revisions of C8051F52x/52xA/F53x/53xA devices.

These differences do not affect the functionality or performance of most systems and are described below.

20.1. Device Identification

The Part Number Identifier on the top side of the device package can be used for decoding device information. The first character of the trace code identifies the silicon revision. On C8051F52x-C/53x-C devices, the trace code (second line on the TSSOP-20 and DFN-10 packages; third line on the QFN-20 package) will begin with the letter "C". The "A" suffix at the end of the part number such as "C8051F530A" is only present on Revision B devices. All other revisions do not include this suffix. Figures 20.1, 20.2, and 20.3 show how to find the part number on the top side of the device package.

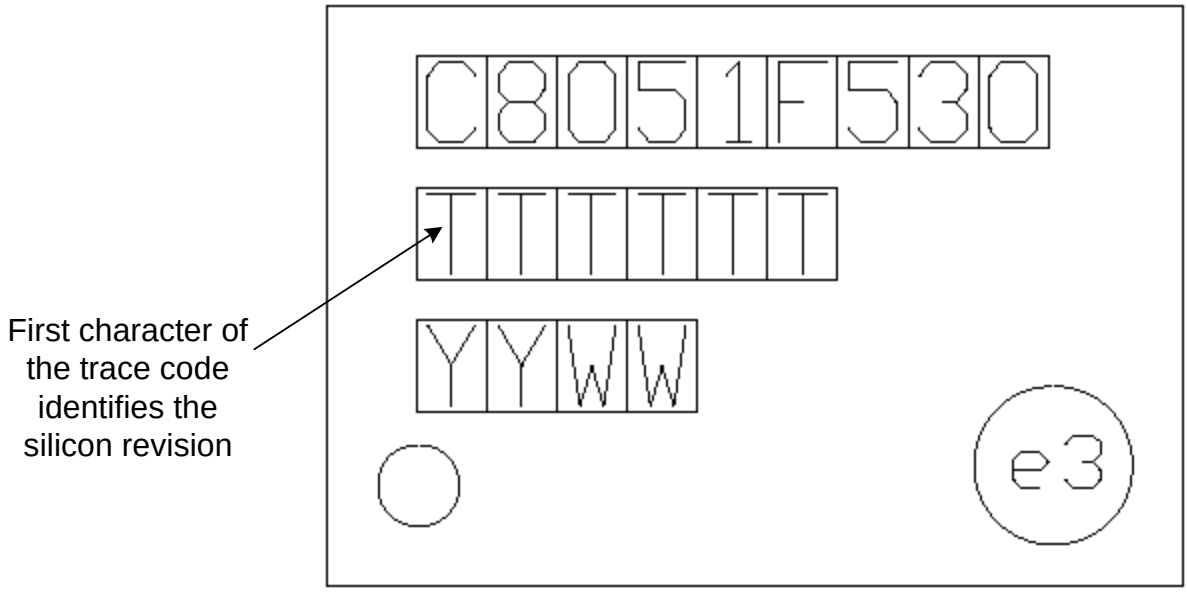

Figure 20.1. Device Package—TSSOP 20

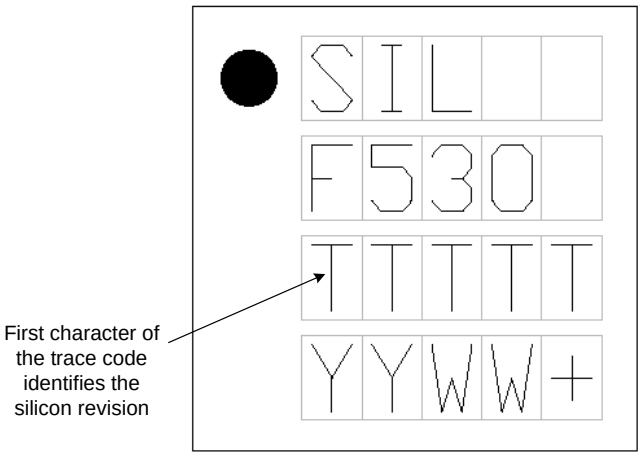

Figure 20.2. Device Package—QFN 20

C2 Register Definition 21.3. REVID: C2 Revision ID

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Reset Value
								Varies

This read-only register returns the 8-bit revision ID.
For example, 0x00 = Revision A.

C2 Register Definition 21.4. FPCTL: C2 Flash Programming Control

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Reset Value
								00000000

Bits7–0 **FPCTL**: Flash Programming Control Register.
This register is used to enable Flash programming via the C2 interface. To enable C2 Flash programming, the following codes must be written in order: 0x02, 0x01. Note that once C2 Flash programming is enabled, a system reset must be issued to resume normal operation.

C2 Register Definition 21.5. FPDAT: C2 Flash Programming Data

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Reset Value
								00000000

Bits7–0: **FPDAT**: C2 Flash Programming Data Register.
This register is used to pass Flash commands, addresses, and data during C2 Flash accesses. Valid commands are listed below.

Code	Command
0x06	Flash Block Read
0x07	Flash Block Write
0x08	Flash Page Erase
0x03	Device Erase