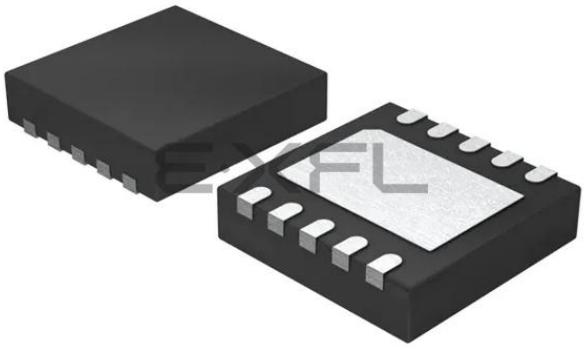

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	6
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.25V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	10-VFDFN Exposed Pad
Supplier Device Package	10-DFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f526-c-imr

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1.5. 12-Bit Analog to Digital Converter

The C8051F52x/F52xA/F53x/F53xA devices include an on-chip 12-bit SAR ADC with a maximum throughput of 200 ksps. The ADC system includes a configurable analog multiplexer that selects the positive ADC input, which is measured with respect to GND. Ports 0 and 1 are available as ADC inputs; additionally, the ADC includes an innovative programmable gain stage which allows the ADC to sample inputs sources greater than the VREF voltage. The on-chip Temperature Sensor output and the core supply voltage (V_{DD}) are also available as ADC inputs. User firmware may shut down the ADC or use it in Burst Mode to save power.

Conversions can be initiated in four ways: a software command, an overflow of Timer 1, an overflow of Timer 2, or an external convert start signal. This flexibility allows the start of conversion to be triggered by software events, a periodic signal (timer overflows), or external HW signals. Conversion completions are indicated by a status bit and an interrupt (if enabled) and occur after 1, 4, 8, or 16 samples have been accumulated by a hardware accumulator. The resulting 12-bit to 16-bit data word is latched into the ADC data SFRs upon completion of a conversion. When the system clock is slow, Burst Mode allows ADC0 to automatically wake from a low power shutdown state, acquire and accumulate samples, then re-enter the low power shutdown state without CPU intervention.

Window compare registers for the ADC data can be configured to interrupt the controller when ADC data is either within or outside of a specified range. The ADC can monitor a key voltage continuously in background mode, but not interrupt the controller unless the converted data is within/outside the specified range.

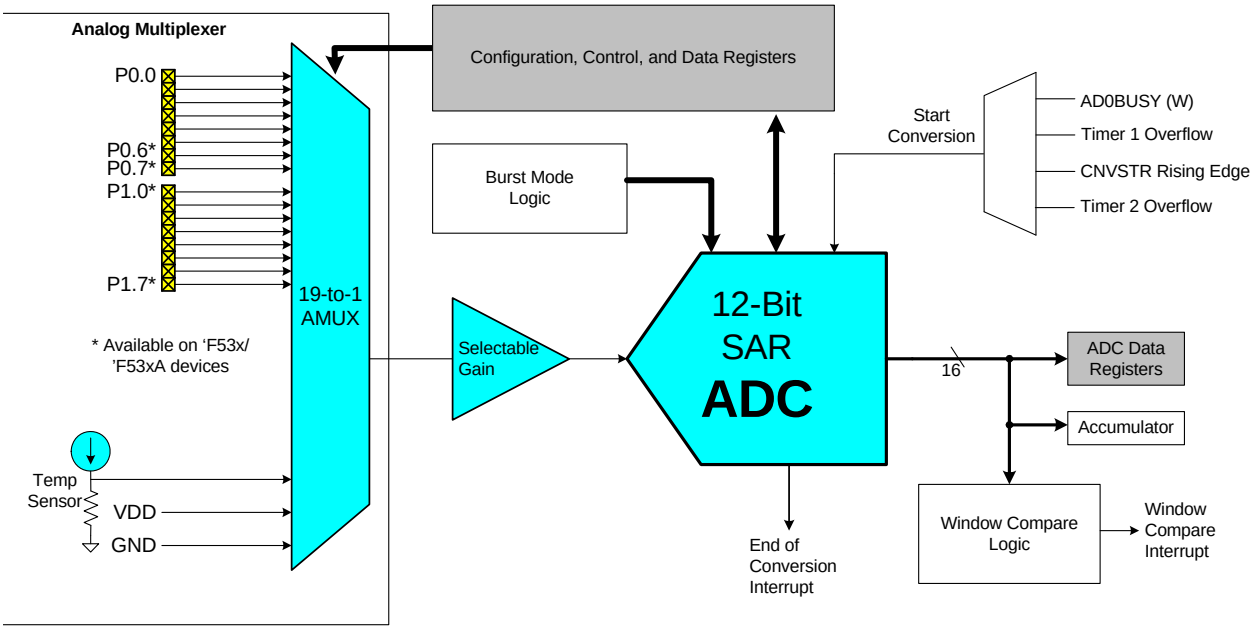


Figure 1.7. 12-Bit ADC Block Diagram

Table 2.2. Global DC Electrical Characteristics

–40 to +125 °C, 25 MHz System Clock unless otherwise specified. Typical values are given at 25 °C

Parameter	Conditions	Min	Typ	Max	Units
Digital Supply Current—CPU Inactive (Idle Mode, not fetching instructions from Flash)					
Idle I_{DD}[3,4]	**V_{DD} = 2.1 V:**				
	Clock = 32 kHz	—	8	—	µA
	Clock = 200 kHz	—	22	—	µA
	Clock = 1 MHz	—	0.09	—	mA
	Clock = 25 MHz	—	2.2	5	mA
	V_{DD} = 2.6 V:				
	Clock = 32 kHz	—	9	—	µA
	Clock = 200 kHz	—	30	—	µA
	Clock = 1 MHz	—	0.13	—	mA
	Clock = 25 MHz	—	3	6.5	mA
Idle I_{DD} Frequency Sensitivity[3,6]	T = 25 °C:				
	V_{DD} = 2.1 V, F ≤ 1 MHz	—	90	—	µA/MHz
	V_{DD} = 2.1 V, F > 1 MHz	—	90	—	µA/MHz
	V_{DD} = 2.6 V, F ≤ 1 MHz	—	118	—	µA/MHz
	V_{DD} = 2.6 V, F > 1 MHz	—	118	—	µA/MHz
Digital Supply Current[3] (Stop or Suspend Mode)	Oscillator not running, V_{DD} Monitor Disabled.				
	T = 25 °C	—	2	—	µA
	T = 60 °C	—	3	—	µA
	T = 125 °C	—	50	—	µA

Notes:

1. For more information on V_{REGIN} characteristics, see Table 2.6 on page 30.
2. SYSCLK must be at least 32 kHz to enable debugging.
3. Based on device characterization data; Not production tested.
4. Does not include internal oscillator or internal regulator supply current.
5. I_{DD} can be estimated for frequencies <= 12 MHz by multiplying the frequency of interest by the frequency sensitivity number for that range. When using these numbers to estimate I_{DD} > 12 MHz, the estimate should be the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: V_{DD} = 2.6 V; F= 20 MHz, I_{DD} = 7.3 mA – (25 MHz – 20 MHz) x 0.184 mA/MHz = 6.38 mA.
6. Idle I_{DD} can be estimated for frequencies <= 1 MHz by multiplying the frequency of interest by the frequency sensitivity number for that range. When using these numbers to estimate I_{DD} > 1 MHz, the estimate should be the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: V_{DD} = 2.6 V; F= 5 MHz, Idle I_{DD} = 3 mA – (25 MHz– 5 MHz) x 118 µA/MHz = 0.64 mA.

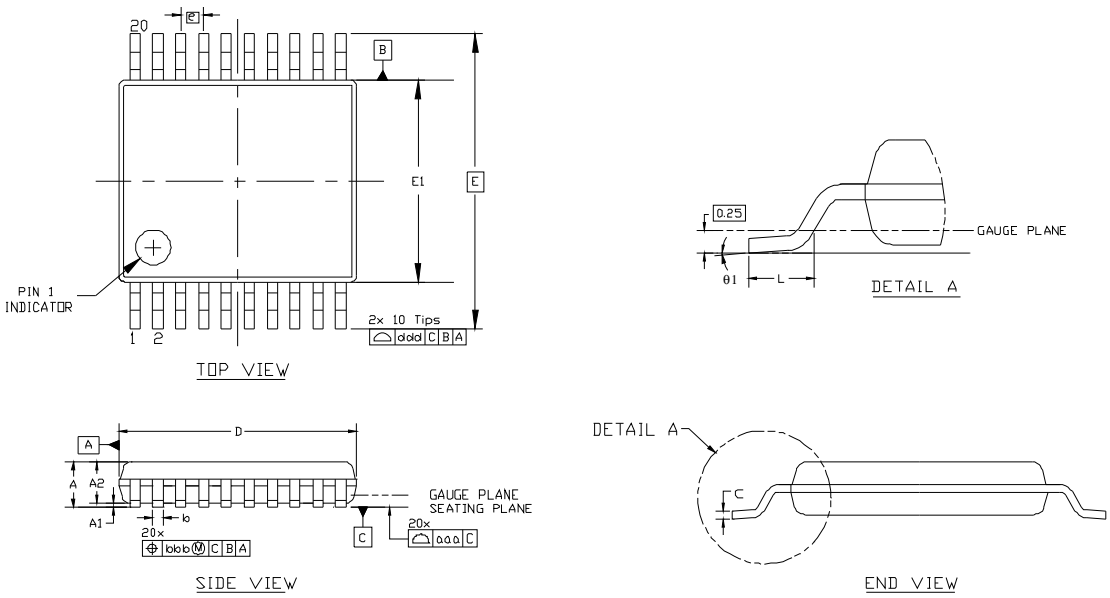


Figure 3.5. TSSOP-20 Package Diagram

Table 3.5. TSSOP-20 Package Diagram Dimensions

Symbol	Min	Nom	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
c	0.09	—	0.20
D	6.40	6.50	6.60
e	0.65 BSC.		
E	6.40 BSC.		
E1	4.30	4.40	4.50
L	0.45	0.60	0.75
θ1	0°	—	8°
aaa	0.10		
bbb	0.10		
ddd	0.20		

Notes:

1. All dimensions shown are in millimeters (mm).
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-153, variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

For example, the initial example in this section requires a gain of 0.44 to convert 5 V full scale to 2.2 V full scale. Using Equation 4.3:

$$GAIN = \left(0.44 - GAINADD \times \left(\frac{1}{64}\right)\right) \times 4096$$

If GAINADD is set to 1, this makes the equation:

$$GAIN = \left(0.44 - 1 \times \left(\frac{1}{64}\right)\right) \times 4096 = 0.424 \times 4096 = 1738 = 0x06CA$$

The actual gain from setting GAINADD to 1 and ADC0GNH and ADC0GNL to 0x6CA is 0.4399. A similar gain can be achieved if GAINADD is set to 0 with a different value for ADC0GNH and ADC0GNL.

4.4.2. Setting the Gain Value

The three programmable gain registers are accessed indirectly using the ADC0H and ADC0L registers when the GAINEN bit (ADC0CF.0) bit is set. ADC0H acts as the address register, and ADC0L is the data register. The programmable gain registers can only be written to and cannot be read. See Gain Register Definition 4.1, Gain Register Definition 4.2, and Gain Register Definition 4.3 for more information.

The gain is programmed using the following steps:

1. Set the GAINEN bit (ADC0CF.0)
2. Load the ADC0H with the ADC0GNH, ADC0GNL, or ADC0GNA address.
3. Load ADC0L with the desired value for the selected gain register.
4. Reset the GAINEN bit (ADC0CF.0)

Notes:

1. An ADC conversion should not be performed while the GAINEN bit is set.
2. Even with gain enabled, the maximum input voltage must be less than V_{REGIN} and the maximum voltage of the signal after gain must be less than or equal to V_{REF}.

In code, changing the value to 0.44 gain from the previous example looks like:

```
// in 'C':
ADC0CF |= 0x01;// GAINEN = 1
ADC0H = 0x04;// Load the ADC0GNH address
ADC0L = 0x6C;// Load the upper byte of 0x6CA to ADC0GNH
ADC0H = 0x07;// Load the ADC0GNL address
ADC0L = 0xA0;// Load the lower nibble of 0x6CA to ADC0GNL
ADC0H = 0x08;// Load the ADC0GNA address
ADC0L = 0x01;// Set the GAINADD bit
ADC0CF &= ~0x01;// GAINEN = 0

; in assembly
ORL ADC0CF,#01H ; GAINEN = 1
MOV ADC0H,#04H; Load the ADC0GNH address
MOV ADC0L,#06CH ; Load the upper byte of 0x6CA to ADC0GNH
MOV ADC0H,#07H; Load the ADC0GNL address
MOV ADC0L,#0A0H ; Load the lower nibble of 0x6CA to ADC0GNL
MOV ADC0H,#08H; Load the ADC0GNA address
MOV ADC0L,#01H ; Set the GAINADD bit
ANL ADC0CF,#0FEH ; GAINEN = 0
```

SFR Definition 4.6. ADC0H: ADC0 Data Word MSB

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xBE

Bits7–0: ADC0 Data Word High-Order Bits.
For AD0LJST = 0 and AD0RPT as follows:
00: Bits 3–0 are the upper 4 bits of the 12-bit result. Bits 7–4 are 0000b.
01: Bits 4–0 are the upper 5 bits of the 14-bit result. Bits 7–5 are 000b.
10: Bits 5–0 are the upper 6 bits of the 15-bit result. Bits 7–6 are 00b.
11: Bits 7–0 are the upper 8 bits of the 16-bit result.
For AD0LJST = 1 (AD0RPT must be '00'): Bits 7–0 are the most-significant bits of the ADC0 12-bit result.

SFR Definition 4.7. ADC0L: ADC0 Data Word LSB

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xBD

Bits7–0: ADC0 Data Word Low-Order Bits.
For AD0LJST = 0: Bits 7–0 are the lower 8 bits of the ADC0 Accumulated Result.
For AD0LJST = 1 (AD0RPT must be '00'): Bits 7–4 are the lower 4 bits of the 12-bit result. Bits 3–0 are 0000b.

4.5. Programmable Window Detector

The ADC Programmable Window Detector continuously compares the ADC0 output registers to user-programmed limits, and notifies the system when a desired condition is detected. This is especially effective in an interrupt-driven system, saving code space and CPU bandwidth while delivering faster system response times. The window detector interrupt flag (AD0WINT in register ADC0CN) can also be used in polled mode. The ADC0 Greater-Than (ADC0GTH, ADC0GTL) and Less-Than (ADC0LTH, ADC0LTL) registers hold the comparison values. The window detector flag can be programmed to indicate when measured data is inside or outside of the user-programmed limits, depending on the contents of the ADC0 Less-Than and ADC0 Greater-Than registers.

SFR Definition 4.10. ADC0GTH: ADC0 Greater-Than Data High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xC4

Bits7–0: High byte of ADC0 Greater-Than Data Word.

SFR Definition 4.11. ADC0GTL: ADC0 Greater-Than Data Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xC3

Bits7–0: Low byte of ADC0 Greater-Than Data Word.

13. Port Input/Output

Digital and analog resources are available through up to 16 I/O pins. Port pins are organized as two or one byte-wide Ports. Each of the Port pins can be defined as general-purpose I/O (GPIO) or analog input/output; Port pins P0.0 - P2.7 can be assigned to one of the internal digital resources as shown in Figure 13.3. The designer has complete control over which functions are assigned, limited only by the number of physical I/O pins. This resource assignment flexibility is achieved through the use of a Priority Crossbar Decoder. Note that the state of a Port I/O pin can always be read in the corresponding Port latch, regardless of the Crossbar settings.

The Crossbar assigns the selected internal digital resources to the I/O pins based on the peripheral priority order of the Priority Decoder (Figure 13.3 and Figure 13.4). The registers XBR0 and XBR1, defined in SFR Definition 13.1 and SFR Definition 13.2, are used to select internal digital functions.

Port I/O pins are 5.25 V tolerant over the operating range of V_{REGIN}. Figure 13.2 shows the Port cell circuit. The Port I/O cells are configured as either push-pull or open-drain in the Port Output Mode registers (PnMDOUT, where n = 0,1). Complete Electrical Specifications for Port I/O are given in Table 2.10 on page 33.

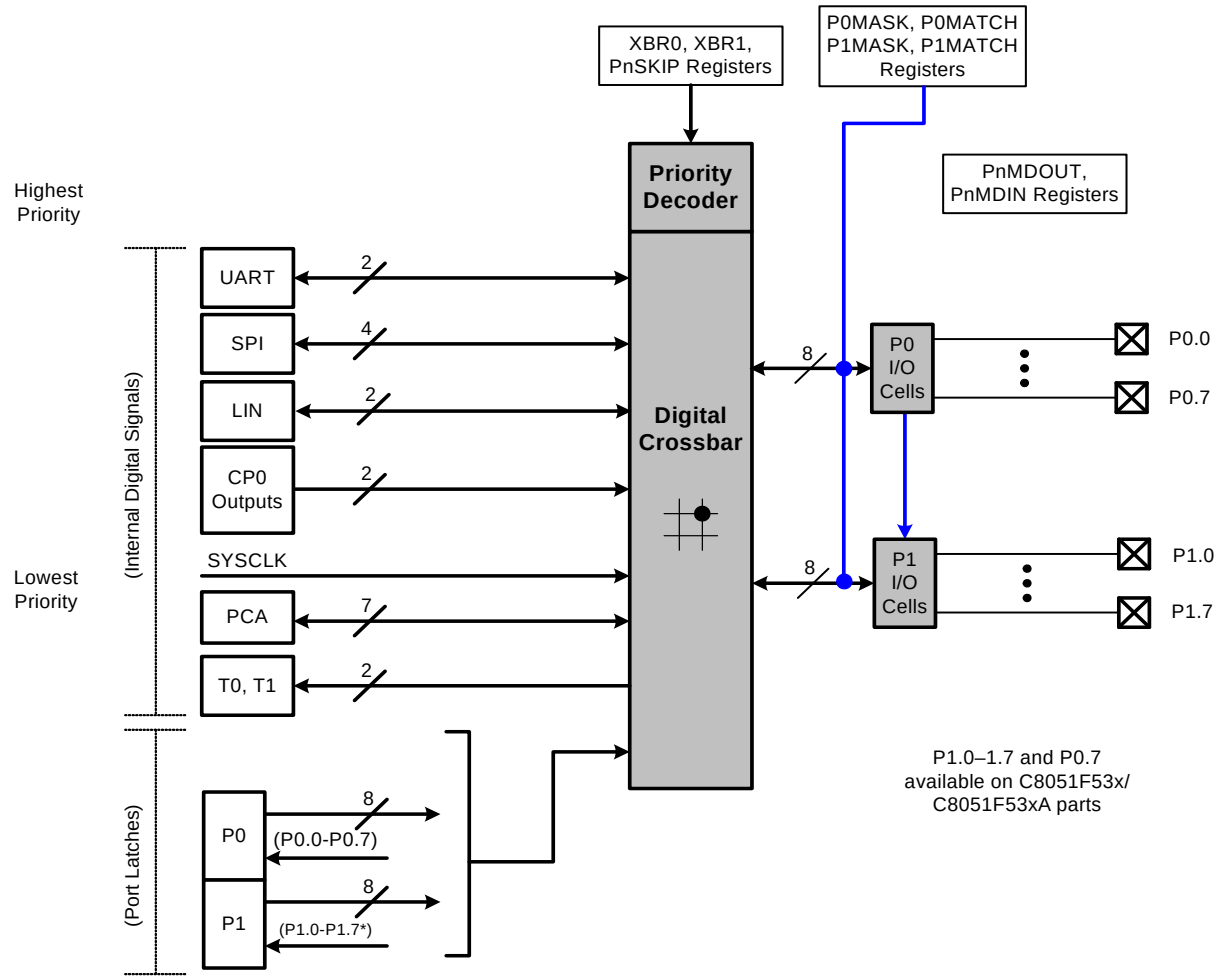
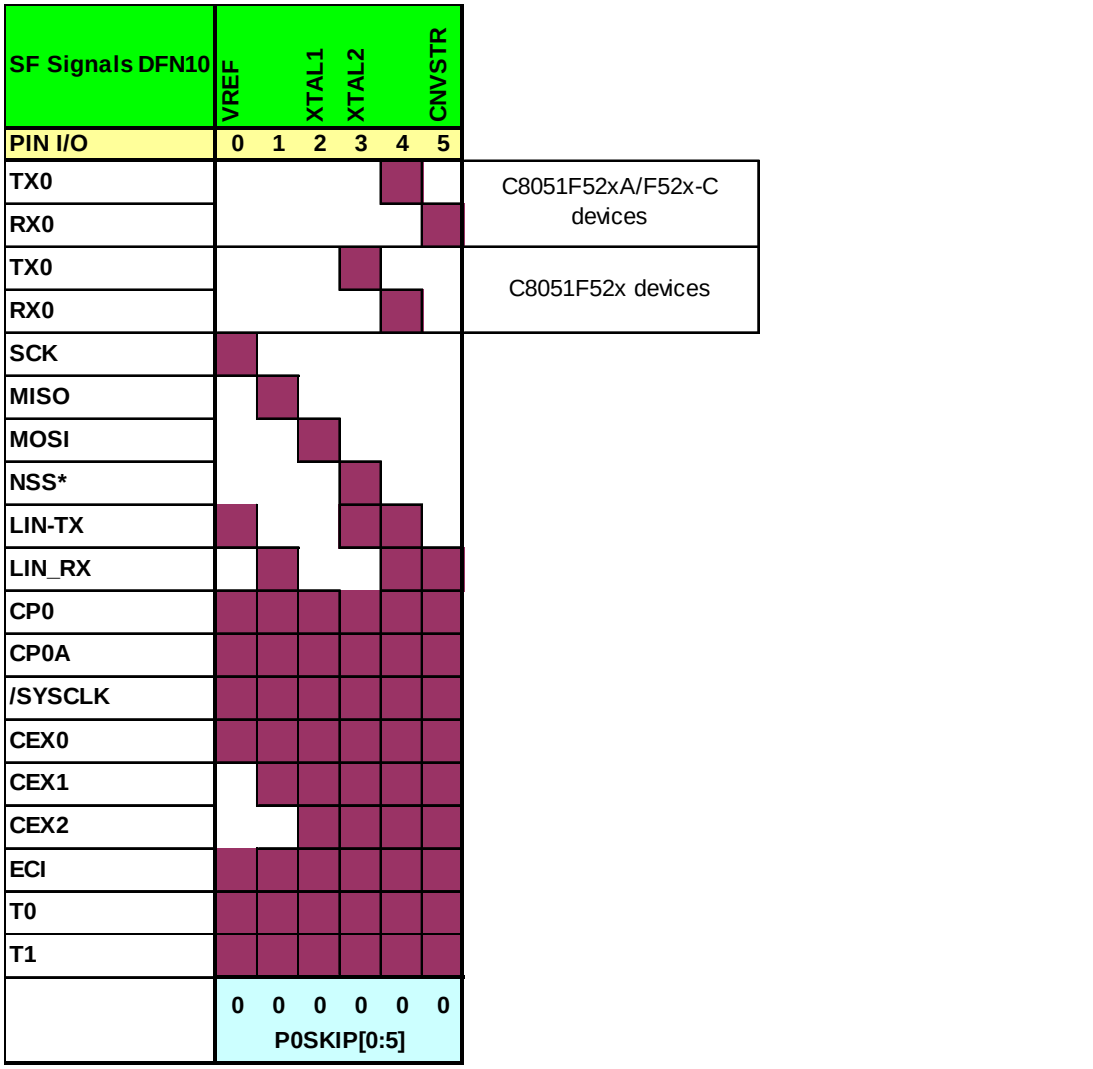


Figure 13.1. Port I/O Functional Block Diagram



Note: 4-Wire SPI Only.

Figure 13.5. Crossbar Priority Decoder with No Pins Skipped (DFN 10)

Important Note: The SPI can be operated in either 3-wire or 4-wire modes, depending on the state of the NSSMD1–NSSMD0 bits in register SPI0CN. According to the SPI mode, the NSS signal may or may not be routed to a Port pin.

13.2. Port I/O Initialization

Port I/O initialization consists of the following steps:

1. Select the input mode (analog or digital) for all Port pins, using the Port Input Mode register (PnMDIN).
2. Select the output mode (open-drain or push-pull) for all Port pins, using the Port Output Mode register (PnMDOUT).
3. Select any pins to be skipped by the I/O Crossbar using the Port Skip registers (PnSKIP).
4. Assign Port pins to desired peripherals using the XBRn registers.
5. Enable the Crossbar (XBARE = 1).

All Port pins must be configured as either analog or digital inputs. Any pins to be used as Comparator or ADC inputs should be configured as an analog inputs. When a pin is configured as an analog input, its weak pullup, digital driver, and digital receiver are disabled. This process saves power and reduces noise on the analog input. Pins configured as digital inputs may still be used by analog peripherals; however, this practice is not recommended.

Additionally, all analog input pins should be configured to be skipped by the Crossbar (accomplished by setting the associated bits in PnSKIP). Port input mode is set in the PnMDIN register, where a 1 indicates a digital input, and a 0 indicates an analog input. All pins default to digital inputs on reset. See SFR Definition 13.4 for the PnMDIN register details.

Important Note: Port 0 and Port 1 pins are 5.25 V tolerant across the operating range of V_{REGIN}.

The output driver characteristics of the I/O pins are defined using the Port Output Mode registers (PnMDOUT). Each Port Output driver can be configured as either open drain or push-pull. This selection is required even for the digital resources selected in the XBRn registers, and is not automatic. When the WEAKPUD bit in XBR1 is 0, a weak pullup is enabled for all Port I/O configured as open-drain. WEAKPUD does not affect the push-pull Port I/O. Furthermore, the weak pullup is turned off on an output that is driving a 0 and for pins configured for analog input mode to avoid unnecessary power dissipation.

Registers XBR0 and XBR1 must be loaded with the appropriate values to select the digital I/O functions required by the design. Setting the XBARE bit in XBR1 to 1 enables the Crossbar. Until the Crossbar is enabled, the external pins remain as standard Port I/O (in input mode), regardless of the XBRn Register settings. For given XBRn Register settings, one can determine the I/O pin-out using the Priority Decode Table.

The Crossbar must be enabled to use Port pins as standard Port I/O in output mode. **Port output drivers are disabled while the Crossbar is disabled.**

16.1. Signal Descriptions

The four signals used by SPI0 (MOSI, MISO, SCK, NSS) are described below.

16.1.1. Master Out, Slave In (MOSI)

The master-out, slave-in (MOSI) signal is an output from a master device and an input to slave devices. It is used to serially transfer data from the master to the slave. This signal is an output when SPI0 is operating as a master and an input when SPI0 is operating as a slave. Data is transferred most-significant bit first. When configured as a master, MOSI is driven by the MSB of the shift register in both 3- and 4-wire mode.

16.1.2. Master In, Slave Out (MISO)

The master-in, slave-out (MISO) signal is an output from a slave device and an input to the master device. It is used to serially transfer data from the slave to the master. This signal is an input when SPI0 is operating as a master and an output when SPI0 is operating as a slave. Data is transferred most-significant bit first. The MISO pin is placed in a high-impedance state when the SPI module is disabled and when the SPI operates in 4-wire mode as a slave that is not selected. When acting as a slave in 3-wire mode, MISO is always driven by the MSB of the shift register.

16.1.3. Serial Clock (SCK)

The serial clock (SCK) signal is an output from the master device and an input to slave devices. It is used to synchronize the transfer of data between the master and slave on the MOSI and MISO lines. SPI0 generates this signal when operating as a master. The SCK signal is ignored by a SPI slave when the slave is not selected (NSS = 1) in 4-wire slave mode.

16.1.4. Slave Select (NSS)

The function of the slave-select (NSS) signal is dependent on the setting of the NSSMD1 and NSSMD0 bits in the SPI0CN register. There are three possible modes that can be selected with these bits:

1. NSSMD[1:0] = 00: 3-Wire Master or 3-Wire Slave Mode: SPI0 operates in 3-wire mode, and NSS is disabled. When operating as a slave device, SPI0 is always selected in 3-wire mode. Since no select signal is present, SPI0 must be the only slave on the bus in 3-wire mode. This is intended for point-to-point communication between a master and one slave.
2. NSSMD[1:0] = 01: 4-Wire Slave or Multi-Master Mode: SPI0 operates in 4-wire mode, and NSS is enabled as an input. When operating as a slave, NSS selects the SPI0 device. When operating as a master, a 1-to-0 transition of the NSS signal disables the master function of SPI0 so that multiple master devices can be used on the same SPI bus.
3. NSSMD[1:0] = 1x: 4-Wire Master Mode: SPI0 operates in 4-wire mode, and NSS is enabled as an output. The setting of NSSMD0 determines what logic level the NSS pin will output. This configuration should only be used when operating SPI0 as a master device.

See Figure 16.2, Figure 16.3, and Figure 16.4 for typical connection diagrams of the various operational modes. **Note that the setting of NSSMD bits affects the pinout of the device.** When in 3-wire master or 3-wire slave mode, the NSS pin will not be mapped by the crossbar. In all other modes, the NSS signal will be mapped to a pin on the device. See Section “13. Port Input/Output” on page 120 for general purpose port I/O and crossbar information.

Table 16.1. SPI Slave Timing Parameters

Parameter	Description	Min	Max	Units
Master Mode Timing* (See Figure 16.6 and Figure 16.7)				
T_{MCKH}	SCK High Time	1 x T_{SYSCLK}	—	ns
T_{MCKL}	SCK Low Time	1 x T_{SYSCLK}	—	ns
T_{MIS}	MISO Valid to SCK Sample Edge	20	—	ns
T_{MIH}	SCK Sample Edge to MISO Change	0	—	ns
Slave Mode Timing* (See Figure 16.8 and Figure 16.9)				
T_{SE}	NSS Falling to First SCK Edge	2 x T_{SYSCLK}	—	ns
T_{SD}	Last SCK Edge to NSS Rising	2 x T_{SYSCLK}	—	ns
T_{SEZ}	NSS Falling to MISO Valid	—	4 x T_{SYSCLK}	ns
T_{SDZ}	NSS Rising to MISO High-Z	—	4 x T_{SYSCLK}	ns
T_{CKH}	SCK High Time	5 x T_{SYSCLK}	—	ns
T_{CKL}	SCK Low Time	5 x T_{SYSCLK}	—	ns
T_{SIS}	MOSI Valid to SCK Sample Edge	2 x T_{SYSCLK}	—	ns
T_{SIH}	SCK Sample Edge to MOSI Change	2 x T_{SYSCLK}	—	ns
T_{SOH}	SCK Shift Edge to MISO Change	—	4 x T_{SYSCLK}	ns

Note: T_{SYSCLK} is equal to one period of the device system clock (SYSCLK) in ns.
The maximum possible frequency of the SPI can be calculated as:
Transmission: SYSCLK/2
Reception: SYSCLK/10

SFR Definition 17.12. LIN0CTRL: LIN0 Control Register

W	W	W	R/W	R/W	R/W	R/W	R/W	Reset Value
STOP	SLEEP	TXRX	DTACK	RSTINT	RSTERR	WUPREQ	STREQ	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Address: 0x08 (indirect)

Bit7: **STOP**: Stop Communication Processing Bit (**slave mode only**).
This bit is to be set by the application to block the processing of the LIN Communications until the next SYNCH BREAK signal. It is used when the application is handling a data request interrupt and cannot use the frame content with the received identifier (always reads 0).

Bit6: **SLEEP**: Sleep Mode Warning.
This bit is to be set by the application to warn the peripheral that a Sleep Mode Frame was received and that the Bus is in sleep mode or if a Bus Idle timeout interrupt is requested. The application must reset it when a Wake-Up interrupt is requested.

Bit5: **TXRX**: Transmit/Receive Selection Bit.
This bit determines if the current frame is a transmit frame or a receive frame.
0: Current frame is a receive operation.
1: Current frame is a transmit operation.

Bit4: **DTACK**: Data acknowledge bit (**slave mode only**).
Set to 1 after handling a data request interrupt to acknowledge the transfer. The bit will automatically be cleared to 0 by the LIN controller.

Bit3: **RSTINT**: Interrupt Reset bit.
This bit always reads as 0.
0: No effect.
1: Reset the LININT bit (LIN0ST.3).

Bit2: **RSTERR**: Error Reset Bit.
This bit always reads as 0.
0: No effect.
1: Reset the error bits in LIN0ST and LIN0ERR.

Bit1: **WUPREQ**: Wake-Up Request Bit.
Set to 1 to terminate sleep mode by sending a wakeup signal. The bit will automatically be cleared to 0 by the LIN controller.

Bit0: **STREQ**: Start Request Bit (**master mode only**).
1: Start a LIN transmission. This should be set only after loading the identifier, data length and data buffer if necessary.
The bit is reset to 0 upon transmission completion or error detection.

18.1.4. Mode 3: Two 8-bit Counter/Timers (Timer 0 Only)

In Mode 3, Timer 0 is configured as two separate 8-bit counter/timers held in TL0 and TH0. The counter/timer in TL0 is controlled using the Timer 0 control/status bits in TCON and TMOD: TR0, C/T0, GATE0 and TF0. TL0 can use either the system clock or an external input signal as its timebase. The TH0 register is restricted to a timer function sourced by the system clock or prescaled clock. TH0 is enabled using the Timer 1 run control bit TR1. TH0 sets the Timer 1 overflow flag TF1 on overflow and thus controls the Timer 1 interrupt.

Timer 1 is inactive in Mode 3. When Timer 0 is operating in Mode 3, Timer 1 can be operated in Modes 0, 1 or 2, but cannot be clocked by external signals nor set the TF1 flag and generate an interrupt. However, the Timer 1 overflow can be used to generate baud rates for the SMBus and UART. While Timer 0 is operating in Mode 3, Timer 1 run control is handled through its mode settings. To run Timer 1 while Timer 0 is in Mode 3, set the Timer 1 Mode as 0, 1, or 2. To disable Timer 1, configure it for Mode 3.

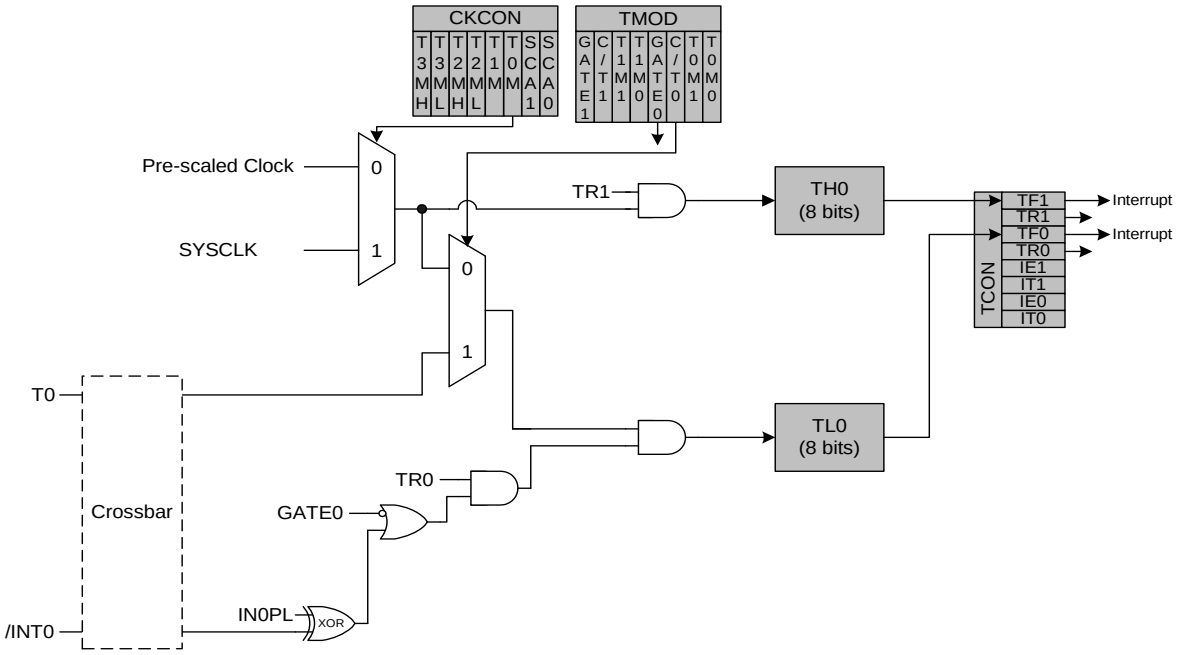


Figure 18.3. T0 Mode 3 Block Diagram

SFR Definition 18.2. TMOD: Timer Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
GATE1	C/T1	T1M1	T1M0	GATE0	C/T0	T0M1	T0M0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
							SFR Address:	0x89

Bit7: **GATE1**: Timer 1 Gate Control.
0: Timer 1 enabled when TR1 = 1 irrespective of $\overline{\text{INT0}}$ logic level.
1: Timer 1 enabled only when TR1 = 1 AND $\overline{\text{INT0}}$ is active as defined by bit IN1PL in register IT01CF (see SFR Definition 10.5. “IT01CF: INT0/INT1 Configuration” on page 105).

Bit6: **C/T1**: Counter/Timer 1 Select.
0: Timer Function: Timer 1 incremented by clock defined by T1M bit (CKCON.4).
1: Counter Function: Timer 1 incremented by high-to-low transitions on external input pin (T1).

Bits5–4: **T1M1–T1M0**: Timer 1 Mode Select.
These bits select the Timer 1 operation mode.

T1M1	T1M0	Mode
0	0	Mode 0: 13-bit counter/timer
0	1	Mode 1: 16-bit counter/timer
1	0	Mode 2: 8-bit counter/timer with auto-reload
1	1	Mode 3: Timer 1 inactive

Bit3: **GATE0**: Timer 0 Gate Control.
0: Timer 0 enabled when TR0 = 1 irrespective of $\overline{\text{INT0}}$ logic level.
1: Timer 0 enabled only when TR0 = 1 AND $\overline{\text{INT0}}$ is active as defined by bit IN0PL in register IT01CF (see SFR Definition 10.5. “IT01CF: INT0/INT1 Configuration” on page 105).

Bit2: **C/T0**: Counter/Timer Select.
0: Timer Function: Timer 0 incremented by clock defined by T0M bit (CKCON.3).
1: Counter Function: Timer 0 incremented by high-to-low transitions on external input pin (T0).

Bits1–0: **T0M1–T0M0**: Timer 0 Mode Select.
These bits select the Timer 0 operation mode.

T0M1	T0M0	Mode
0	0	Mode 0: 13-bit counter/timer
0	1	Mode 1: 16-bit counter/timer
1	0	Mode 2: 8-bit counter/timer with auto-reload
1	1	Mode 3: Two 8-bit counter/timers

19.2.4. Frequency Output Mode

Frequency Output Mode produces a programmable-frequency square wave on the module's associated CEXn pin. The capture/compare module high byte holds the number of PCA clocks to count before the output is toggled. The frequency of the square wave is then defined by Equation 19.1.

$$F_{CEXn} = \frac{F_{PCA}}{2 \times PCA0CPHn}$$

Note: A value of 0x00 in the PCA0CPHn register is equal to 256 for this equation.

Equation 19.1. Square Wave Frequency Output

Where F_{PCA} is the frequency of the clock selected by the CPS2-0 bits in the PCA mode register, PCA0MD. The lower byte of the capture/compare module is compared to the PCA counter low byte; on a match, CEXn is toggled and the offset held in the high byte is added to the matched value in PCA0CPLn. Frequency Output Mode is enabled by setting the ECOMn, TOGn, and PWMn bits in the PCA0CPMn register.

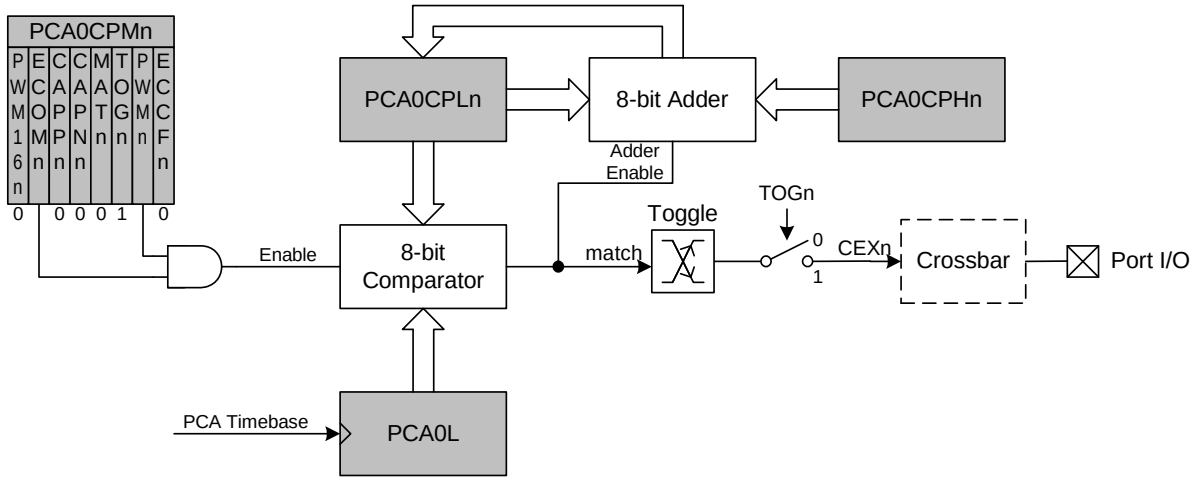


Figure 19.7. PCA Frequency Output Mode

19.3.1. Watchdog Timer Operation

While the WDT is enabled:

- PCA counter is forced on.
- Writes to PCA0L and PCA0H are not allowed.
- PCA clock source bits (CPS2-CPS0) are frozen.
- PCA Idle control bit (CIDL) is frozen.
- Module 2 is forced into software timer mode.
- Writes to the Module 2 mode register (PCA0CPM2) are disabled.

While the WDT is enabled, writes to the CR bit will not change the PCA counter state; the counter will run until the WDT is disabled. The PCA counter run control (CR) will read zero if the WDT is enabled but user software has not enabled the PCA counter. If a match occurs between PCA0CPH2 and PCA0H while the WDT is enabled, a reset will be generated. To prevent a WDT reset, the WDT may be updated with a write of any value to PCA0CPH2. Upon a PCA0CPH2 write, PCA0H plus the offset held in PCA0CPL2 is loaded into PCA0CPH2 (See Figure 19.10).

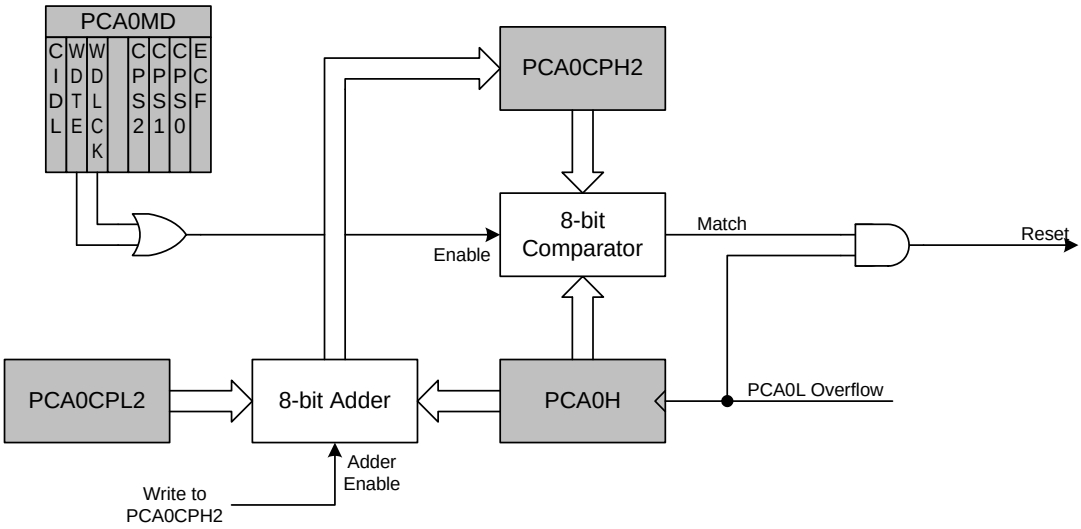


Figure 19.10. PCA Module 2 with Watchdog Timer Enabled

Note that the 8-bit offset held in PCA0CPH2 is compared to the upper byte of the 16-bit PCA counter. This offset value is the number of PCA0L overflows before a reset. Up to 256 PCA clocks may pass before the first PCA0L overflow occurs, depending on the value of the PCA0L when the update is performed. The total offset is then given (in PCA clocks) by Equation 19.4, where PCA0L is the value of the PCA0L register at the time of the update.

$$Offset = (256 \times PCA0CPL2) + (256 - PCA0L)$$

Equation 19.4. Watchdog Timer Offset in PCA Clocks

The WDT reset is generated when PCA0L overflows while there is a match between PCA0CPH2 and PCA0H. Software may force a WDT reset by writing a 1 to the CCF2 flag (PCA0CN.2) while the WDT is enabled.

C2 Register Definition 21.3. REVID: C2 Revision ID

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Reset Value
								Varies

This read-only register returns the 8-bit revision ID.
For example, 0x00 = Revision A.

C2 Register Definition 21.4. FPCTL: C2 Flash Programming Control

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Reset Value
								00000000

Bits7–0 **FPCTL**: Flash Programming Control Register.
This register is used to enable Flash programming via the C2 interface. To enable C2 Flash programming, the following codes must be written in order: 0x02, 0x01. Note that once C2 Flash programming is enabled, a system reset must be issued to resume normal operation.

C2 Register Definition 21.5. FPDAT: C2 Flash Programming Data

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Reset Value
								00000000

Bits7–0: **FPDAT**: C2 Flash Programming Data Register.
This register is used to pass Flash commands, addresses, and data during C2 Flash accesses. Valid commands are listed below.

Code	Command
0x06	Flash Block Read
0x07	Flash Block Write
0x08	Flash Page Erase
0x03	Device Erase

Document Change List

Revision 0.3 to 0.4

- Updated all specification tables.
- Added 'F52xA and 'F53xA information.
- Updated the Selectable Gain section in the ADC section.
- Updated the External Crystal Example in the Oscillators section.
- Updated the LIN section.

Revision 0.4 to 0.5

- Updated all specification tables.
- Updated Figures 1.1, 1.2, 1.3, and 1.4.
- Updated Section 4 pinout diagrams and tables.

Revision 0.5 to 1.0

- Updated all specification tables and moved them to one section.
- Added Figure 3.1 and Figure 3.2.
- Updated Section 4 pinout diagrams and tables.
- Updated Figure 5.6.
- Added Figure 15.3.
- Updated equations in Section 17.
- Updated Figure 21.3.

Revision 1.0 to 1.1

- Updated Table 2.3, “ADC0 Electrical Characteristics,” on page 28 with new Burst Mode Oscillator specification, new Power Supply Current maximum, and made corrections to Temperature Sensor Offset and Offset Error conditions.
- Updated Table 2.9, “Flash Electrical Characteristics,” on page 33 with new Flash Write and Erase timing.
- Made correction in Equivalent Gain table in Section “4.4. Selectable Gain” on page 60.
- Updated Section “11.2. Power-Fail Reset / VDD Monitors (VDDMON0 and VDDMON1)” on page 108 regarding higher V_{DD} monitor threshold.

Revision 1.1 to 1.2

- Updated “Ordering Information” on page 14 and Table 1.1, “Product Selection Guide (Recommended for New Designs),” on page 14 to include -A (Automotive) devices and automotive qualification information.
- Updated Table 2.3, “ADC0 Electrical Characteristics,” on page 28 to include Temperature Sensor tracking time requirement and update INL maximum specification.
- Updated Figure 3.2. ’DFN-10 Package Diagram’ on page 38 with new Pin-1 detail drawing.
- Updated Table 8.1, “CIP-51 Instruction Set Summary,” on page 83 with correct CJNE and CPL timing.
- Updated “Power-Fail Reset / VDD Monitors (VDDMON0 and VDDMON1)” on page 108 to clarify the recommendations for the VDD monitor.

Note: All items from the C8051F52xA-F53xA Errata dated August 26, 2009 are incorporated into this data sheet.

- Replaced minimum VDD value for Flash write/erase operations in Table 2.9 on page 33 with references to the $V_{RST-HIGH}$ theshold specified in Table 2.8 on page 32.
- Removed Output Low Voltage values for condition 'V_{REGIN} = 1.8 V' from Table 2.10, "Port I/O DC Electrical Characteristics," on page 33.
- Corrected minor typo ("IFCN = 111b") in Table 2.11, "Internal Oscillator Electrical Characteristics," on page 34.
- Removed the typical value and added the maximum value for the 'Wake-up Time From Suspend' specification with the 'ZTCEN = 0' condition in Table 2.11, "Internal Oscillator Electrical Characteristics," on page 34.
- Added Internal Oscillator Supply current values at specific temperatures for conditions 'ZTCEN = 1' and 'ZTCEN = 0' in Table 2.11, "Internal Oscillator Electrical Characteristics," on page 34. Also updated the table name to clarify that the specifications apply to the internal oscillator.
- Updated Section "1.1. Ordering Information" on page 14 and Table 1.1 with new C8051F52x-C/F53x-C part numbers.
- Updated Table 1.2, "Product Selection Guide (Not Recommended for New Designs)," on page 15 to include C8051F52xA/F53xA part numbers.
- Updated Figure 1.1, Figure 1.2, Figure 1.3, and Figure 1.4 titles to clarify applicable silicon revisions.
- Added figure references to pinout diagrams (Figure 3.1, Figure 3.4, and Figure 3.7) and updated labels to clarify applicable part numbers.
- Updated Table 3.1, Table 3.4, and Table 3.7 to indicate pinouts applicable to C8051F52x-C/F53x-C devices.
- Added note in Section "6. Voltage Regulator (REG0)" on page 74 to indicate the need for bypass capacitors for voltage regulator stability.
- Updated Figure 11.1 on Page 106 and text in Section "11.1. Power-On Reset" on page 107 and Section "11.2. Power-Fail Reset / VDD Monitors (VDDMON0 and VDDMON1)" on page 108 to describe the new level-sensitive V_{DD} monitor (VDDMON1).
- Updated SFR Definition 11.1. "VDDMON: VDD Monitor Control" on page 109 to include the VDM1EN bit (bit 4) that controls the new level-sensitive V_{DD} monitor (VDDMON1).
- Added notes in Section 11.1 on page 107, Section 11.2 on page 108, and Section 11.3 on page 110 with references to relevant parts of Section "20. Device Specific Behavior" on page 210.
- Moved some notes related to VDD Monitor (VDDMON0) High Threshold setting ($V_{RST-HIGH}$) from Section 11.2 on page 108 to Section 20.5 on page 212 in Section "20. Device Specific Behavior".
- Added Section "11.2.1. VDD Monitor Thresholds and Minimum VDD" on page 108 to describe the recommendations for minimum V_{DD} as it relates to the V_{DD} monitor thresholds.
- Clarified text in Section "11.7. Flash Error Reset" on page 110.
- Clarified text in items 2, 3 and 4 in Section "12.2.1. V_{DD} Maintenance and the V_{DD} monitor" on page 115 to reference appropriate specification tables and specify "VDDMON0".