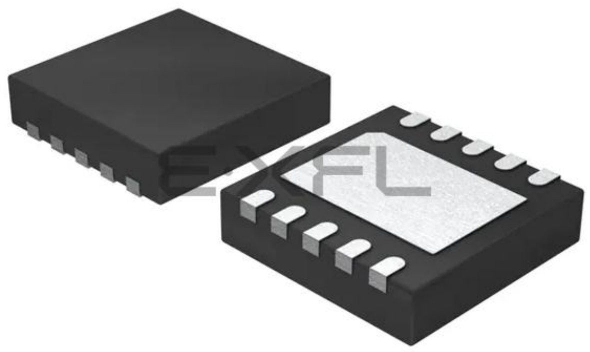

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	6
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.25V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	10-VFDFN Exposed Pad
Supplier Device Package	10-DFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f527-c-imr

1.6. Programmable Comparator

C8051F52x/F52xA/F53x/F53xA devices include a software-configurable voltage comparator with an input multiplexer. The comparator offers programmable response time and hysteresis and an output that is optionally available at the Port pins: a synchronous "latched" output (CP0). The comparator interrupt may be generated on rising, falling, or both edges. When in IDLE or SUSPEND mode, these interrupts may be used as a "wake-up" source for the processor. The Comparator may also be configured as a reset source. A block diagram of the comparator is shown in Figure 1.8.

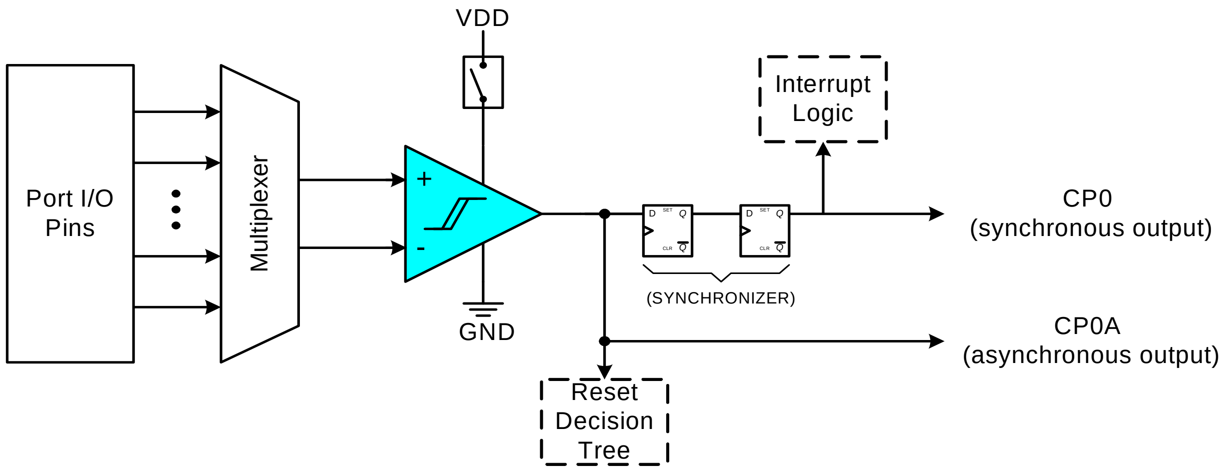


Figure 1.8. Comparator Block Diagram

1.7. Voltage Regulator

C8051F52x/F52xA/F53x/F53xA devices include an on-chip low dropout voltage regulator (REG0). The input to REG0 at the V_{REGIN} pin can be as high as 5.25 V. The output can be selected by software to 2.1 or 2.6 V. When enabled, the output of REG0 powers the device and drives the V_{DD} pin. The voltage regulator can be used to power external devices connected to V_{DD}.

1.8. Serial Port

The C8051F52x/F52xA/F53x/F53xA family includes a full-duplex UART with enhanced baud rate configuration, and an Enhanced SPI interface. Each of the serial buses is fully implemented in hardware and makes extensive use of the CIP-51's interrupts, thus requiring very little CPU intervention.

2.2. Electrical Characteristics

Table 2.2. Global DC Electrical Characteristics

–40 to +125 °C, 25 MHz System Clock unless otherwise specified. Typical values are given at 25 °C

Parameter	Conditions	Min	Typ	Max	Units
Supply Input Voltage (V_{REGIN})[1]	Output Current ≤ 1 mA C8051F52x/53x C8051F52xA/53xA C8051F52x-C/53x-C	 2.7 1.8[1] 2.0[1]	 — — —	 5.25 5.25 5.25	 V V V
Digital Supply Voltage (V_{DD})	C8051F52x/53x C8051F52xA/53xA C8051F52x-C/53x-C	2.0 1.8 2.0	— — —	2.7 2.7 2.75	V V V
Core Supply RAM Data Retention Voltage		—	1.5	—	V
SYSCLK (System Clock)[2]		0	—	25	MHz
Specified Operating Temperature Range		–40	—	+125	°C
Digital Supply Current—CPU Active (Normal Mode, fetching instructions from Flash)					
I_{DD}[3,4]	**V_{DD} = 2.1 V:** Clock = 32 kHz Clock = 200 kHz Clock = 1 MHz Clock = 25 MHz **V_{DD} = 2.6 V:** Clock = 32 kHz Clock = 200 kHz Clock = 1 MHz Clock = 25 MHz	 — — — — — — — —	 13 60 0.28 5.1 22 105 0.5 7.3	 — — — 9 — — — 13	 µA µA mA mA µA µA mA mA
I_{DD} Frequency Sensitivity[3,5]	T = 25 °C: V_{DD} = 2.1 V, F ≤ 12 MHz V_{DD} = 2.1 V, F > 12 MHz V_{DD} = 2.6 V, F ≤ 12 MHz V_{DD} = 2.6 V, F > 12 MHz	 — — — —	 0.276 0.140 0.424 0.184	 — — — —	 mA/MHz mA/MHz mA/MHz mA/MHz

Notes:
1. For more information on V_{REGIN} characteristics, see Table 2.6 on page 30.
2. SYSCLK must be at least 32 kHz to enable debugging.
3. Based on device characterization data; Not production tested.
4. Does not include internal oscillator or internal regulator supply current.
5. I_{DD} can be estimated for frequencies <= 12 MHz by multiplying the frequency of interest by the frequency sensitivity number for that range. When using these numbers to estimate I_{DD} > 12 MHz, the estimate should be the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: V_{DD} = 2.6 V; F= 20 MHz, I_{DD} = 7.3 mA – (25 MHz – 20 MHz) x 0.184 mA/MHz = 6.38 mA.
6. Idle I_{DD} can be estimated for frequencies <= 1 MHz by multiplying the frequency of interest by the frequency sensitivity number for that range. When using these numbers to estimate I_{DD} > 1 MHz, the estimate should be the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: V_{DD} = 2.6 V; F= 5 MHz, Idle I_{DD} = 3 mA – (25 MHz– 5 MHz) x 118 µA/MHz = 0.64 mA.

Table 2.2. Global DC Electrical Characteristics

–40 to +125 °C, 25 MHz System Clock unless otherwise specified. Typical values are given at 25 °C

Parameter	Conditions	Min	Typ	Max	Units
Digital Supply Current—CPU Inactive (Idle Mode, not fetching instructions from Flash)					
Idle I_{DD}[3,4]	**V_{DD} = 2.1 V:**				
	Clock = 32 kHz	—	8	—	µA
	Clock = 200 kHz	—	22	—	µA
	Clock = 1 MHz	—	0.09	—	mA
	Clock = 25 MHz	—	2.2	5	mA
	V_{DD} = 2.6 V:				
	Clock = 32 kHz	—	9	—	µA
	Clock = 200 kHz	—	30	—	µA
	Clock = 1 MHz	—	0.13	—	mA
	Clock = 25 MHz	—	3	6.5	mA
Idle I_{DD} Frequency Sensitivity[3,6]	T = 25 °C:				
	V_{DD} = 2.1 V, F $\leq$ 1 MHz	—	90	—	µA/MHz
	V_{DD} = 2.1 V, F > 1 MHz	—	90	—	µA/MHz
	V_{DD} = 2.6 V, F $\leq$ 1 MHz	—	118	—	µA/MHz
	V_{DD} = 2.6 V, F > 1 MHz	—	118	—	µA/MHz
Digital Supply Current[3] (Stop or Suspend Mode)	Oscillator not running, V_{DD} Monitor Disabled.				
	T = 25 °C	—	2	—	µA
	T = 60 °C	—	3	—	µA
	T = 125 °C	—	50	—	µA

Notes:

1. For more information on V_{REGIN} characteristics, see Table 2.6 on page 30.
2. SYSCLK must be at least 32 kHz to enable debugging.
3. Based on device characterization data; Not production tested.
4. Does not include internal oscillator or internal regulator supply current.
5. I_{DD} can be estimated for frequencies <= 12 MHz by multiplying the frequency of interest by the frequency sensitivity number for that range. When using these numbers to estimate I_{DD} > 12 MHz, the estimate should be the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: V_{DD} = 2.6 V; F= 20 MHz, I_{DD} = 7.3 mA – (25 MHz – 20 MHz) x 0.184 mA/MHz = 6.38 mA.
6. Idle I_{DD} can be estimated for frequencies <= 1 MHz by multiplying the frequency of interest by the frequency sensitivity number for that range. When using these numbers to estimate I_{DD} > 1 MHz, the estimate should be the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: V_{DD} = 2.6 V; F= 5 MHz, Idle I_{DD} = 3 mA – (25 MHz– 5 MHz) x 118 µA/MHz = 0.64 mA.

Table 3.4. Pin Definitions for the C8051F53x and C805153xA (TSSOP 20) (Continued)

Name	Pin Numbers		Type	Description
	‘F53xA ‘F53x-C	‘F53x		
V_{REGIN}	7	7		On-Chip Voltage Regulator Input.
P1.7	8	8	D I/O or A In	Port 1.7. See Port I/O Section for a complete description.
P1.6	9	9	D I/O or A In	Port 1.6. See Port I/O Section for a complete description.
P1.5	10	10	D I/O or A In	Port 1.5. See Port I/O Section for a complete description.
P1.4	11	11	D I/O or A In	Port 1.4. See Port I/O Section for a complete description.
P1.3	12	12	D I/O or A In	Port 1.3. See Port I/O Section for a complete description.
P1.2/ CNVSTR	13	13	D I/O or A In D In	Port 1.2. See Port I/O Section for a complete description. External Converter start input for the ADC0, see Section “4. 12-Bit ADC (ADC0)” on page 52 for a complete description.
P1.1	14	14	D I/O or A In	Port 1.1. See Port I/O Section for a complete description.
P1.0/ XTAL2	15	15	D I/O or A In D I/O	Port 1.0. See Port I/O Section for a complete description. External Clock Output. For an external crystal or resonator, this pin is the excitation driver. This pin is the external clock input for CMOS, capacitor, or RC oscillator configurations. See Section “14. Oscillators” on page 135.
P0.7/ XTAL1	16	16	D I/O or A In A In	Port 0.7. See Port I/O Section for a complete description. External Clock Input. This pin is the external oscillator return for a crystal or resonator. Section “14. Oscillators” on page 135.
P0.6/ C2D	17	17	D I/O or A In D I/O	Port 0.6. See Port I/O Section for a complete description. Bi-directional data signal for the C2 Debug Interface.
P0.5/RX*	18	—	D I/O or A In	Port 0.5. See Port I/O Section for a complete description.
P0.5	—	18	D I/O or A In	Port 0.5. See Port I/O Section for a complete description.

***Note:** Please refer to Section “20. Device Specific Behavior” on page 210.

4.2. Temperature Sensor

An on-chip temperature sensor is included on the C8051F52x/F52xA/F53x/F53xA devices which can be directly accessed via the ADC0 multiplexer. To use ADC0 to measure the temperature sensor, the ADC multiplexer channel should be configured to connect to the temperature sensor. The temperature sensor transfer function is shown in Figure 5.2. The output voltage (V_{TEMP}) is the positive ADC input selected by bits AD0MX[4:0] in register ADC0MX. The TEMPE bit in register REF0CN enables/disables the temperature sensor, as described in SFR Definition 5.1. While disabled, the temperature sensor defaults to a high impedance state and any ADC measurements performed on the sensor will result in meaningless data. Refer to Table 5.1 for the slope and offset parameters of the temperature sensor.

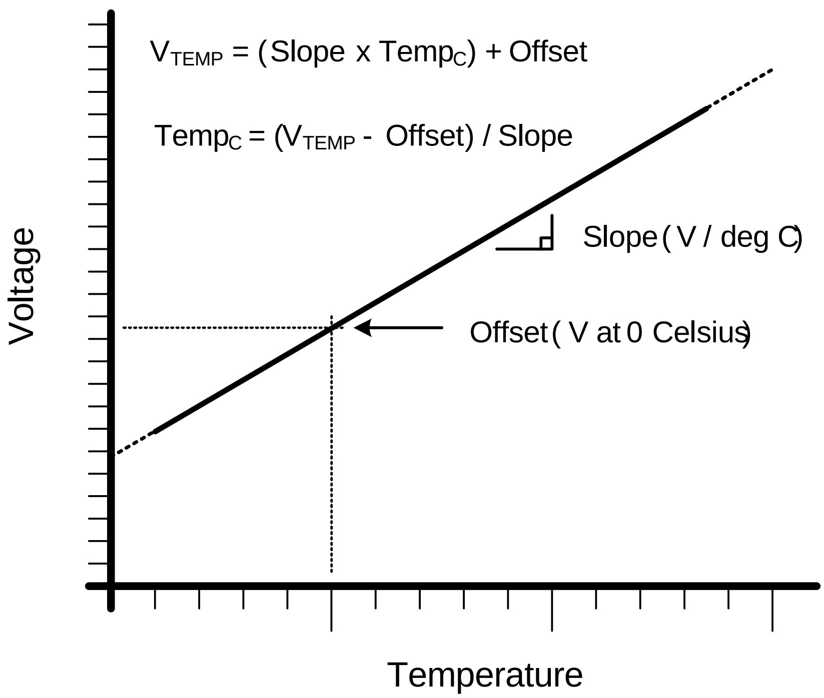


Figure 4.2. Typical Temperature Sensor Transfer Function

4.3. ADC0 Operation

In a typical system, ADC0 is configured using the following steps:

1. If a gain adjustment is required, refer to Section "4.4. Selectable Gain" on page 60.
2. Choose the start of conversion source.
3. Choose Normal Mode or Burst Mode operation.
4. If Burst Mode, choose the ADC0 Idle Power State and set the Power-Up Time.
5. Choose the tracking mode. Note that Pre-Tracking Mode can only be used with Normal Mode.
6. Calculate required settling time and set the post convert-start tracking time using the AD0TK bits.
7. Choose the repeat count.
8. Choose the output word justification (Right-Justified or Left-Justified).
9. Enable or disable the End of Conversion and Window Comparator Interrupts.

4.3.1. Starting a Conversion

A conversion can be initiated in one of four ways, depending on the programmed states of the ADC0 Start of Conversion Mode bits (AD0CM1–0) in register ADC0CN. Conversions may be initiated by one of the following:

- Writing a 1 to the AD0BUSY bit of register ADC0CN
- A rising edge on the CNVSTR input signal (pin P0.6)
- A Timer 1 overflow (i.e., timed continuous conversions)
- A Timer 2 overflow (i.e., timed continuous conversions)

Writing a 1 to AD0BUSY provides software control of ADC0 whereby conversions are performed "on-demand." During conversion, the AD0BUSY bit is set to logic 1 and reset to logic 0 when the conversion is complete. The falling edge of AD0BUSY triggers an interrupt (when enabled) and sets the ADC0 interrupt flag (AD0INT). Note: When polling for ADC conversion completions, the ADC0 interrupt flag (AD0INT) should be used. Converted data is available in the ADC0 data registers, ADC0H:ADC0L, when bit AD0INT is logic 1. Note that when Timer 2 overflows are used as the conversion source, Low Byte overflows are used if Timer2 is in 8-bit mode; High byte overflows are used if Timer 2 is in 16-bit mode. See Section "18. Timers" on page 182 for timer configuration.

Important Note: The CNVSTR input pin also functions as Port pin P0.5 on C8051F52x/52xA devices and P1.2 on C8051F53x/53xA devices. When the CNVSTR input is used as the ADC0 conversion source, Port pin P0.5 or P1.2 should be skipped by the Digital Crossbar. To configure the Crossbar to skip P0.5 or P1.2, set to 1 to the appropriate bit in the PnSKIP register. See Section "13. Port Input/Output" on page 120 for details on Port I/O configuration.

4.3.2. Tracking Modes

Each ADC0 conversion must be preceded by a minimum tracking time for the converted result to be accurate, as shown in Table 2.3 on page 28. ADC0 has three tracking modes: Pre-Tracking, Post-Tracking, and Dual-Tracking. Pre-Tracking Mode provides the minimum delay between the convert start signal and end of conversion by tracking continuously before the convert start signal. This mode requires software management in order to meet minimum tracking requirements. In Post-Tracking Mode, a programmable tracking time starts after the convert start signal and is managed by hardware. Dual-Tracking Mode maximizes tracking time by tracking before and after the convert start signal. Figure 4.3 shows examples of the three tracking modes.

Pre-Tracking Mode is selected when AD0TM is set to 10b. Conversions are started immediately following the convert start signal. ADC0 is tracking continuously when not performing a conversion. Software must allow at least the minimum tracking time between each end of conversion and the next convert start signal. The minimum tracking time must also be met prior to the first convert start signal after ADC0 is enabled.

4.5.1. Window Detector In Single-Ended Mode

Figure 4.7 shows two example window comparisons for right-justified data with ADC0LTH:ADC0LTL = 0x0200 (512d) and ADC0GTH:ADC0GTL = 0x0100 (256d). The input voltage can range from 0 to V_{REF} x (4095/4096) with respect to GND, and is represented by a 12-bit unsigned integer value. The repeat count is set to one. In the left example, an AD0WINT interrupt will be generated if the ADC0 conversion word (ADC0H:ADC0L) is within the range defined by ADC0GTH:ADC0GTL and ADC0LTH:ADC0LTL (if 0x0100 < ADC0H:ADC0L < 0x0200). In the right example, and AD0WINT interrupt will be generated if the ADC0 conversion word is outside of the range defined by the ADC0GT and ADC0LT registers (if ADC0H:ADC0L < 0x0100 or ADC0H:ADC0L > 0x0200). Figure 4.8 shows an example using left-justified data with the same comparison values.

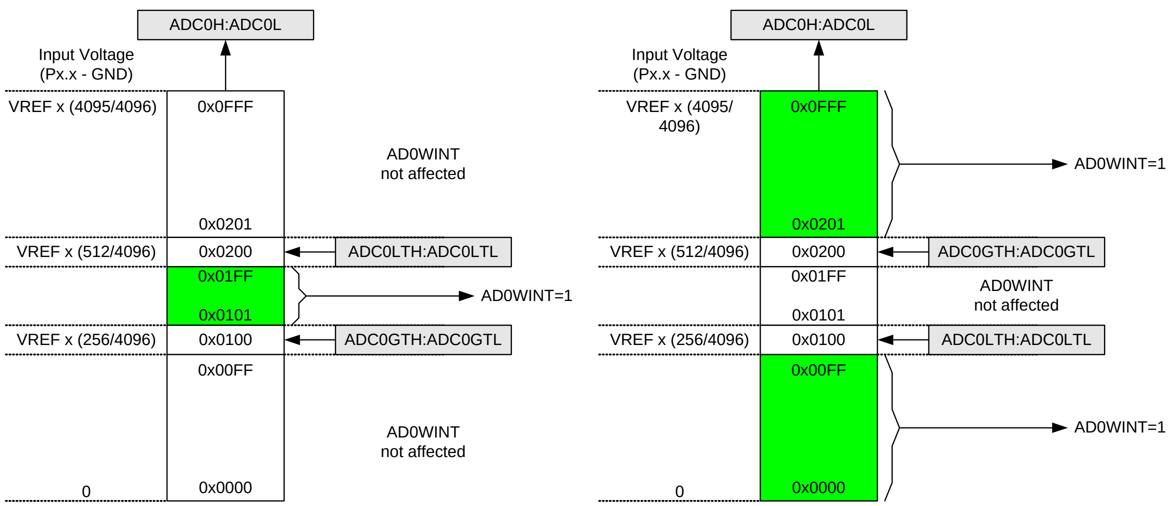


Figure 4.7. ADC Window Compare Example: Right-Justified Single-Ended Data

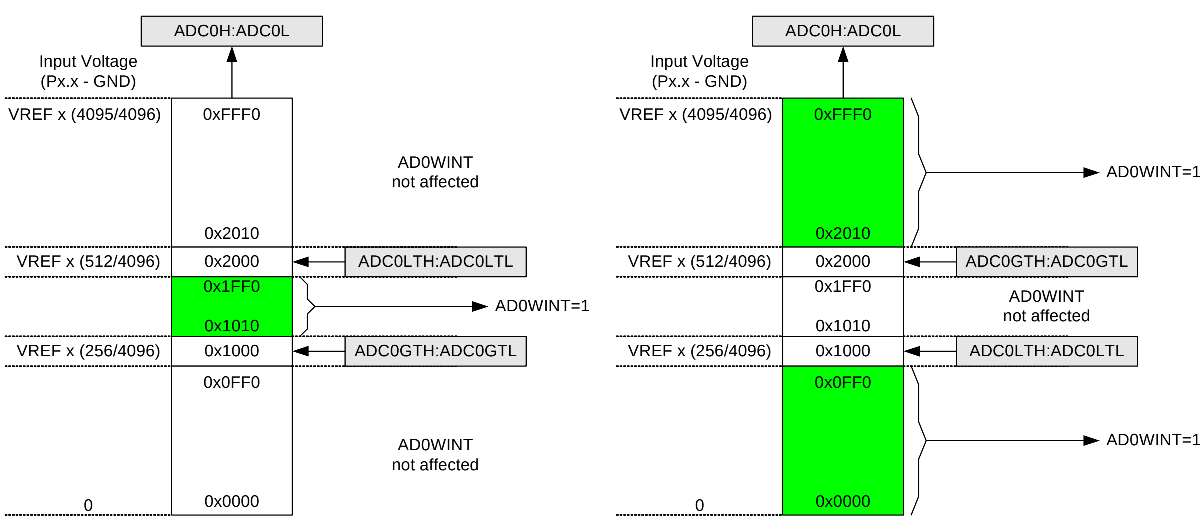


Figure 4.8. ADC Window Compare Example: Left-Justified Single-Ended Data

9. Memory Organization and SFRs

The memory organization of the C8051F52x/F52xA/F53x/F53xA is similar to that of a standard 8051. There are two separate memory spaces: program memory and data memory. Program and data memory share the same address space but are accessed via different instruction types. The memory map is shown in Figure 9.1.

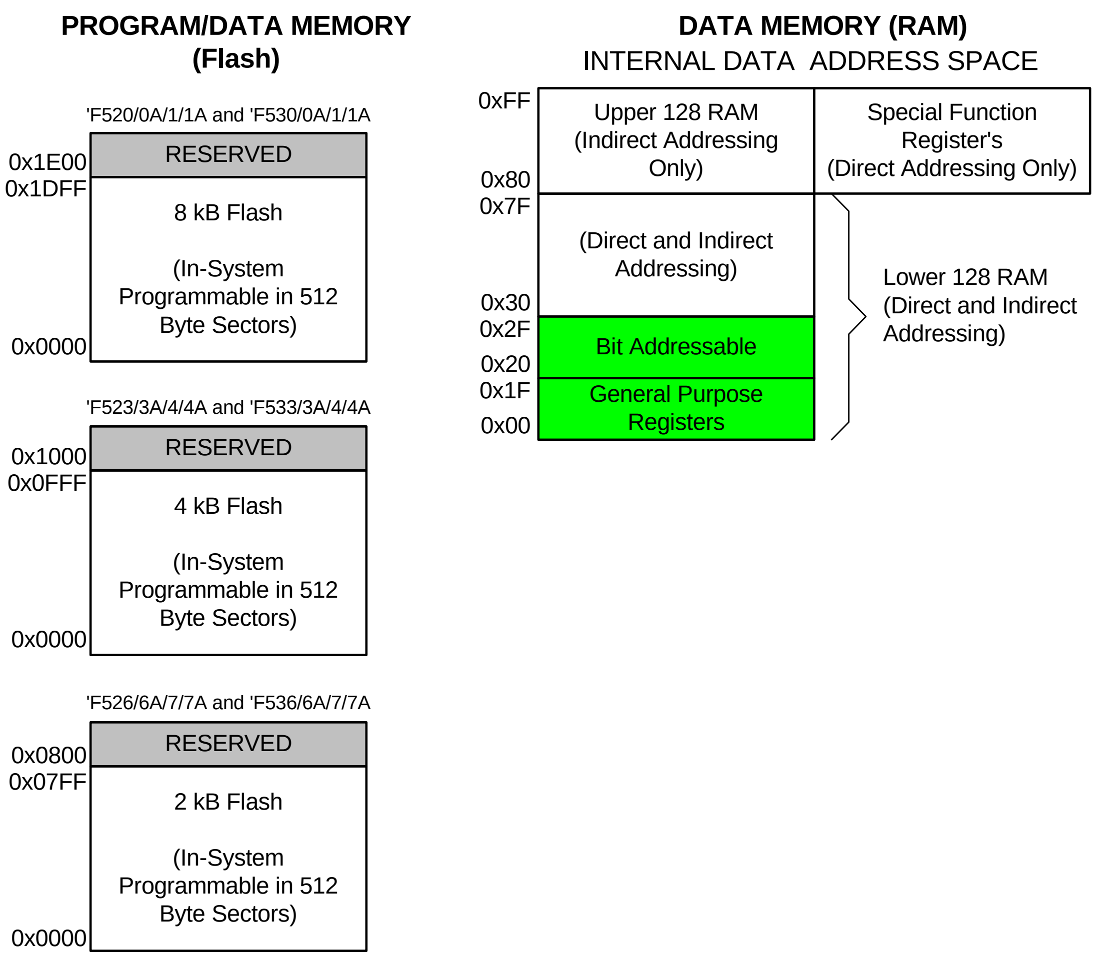


Figure 9.1. Memory Map

9.1. Program Memory

The CIP-51 core has a 64 kB program memory space. The C8051F520/0A/1/1A and C8051F530/0A/1/1A implement 8 kB of this program memory space as in-system, re-programmable Flash memory, organized in a contiguous block from addresses 0x0000 to 0x1FFF. Addresses above 0x1DFF are reserved on the 8 kB devices. The C8051F523/3A/4/4A and C8051F533/3A/4/4A implement 4 kB of Flash from addresses 0x0000 to 0x0FFF. The C8051F526/6A/7/7A and C8051F536/6A/7/7A implement 2 kB of Flash from addresses 0x0000 to 0x07FF.

Program memory is normally assumed to be read-only. However, the C8051F52x/F52xA/F53x/F53xA can write to program memory by setting the Program Store Write Enable bit (PSCTL.0) and using the MOVX write instruction. This feature provides a mechanism for updates to program code and use of the program memory space for non-volatile data storage. Refer to Section “12. Flash Memory” on page 113 for further details.

12.3. Non-volatile Data Storage

The Flash memory can be used for non-volatile data storage as well as program code. This allows data such as calibration coefficients to be calculated and stored at run time. Data is written using the MOVX write instruction and read using the MOVC instruction. Note: MOVX read instructions always target XRAM.

Note: See Section “12.1. Programming The Flash Memory” on page 113 for minimum V_{DD} and temperature requirements for flash erase and write operations.

12.4. Security Options

The CIP-51 provides security options to protect the Flash memory from inadvertent modification by software as well as to prevent the viewing of proprietary program code and constants. The Program Store Write Enable (bit PSWE in register PSCTL) and the Program Store Erase Enable (bit PSEE in register PSCTL) bits protect the Flash memory from accidental modification by software. PSWE must be explicitly set to 1 before software can modify the Flash memory; both PSWE and PSEE must be set to 1 before software can erase Flash memory. Additional security features prevent proprietary program code and data constants from being read or altered across the C2 interface.

A Security Lock Byte located at the last byte of Flash user space offers protection of the Flash program memory from access (reads, writes, or erases) by unprotected code or the C2 interface. The Flash security mechanism allows the user to lock *n* 512-byte Flash pages, starting at page 0 (addresses 0x0000 to 0x01FF), where *n* is the 1’s complement number represented by the Security Lock Byte. **Note that the page containing the Flash Security Lock Byte is unlocked when no other Flash pages are locked (all bits of the Lock Byte are 1) and locked when any other Flash pages are locked (any bit of the Lock Byte is 0).** See example below.

Security Lock Byte:	11111101b
1’s Complement:	00000010b
Flash pages locked:	3 (First two Flash pages + Lock Byte Page)
Addresses locked:	0x0000 to 0x03FF (first two Flash pages) 0x1C00 to 0x1DFF in ’F520/0A/1/1A and ’F530/0A/1/1A 0x0C00 to 0x0FFF in ’F523/3A/4/4A and ’F533/3A/4/4A and 0x0600 to 0x07FF in ’F526/6A/7/7A and ’F536/6A/7/7A

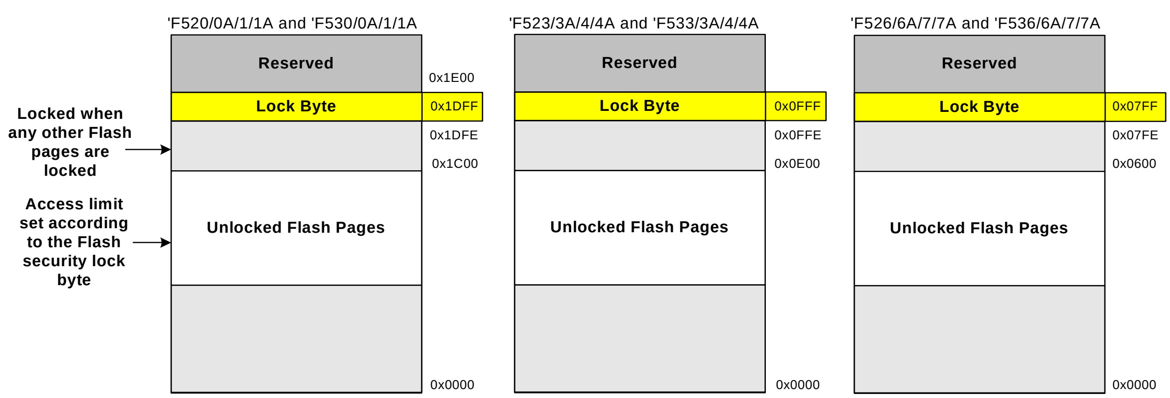


Figure 12.1. Flash Program Memory Map

SFR Definition 12.1. PSCTL: Program Store R/W Control

R	R	R	R	R	R	R/W	R/W	Reset Value
—	—	—	—	—	—	PSEE	PSWE	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x8F

Bits7–2: **UNUSED**: Read = 000000b, Write = don't care.

Bit1: **PSEE**: Program Store Erase Enable
Setting this bit (in combination with PSWE) allows an entire page of Flash program memory to be erased. If this bit is logic 1 and Flash writes are enabled (PSWE is logic 1), a write to Flash memory using the MOVX instruction will erase the entire page that contains the location addressed by the MOVX instruction. The value of the data byte written does not matter.
0: Flash program memory erasure disabled.
1: Flash program memory erasure enabled.

Bit0: **PSWE**: Program Store Write Enable
Setting this bit allows writing a byte of data to the Flash program memory using the MOVX write instruction. The Flash location should be erased before writing data.
0: Writes to Flash program memory disabled.
1: Writes to Flash program memory enabled; the MOVX write instruction targets Flash memory.

Note: See Section "12.1. Programming The Flash Memory" on page 113 for minimum V_{DD} and temperature requirements for flash erase and write operations.

SFR Definition 12.2. FLKEY: Flash Lock and Key

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xB7

Bits7–0: **FLKEY**: Flash Lock and Key Register
Write:
This register provides a lock and key function for Flash erasures and writes. Flash writes and erases are enabled by writing 0xA5 followed by 0xF1 to the FLKEY register. Flash writes and erases are automatically disabled after the next write or erase is complete. If any writes to FLKEY are performed incorrectly, or if a Flash write or erase operation is attempted while these operations are disabled, the Flash will be permanently locked from writes or erasures until the next device reset. If an application never writes to Flash, it can intentionally lock the Flash by writing a non-0xA5 value to FLKEY from software.
Read:
When read, bits 1–0 indicate the current Flash lock state.
00: Flash is write/erase locked.
01: The first key code has been written (0xA5).
10: Flash is unlocked (writes/erases allowed).
11: Flash writes/erases disabled until the next reset.

Important Note: The SPI can be operated in either 3-wire or 4-wire modes, depending on the state of the NSSMD1–NSSMD0 bits in register SPI0CN. According to the SPI mode, the NSS signal may or may not be routed to a Port pin.

13.2. Port I/O Initialization

Port I/O initialization consists of the following steps:

1. Select the input mode (analog or digital) for all Port pins, using the Port Input Mode register (PnMDIN).
2. Select the output mode (open-drain or push-pull) for all Port pins, using the Port Output Mode register (PnMDOUT).
3. Select any pins to be skipped by the I/O Crossbar using the Port Skip registers (PnSKIP).
4. Assign Port pins to desired peripherals using the XBRn registers.
5. Enable the Crossbar (XBARE = 1).

All Port pins must be configured as either analog or digital inputs. Any pins to be used as Comparator or ADC inputs should be configured as an analog inputs. When a pin is configured as an analog input, its weak pullup, digital driver, and digital receiver are disabled. This process saves power and reduces noise on the analog input. Pins configured as digital inputs may still be used by analog peripherals; however, this practice is not recommended.

Additionally, all analog input pins should be configured to be skipped by the Crossbar (accomplished by setting the associated bits in PnSKIP). Port input mode is set in the PnMDIN register, where a 1 indicates a digital input, and a 0 indicates an analog input. All pins default to digital inputs on reset. See SFR Definition 13.4 for the PnMDIN register details.

Important Note: Port 0 and Port 1 pins are 5.25 V tolerant across the operating range of V_{REGIN}.

The output driver characteristics of the I/O pins are defined using the Port Output Mode registers (PnMDOUT). Each Port Output driver can be configured as either open drain or push-pull. This selection is required even for the digital resources selected in the XBRn registers, and is not automatic. When the WEAKPUD bit in XBR1 is 0, a weak pullup is enabled for all Port I/O configured as open-drain. WEAKPUD does not affect the push-pull Port I/O. Furthermore, the weak pullup is turned off on an output that is driving a 0 and for pins configured for analog input mode to avoid unnecessary power dissipation.

Registers XBR0 and XBR1 must be loaded with the appropriate values to select the digital I/O functions required by the design. Setting the XBARE bit in XBR1 to 1 enables the Crossbar. Until the Crossbar is enabled, the external pins remain as standard Port I/O (in input mode), regardless of the XBRn Register settings. For given XBRn Register settings, one can determine the I/O pin-out using the Priority Decode Table.

The Crossbar must be enabled to use Port pins as standard Port I/O in output mode. **Port output drivers are disabled while the Crossbar is disabled.**

SFR Definition 14.1. OSCICN: Internal Oscillator Control

R/W	R/W	R/W	R	R	R/W	R/W	R/W	Reset Value
IOSCEN1	IOSCEN0	SUSPEND	IFRDY	—	IFCN2	IFCN1	IFCN0	11000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xB2

Bits7–6: **IOSCEN[1:0]**: Internal Oscillator Enable Bits.
00: Oscillator Disabled.
01: Reserved.
10: Reserved.
11: Oscillator Enabled in Normal Mode and Disabled in Suspend Mode.

Bit5: **SUSPEND**: Internal Oscillator Suspend Enable Bit.
Setting this bit to logic 1 places the internal oscillator in SUSPEND mode. The internal oscillator resumes operation when one of the SUSPEND mode awakening events occur.

Bit4: **IFRDY**: Internal Oscillator Frequency Ready Flag.
0: Internal Oscillator is not running at programmed frequency.
1: Internal Oscillator is running at programmed frequency.

Bit3: **UNUSED**. Read = 0b, Write = don't care.

Bits2–0: **IFCN2–0**: Internal Oscillator Frequency Control Bits.
000: SYSCLK derived from Internal Oscillator divided by 128 (default).
001: SYSCLK derived from Internal Oscillator divided by 64.
010: SYSCLK derived from Internal Oscillator divided by 32.
011: SYSCLK derived from Internal Oscillator divided by 16.
100: SYSCLK derived from Internal Oscillator divided by 8.
101: SYSCLK derived from Internal Oscillator divided by 4.
110: SYSCLK derived from Internal Oscillator divided by 2.
111: SYSCLK derived from Internal Oscillator divided by 1.

14.2. External Oscillator Drive Circuit

The external oscillator circuit may drive an external crystal, ceramic resonator, capacitor, or RC network. A CMOS clock may also provide a clock input. For a crystal or ceramic resonator configuration, the crystal/resonator must be wired across the XTAL1 and XTAL2 pins as shown in Option 1 of Figure 14.1. A 10 MΩ resistor also must be wired across the XTAL1 and XTAL2 pins for the crystal/resonator configuration. In RC, capacitor, or CMOS clock configuration, the clock source should be wired to the XTAL2 pin as shown in Option 2, 3, or 4 of Figure 14.1. The type of external oscillator must be selected in the OSCXCN register, and the frequency control bits (XFCN) must be selected appropriately (see SFR Definition 14.4. OSCXCN: External Oscillator Control).

Important Note on External Oscillator Usage: Port pins must be configured when using the external oscillator circuit. When the external oscillator drive circuit is enabled in crystal/resonator mode, Port pins P0.7 and P1.0 ('F53x/'F53xA) or P0.2 and P0.3 ('F52x/'F52xA) are used as XTAL1 and XTAL2 respectively. When the external oscillator drive circuit is enabled in capacitor, RC, or CMOS clock mode, Port pin P1.0 ('F53x/'F53xA) or P0.3 ('F52x/'F52xA) is used as XTAL2. The Port I/O Crossbar should be configured to skip the Port pins used by the oscillator circuit; see Section "13.1. Priority Crossbar Decoder" on page 122 for Crossbar configuration. Additionally, when using the external oscillator circuit in crystal/resonator, capacitor, or RC mode, the associated Port pins should be configured as **analog inputs**. In CMOS clock mode, the associated pin should be configured as a **digital input**. See Section "13.2. Port I/O Initialization" on page 126 for details on Port input mode selection.

14.2.1. Clocking Timers Directly Through the External Oscillator

The external oscillator source divided by eight is a clock option for the timers (Section "18. Timers" on page 182) and the Programmable Counter Array (PCA) (Section "19. Programmable Counter Array (PCA0)" on page 195). When the external oscillator is used to clock these peripherals, but is not used as the system clock, the external oscillator frequency must be less than or equal to the system clock frequency. In this configuration, the clock supplied to the peripheral (external oscillator / 8) is synchronized with the system clock; the jitter associated with this synchronization is limited to ±0.5 system clock cycles.

14.2.2. External Crystal Example

If a crystal or ceramic resonator is used as an external oscillator source for the MCU, the circuit should be configured as shown in Figure 14.1, Option 1. The External Oscillator Frequency Control value (XFCN) should be chosen from the Crystal column of the table in SFR Definition 14.4. For example, a 12 MHz crystal requires an XFCN setting of 111b.

When the crystal oscillator is first enabled, the oscillator amplitude detection circuit requires a settling time to achieve proper bias. Introducing a delay of 1 ms between enabling the oscillator and checking the XTLVLD bit will prevent a premature switch to the external oscillator as the system clock. Switching to the external oscillator before the crystal oscillator has stabilized can result in unpredictable behavior. The recommended procedure is:

1. Configure XTAL1 and XTAL2 pins by writing 1 to the port latch.
2. Configure XTAL1 and XTAL2 as analog inputs.
3. Enable the external oscillator.
4. Wait at least 1 ms.
5. Poll for XTLVLD => 1.
6. Switch the system clock to the external oscillator.

Note: Tuning-fork crystals may require additional settling time before XTLVLD returns a valid result.

The capacitors shown in the external crystal configuration provide the load capacitance required by the crystal for correct oscillation. These capacitors are "in series" as seen by the crystal and "in parallel" with the stray capacitance of the XTAL1 and XTAL2 pins.

15.1. Enhanced Baud Rate Generation

The UART0 baud rate is generated by Timer 1 in 8-bit auto-reload mode. The TX clock is generated by TL1; the RX clock is generated by a copy of TL1 (shown as RX Timer in Figure 15.2), which is not user-accessible. Both TX and RX Timer overflows are divided by two to generate the TX and RX baud rates. The RX Timer runs when Timer 1 is enabled, and uses the same reload value (TH1). However, an RX Timer reload is forced when a START condition is detected on the RX pin. This allows a receive to begin any time a START is detected, independent of the TX Timer state.

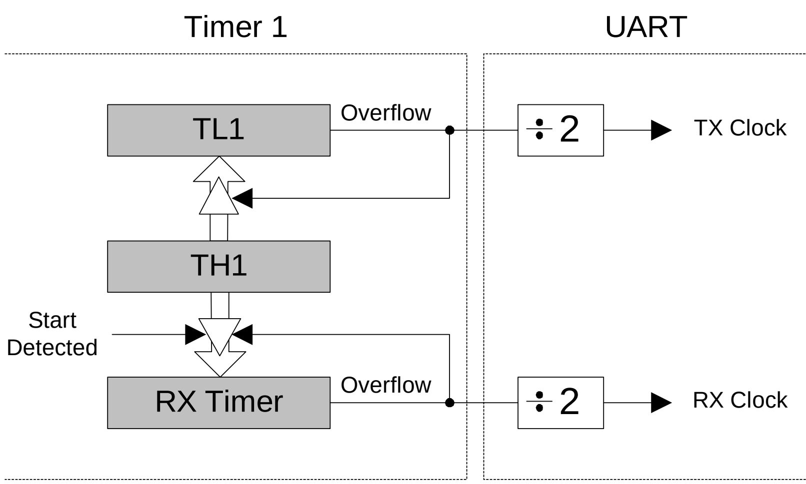


Figure 15.2. UART0 Baud Rate Logic

Timer 1 should be configured for Mode 2, 8-bit auto-reload (see Section “18.1.3. Mode 2: 8-bit Counter/Timer with Auto-Reload” on page 184). The Timer 1 reload value should be set so that overflows will occur at two times the desired UART baud rate frequency. Note that Timer 1 may be clocked by one of six sources: SYSCLK, SYSCLK / 4, SYSCLK / 12, SYSCLK / 48, the external oscillator clock / 8, or an external input T1. The UART0 baud rate is determined by Equation 15.1-A and Equation 15.1-B.

A) $$UartBaudRate = \frac{1}{2} \times T1\_Overflow\_Rate$$

B) $$T1\_Overflow\_Rate = \frac{T1_{CLK}}{256 - TH1}$$

Equation 15.1. UART0 Baud Rate

Where $T1_{CLK}$ is the frequency of the clock supplied to Timer 1, and *T1H* is the high byte of Timer 1 (8-bit auto-reload mode reload value). Timer 1 clock frequency is selected as described in Section “18. Timers” on page 182. A quick reference for typical baud rates and system clock frequencies is given in Table 15.1. Note that the internal oscillator may still generate the system clock when the external oscillator is driving Timer 1.

The shift register contents are locked after the slave detects the first edge of SCK. Writes to SPI0DAT that occur after the first SCK edge will be held in the TX latch until the end of the current transfer.

When configured as a slave, SPI0 can be configured for 4-wire or 3-wire operation. The default, 4-wire slave mode, is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 1. In 4-wire mode, the NSS signal is routed to a port pin and configured as a digital input. SPI0 is enabled when NSS is logic 0, and disabled when NSS is logic 1. The bit counter is reset on a falling edge of NSS. Note that the NSS signal must be driven low at least 2 system clocks before the first active edge of SCK for each byte transfer. Figure 16.4 shows a connection diagram between two slave devices in 4-wire slave mode and a master device.

3-wire slave mode is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 0. NSS is not used in this mode, and is not mapped to an external port pin through the crossbar. Since there is not a way of uniquely addressing the device in 3-wire slave mode, SPI0 must be the only slave device present on the bus. It is important to note that in 3-wire slave mode there is no external means of resetting the bit counter that determines when a full byte has been received. The bit counter can only be reset by disabling and re-enabling SPI0 with the SPIEN bit. Figure 16.3 shows a connection diagram between a slave device in 3-wire slave mode and a master device.

16.4. SPI0 Interrupt Sources

When SPI0 interrupts are enabled, the following four flags will generate an interrupt when they are set to logic 1:

Note that all of the following interrupt bits must be cleared by software.

1. The SPI Interrupt Flag, SPIF (SPI0CN.7) is set to logic 1 at the end of each byte transfer. This flag can occur in all SPI0 modes.
2. The Write Collision Flag, WCOL (SPI0CN.6) is set to logic 1 if a write to SPI0DAT is attempted when the transmit buffer has not been emptied to the SPI shift register. When this occurs, the write to SPI0DAT will be ignored, and the transmit buffer will not be written.This flag can occur in all SPI0 modes.
3. The Mode Fault Flag MODF (SPI0CN.5) is set to logic 1 when SPI0 is configured as a master in multi-master mode and the NSS pin is pulled low. When a Mode Fault occurs, the MSTEN and SPIEN bits in SPI0CN are set to logic 0 to disable SPI0 and allow another master device to access the bus.
4. The Receive Overrun Flag RXOVRN (SPI0CN.4) is set to logic 1 when configured as a slave, and a transfer is completed while the receive buffer still holds an unread byte from a previous transfer. The new byte is not transferred to the receive buffer, allowing the previously received data byte to be read. The data byte which caused the overrun is lost.

17. LIN (C8051F520/0A/3/3A/6/6A and C8051F530/0A/3/3A/6/6A)

Important Note: This chapter assumes an understanding of the Local Interconnect Network (LIN) protocol. For more information about the LIN protocol, including specifications, please refer to the LIN consortium (http://www.lin-subbus.org/).

LIN is an asynchronous, serial communications interface used primarily in automotive networks. The Silicon Laboratories LIN controller is compliant to the 2.1 Specification, implements a complete hardware LIN interface, and includes the following features:

- Selectable Master and Slave modes.
- Automatic baud rate option in slave mode
- The internal oscillator is accurate to within 0.5% of 24.5 MHz across the entire temperature range and for VDD voltages greater than or equal to the minimum output of the on-chip voltage regulator, so an external oscillator is not necessary for master mode operation for most systems.

Note: The minimum system clock (SYSCLK) required when using the LIN peripheral is 8 MHz.

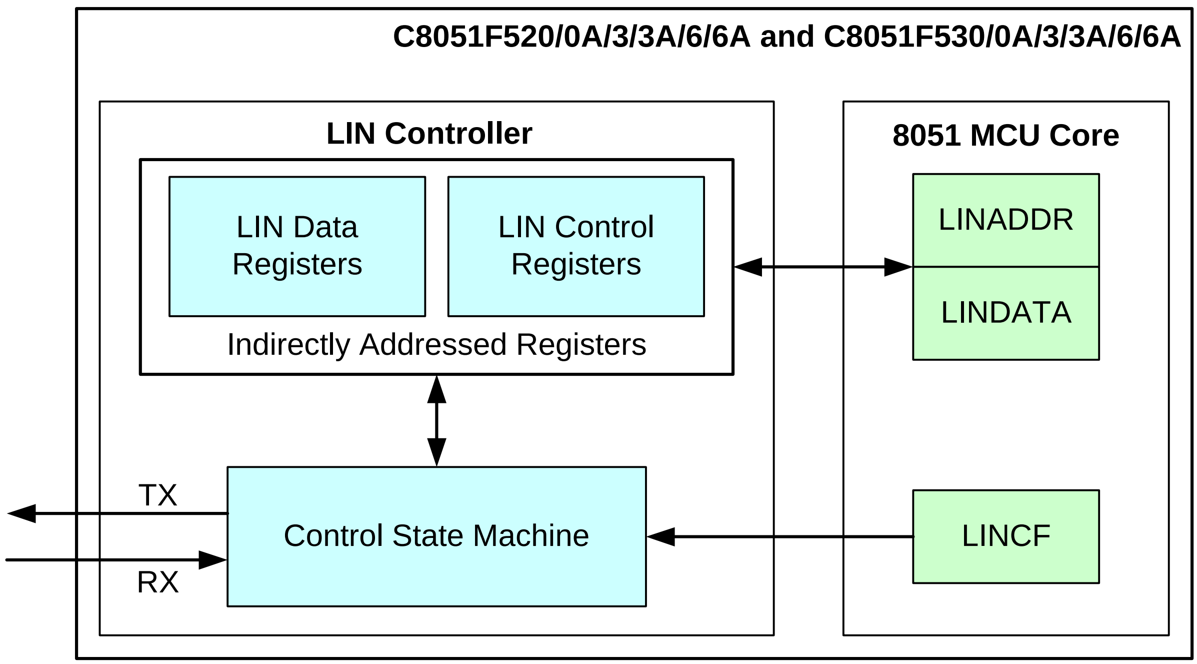


Figure 17.1. LIN Block Diagram

The LIN peripheral has four main components:

1. LIN Access Registers—Provide the interface between the MCU core and the LIN peripheral.
2. LIN Data Registers—Where transmitted and received message data bytes are stored.
3. LIN Control Registers—Control the functionality of the LIN interface.
4. Control State Machine and Bit Streaming Logic—Contains the hardware that serializes messages and controls the bus timing of the controller.

17.3. LIN Master Mode Operation

The master node is responsible for the scheduling of messages and sends the header of each frame, containing the SYNCH BREAK FIELD, SYNCH FIELD and IDENTIFIER FIELD. The steps to schedule a message transmission or reception are listed below.

1. Load the 6-bit Identifier into the LIN0ID register.
2. Load the data length into the LIN0SIZE register. Set the value to the number of data bytes or "1111b" if the data length should be decoded from the identifier. Also, set the checksum type, classic or enhanced, in the same LIN0SIZE register.
3. Set the data direction by setting the TXRX bit (LIN0CTRL.5). Set the bit to 1 to perform a master transmit operation, or set the bit to 0 to perform a master receive operation.
4. If performing a master transmit operation, load the data bytes to transmit into the data buffer (LIN0DT1 to LIN0DT8).
5. Set the STREQ bit (LIN0CTRL.0) to start the message transfer. The LIN peripheral will schedule the message frame and request an interrupt if the message transfer is successfully completed or if an error has occurred.

This code segment shows the procedure to schedule a message in a transmission operation:

```
LINADDR   = 0x08;// Point to LIN0CTRL
LINDATA  |=  0x20;// Select to transmit data
LINADDR   = 0x0E;// Point to LIN0ID
LINDATA   = 0x11;// Load the ID, in this example 0x11
LINADDR   = 0x0B;// Point to LIN0SIZE
LINDATA   = ( LINDATA & 0xF0 ) | 0x08; // Load the size with 8

LINADDR = 0x00;// Point to Data buffer first byte
for (i=0; i<8; i++)
{
   LINDATA = i + 0x41;// Load the buffer with ‘A’, ‘B’, ...
   LINADDR++;// Increment the address to the next buffer
}
LINADDR   = 0x08;// Point to LIN0CTRL
LINDATA   = 0x01;// Start Request
```

The application should perform the following steps when an interrupt is requested.

1. Check the DONE bit (LIN0ST.0) and the ERROR bit (LIN0ST.2).
2. If performing a master receive operation and the transfer was successful, read the received data from the data buffer.
3. If the transfer was not successful, check the error register to determine the kind of error. Further error handling has to be done by the application.
4. Set the RSTINT (LIN0CTRL.3) and RSTERR bits (LIN0CTRL.2) to reset the interrupt request and the error flags.

17.4. LIN Slave Mode Operation

When the device is configured for slave mode operation, it must wait for a command from a master node. Access from the firmware to data buffer and ID registers of the LIN peripheral is only possible when a data request is pending (DTREQ bit (LIN0ST.4) is 1) and also when the LIN bus is not active (ACTIVE bit (LIN0ST.7) is set to 0).

The LIN peripheral in slave mode detects the header of the message frame sent by the LIN master. If slave synchronization is enabled (autobaud), the slave synchronizes its internal bit time to the master bit time.

The LIN peripheral configured for slave mode will generated an interrupt in one of three situations:

1. After the reception of the IDENTIFIER FIELD.
2. When an error is detected.
3. When the message transfer is completed.

The application should perform the following steps when an interrupt is detected:

1. Check the status of the DTREQ bit (LIN0ST.4). This bit is set when the IDENTIFIER FIELD has been received.
2. If DTREQ (LIN0ST.4) is set, read the identifier from LIN0ID and process it. If DTREQ (LIN0ST.4) is not set, continue to step 7.
3. Set the TXRX bit (LIN0CTRL.5) to 1 if the current frame is a transmit operation for the slave and set to 0 if the current frame is a receive operation for the slave.
4. Load the data length into LIN0SIZE.
5. For a slave transmit operation, load the data to transmit into the data buffer.
6. Set the DTACK bit (LIN0CTRL.4). Continue to step 10.
7. If DTREQ (LIN0ST.4) is not set, check the DONE bit (LIN0ST.0). The transmission was successful if the DONE bit is set.
8. If the transmission was successful and the current frame was a receive operation for the slave, load the received data bytes from the data buffer.
9. If the transmission was not successful, check LIN0ERR to determine the nature of the error. Further error handling has to be done by the application.
10. Set the RSTINT (LIN0CTRL.3) and RSTERR bits (LIN0CTRL.2) to reset the interrupt request and the error flags.

In addition to these steps, the application should be aware of the following:

1. If the current frame is a transmit operation for the slave, steps 1 through 5 must be completed during the IN-FRAME RESPONSE SPACE. If it is not completed in time, a timeout will be detected by the master.
2. If the current frame is a receive operation for the slave, steps 1 through 5 have to be finished until the reception of the first byte after the IDENTIFIER FIELD. Otherwise, the internal receive buffer of the LIN peripheral will be overwritten and a timeout error will be detected in the LIN peripheral.
3. The LIN module does not directly support LIN Version 1.3 Extended Frames. If the application detects an unknown identifier (e.g. extended identifier), it has to write a 1 to the STOP bit (LIN0CTRL.7) instead of setting the DTACK (LIN0CTRL.4) bit. At that time, steps 2 through 5 can then be skipped. In this situation, the LIN peripheral stops the processing of the LIN communication until the next SYNC BREAK is received.
4. Changing the configuration of the checksum during a transaction will cause the interface to reset and the transaction to be lost. To prevent this, the checksum should not be configured while a transaction is

17.7.2. LIN Indirect Access SFR Registers Definition

Table 17.4. LIN Registers* (Indirectly Addressable)

Name	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LIN0DT1	0x00	DATA1[7:0]							
LIN0DT2	0x01	DATA2[7:0]							
LIN0DT3	0x02	DATA3[7:0]							
LIN0DT4	0x03	DATA4[7:0]							
LIN0DT5	0x04	DATA5[7:0]							
LIN0DT6	0x05	DATA6[7:0]							
LIN0DT7	0x06	DATA7[7:0]							
LIN0DT8	0x07	DATA8[7:0]							
LIN0CTRL	0x08	STOP(s)	SLEEP(s)	TXRX	DTACK(s)	RSTINT	RSTERR	WUPREQ	STREQ(m)
LIN0ST	0x09	ACTIVE	IDLTOUT	ABORT(s)	DTREQ(s)	LININT	ERROR	WAKEUP	DONE
LIN0ERR	0x0A				SYNCH(s)	PRTY(s)	TOUT	CHK	BITERR
LIN0SIZE	0x0B	ENHCHK				LINSIZE[3:0]			
LIN0DIV	0x0C	DIVLSB[7:0]							
LIN0MUL	0x0D	PRESCL[1:0]		LINMUL[4:0]					DIV9
LIN0ID	0x0E			ID[5:0]					

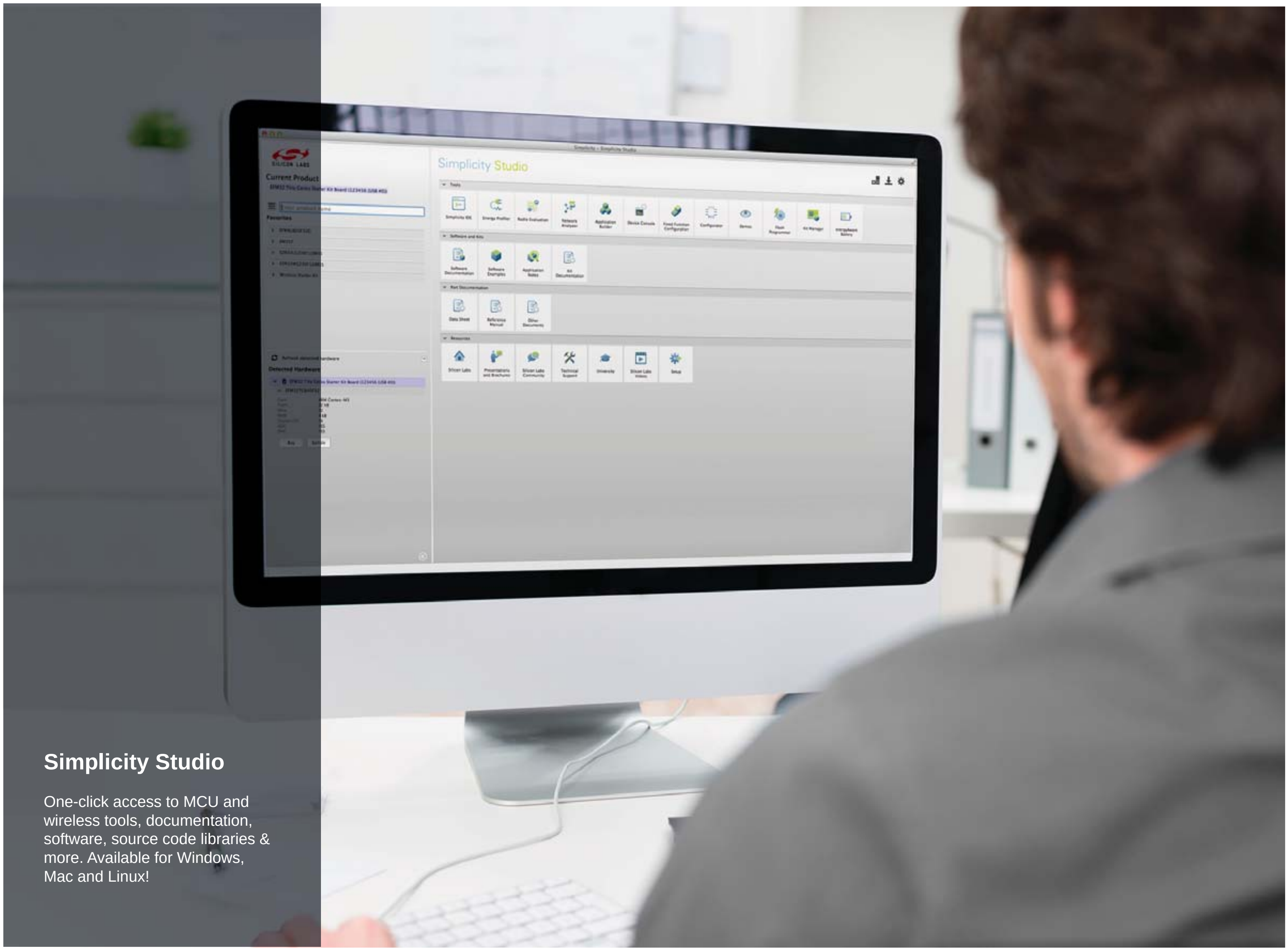
*These registers are used in both master and slave mode. The register bits marked with (m) are accessible only in Master mode while the register bits marked with (s) are accessible only in slave mode. All other registers are accessible in both modes.

SFR Definition 17.4. LIN0DT1: LIN0 Data Byte 1

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Address: 0x00 (indirect)

Bit7–0: **LIN0DT1**: LIN Data Byte 1.
Serial Data Byte 1 that is received or transmitted across the LIN interface.



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