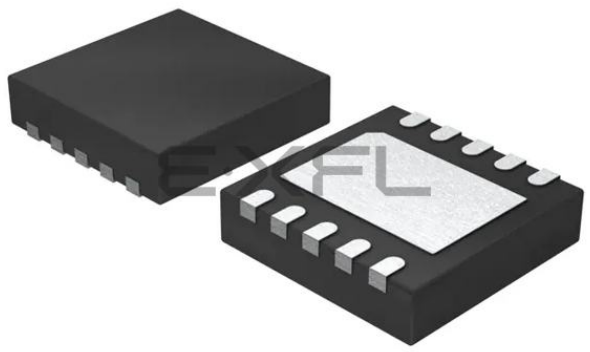

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	6
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	10-VFDFN Exposed Pad
Supplier Device Package	10-DFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f527a-imr

List of Figures

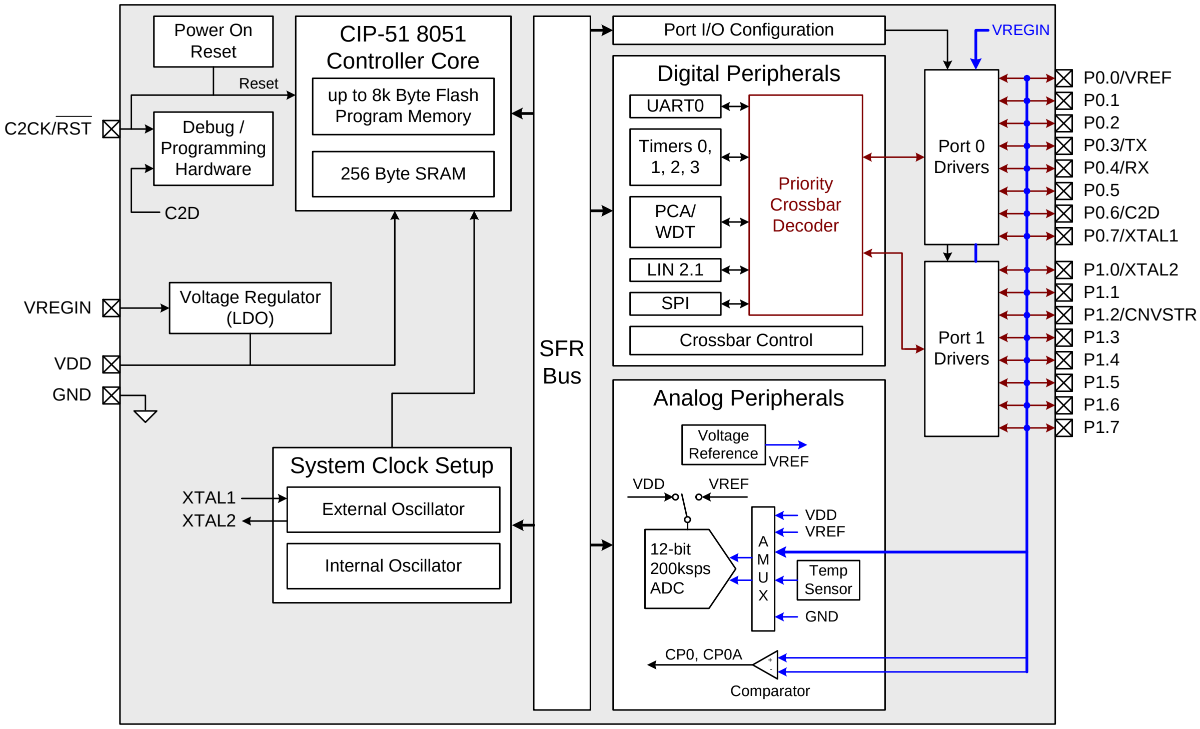


Figure 1.3. C8051F53x Block Diagram (Silicon Revision A)

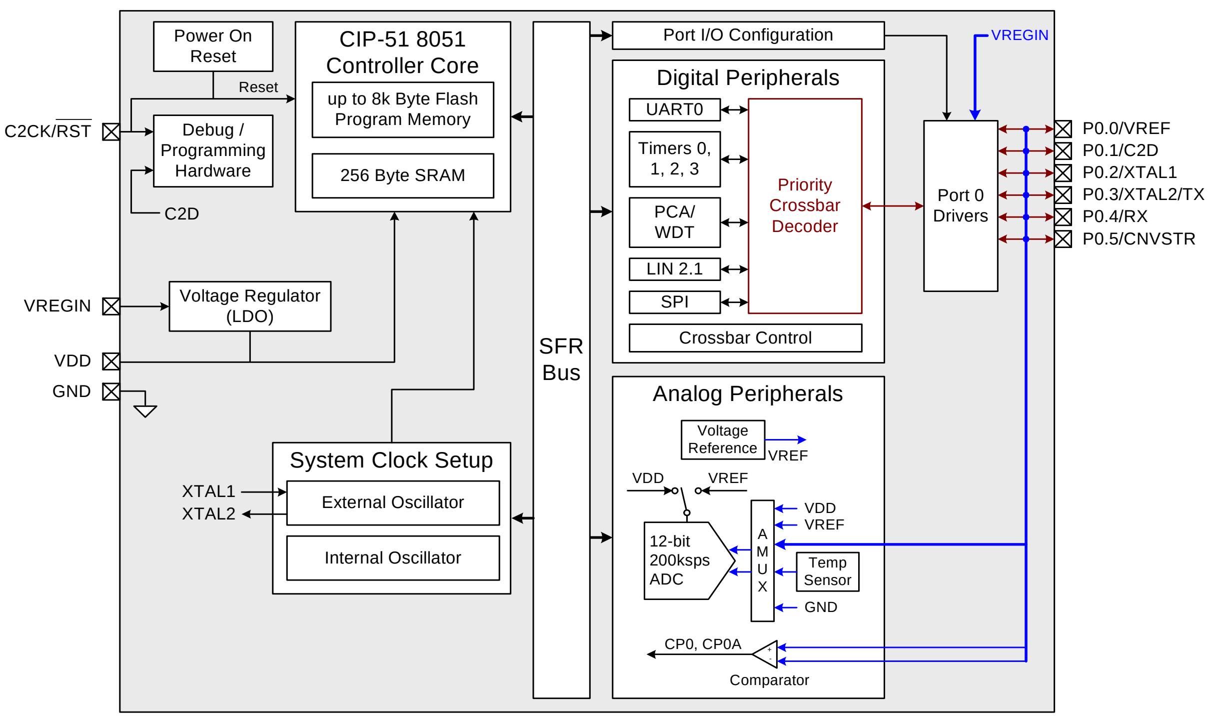


Figure 1.4. C8051F52x Block Diagram (Silicon Revision A)

Table 3.1. Pin Definitions for the C8051F52x and C8051F52xA (DFN 10)

Name	Pin Numbers		Type	Description
	‘F52xA ‘F52x-C	‘F52x		
$\overline{RST}$/	1	1	D I/O	Device Reset. Open-drain output of internal POR or V_{DD} monitor. An external source can initiate a system reset by driving this pin low for at least the minimum $\overline{RST}$ low time to generate a system reset, as defined in Table 2.8 on page 32. A 1 kΩ pullup to V_{REGIN} is recommended. See Reset Sources Section for a complete description.
C2CK			D I/O	Clock signal for the C2 Debug Interface.
P0.0/	2	2	D I/O or A In	Port 0.0. See Port I/O Section for a complete description.
V_{REF}			A O or D In	External V_{REF} Input. See V_{REF} Section.
GND	3	3		Ground.
V_{DD}	4	4		Core Supply Voltage.
V_{REGIN}	5	5		On-Chip Voltage Regulator Input.
P0.5/RX*/	6	—	D I/O or A In	Port 0.5. See Port I/O Section for a complete description.
CNVSTR			D In	External Converter start input for the ADC0, see Section “4. 12-Bit ADC (ADC0)” on page 52 for a complete description.
P0.5/	—	6	D I/O or A In	Port 0.5. See Port I/O Section for a complete description.
CNVSTR			D In	External Converter start input for the ADC0, see Section “4. 12-Bit ADC (ADC0)” on page 52 for a complete description.
P0.4/TX*	7	—	D I/O or A In	Port 0.4. See Port I/O Section for a complete description.
P0.4/RX*	—	7	D I/O or A In	Port 0.4. See Port I/O Section for a complete description.
P0.3	8	—	D I/O or A In	Port 0.3. See Port I/O Section for a complete description.
XTAL2			D I/O	External Clock Output. For an external crystal or resonator, this pin is the excitation driver. This pin is the external clock input for CMOS, capacitor, or RC oscillator configurations. See Section “14. Oscillators” on page 135.

Note: Please refer to Section “20. Device Specific Behavior” on page 210.

Table 3.4. Pin Definitions for the C8051F53x and C805153xA (TSSOP 20) (Continued)

Name	Pin Numbers		Type	Description
	‘F53xA ‘F53x-C	‘F53x		
P0.4/TX*	19	—	D I/O or A In	Port 0.4. See Port I/O Section for a complete description.
P0.4/RX*	—	19	D I/O or A In	Port 0.4. See Port I/O Section for a complete description.
P0.3	20	—	D I/O or A In	Port 0.3. See Port I/O Section for a complete description.
P0.3/TX*	—	20	D I/O or A In	Port 0.3. See Port I/O Section for a complete description.
***Note:** Please refer to Section “20. Device Specific Behavior” on page 210.				

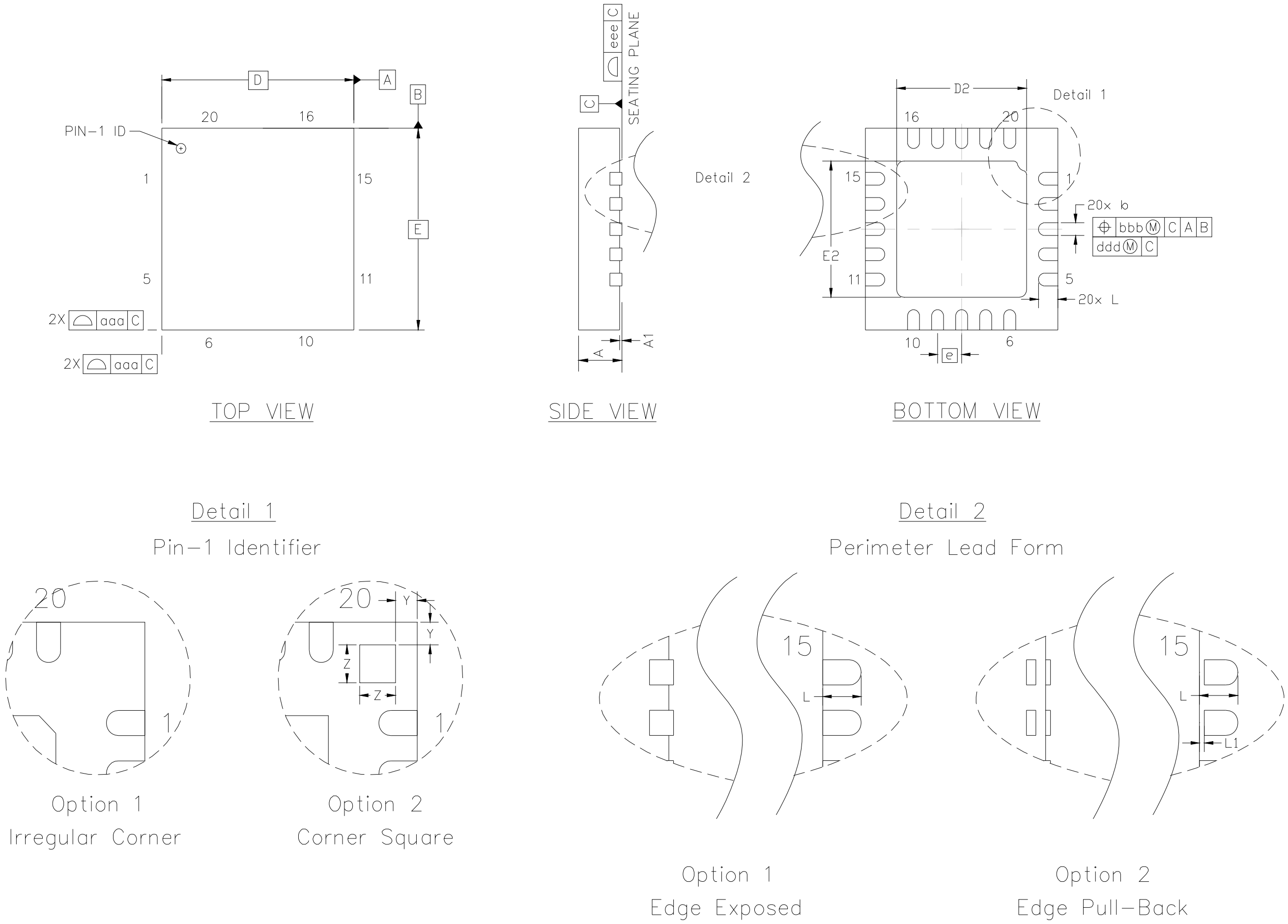


Figure 3.8. QFN-20 Package Diagram*

***Note:** The Package Dimensions are given in Table 3.8, “QFN-20 Package Diagram Dimensions,” on page 49.

Table 3.9. QFN-20 Landing Diagram Dimensions

Symbol	Min	Max
C1	3.90	4.00
C2	3.90	4.00
E	0.50 BSC.	
X1	0.20	0.30
X2	2.75	2.85
Y1	0.65	0.75
Y2	2.75	2.85

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

Solder Mask Design

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 2x2 array of 1.10 x 1.10 mm openings on 1.30 mm pitch should be used for the center ground pad.

Card Assembly

8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Gain Register Definition 4.1. ADC0GNH: ADC0 Selectable Gain High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
GAINH[7:0]								11111100
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Address: 0x04

Bits7–0: High byte of Selectable Gain Word.

Gain Register Definition 4.2. ADC0GNL: ADC0 Selectable Gain Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
GAINL[3:0]				Reserved	Reserved	Reserved	Reserved	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Address: 0x07

Bits7–4: Lower 4 bits of the Selectable Gain Word.
Bits3–0: **Reserved**. Must Write 0000b.

Gain Register Definition 4.3. ADC0GNA: ADC0 Additional Selectable Gain

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	GAINADD	00000001
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Address: 0x08

Bits7–1: **Reserved**. Must Write 0000000b.
Bit0: **GAINADD**: Additional Gain Bit.
Setting this bit adds 1/64 (0.016) gain to the gain value in the ADC0GNH and ADC0GNL registers.

9. Memory Organization and SFRs

The memory organization of the C8051F52x/F52xA/F53x/F53xA is similar to that of a standard 8051. There are two separate memory spaces: program memory and data memory. Program and data memory share the same address space but are accessed via different instruction types. The memory map is shown in Figure 9.1.

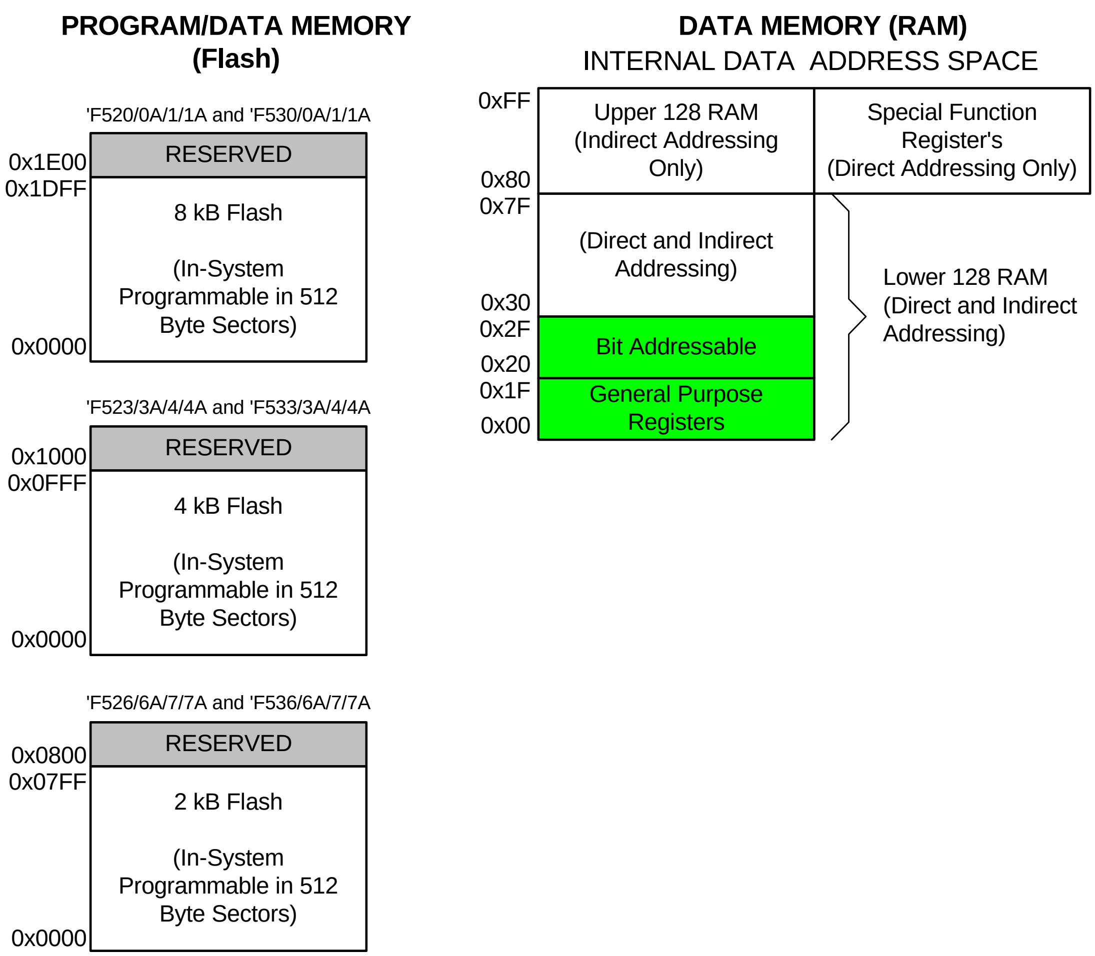


Figure 9.1. Memory Map

9.1. Program Memory

The CIP-51 core has a 64 kB program memory space. The C8051F520/0A/1/1A and C8051F530/0A/1/1A implement 8 kB of this program memory space as in-system, re-programmable Flash memory, organized in a contiguous block from addresses 0x0000 to 0x1FFF. Addresses above 0x1DFF are reserved on the 8 kB devices. The C8051F523/3A/4/4A and C8051F533/3A/4/4A implement 4 kB of Flash from addresses 0x0000 to 0x0FFF. The C8051F526/6A/7/7A and C8051F536/6A/7/7A implement 2 kB of Flash from addresses 0x0000 to 0x07FF.

Program memory is normally assumed to be read-only. However, the C8051F52x/F52xA/F53x/F53xA can write to program memory by setting the Program Store Write Enable bit (PSCTL.0) and using the MOVX write instruction. This feature provides a mechanism for updates to program code and use of the program memory space for non-volatile data storage. Refer to Section “12. Flash Memory” on page 113 for further details.

SFRs used to configure and access the sub-systems unique to the MCU. This allows the addition of new functionality while retaining compatibility with the MCS-51™ instruction set. Table 9.1 lists the SFRs implemented in the CIP-51 System Controller.

The SFR registers are accessed anytime the direct addressing mode is used to access memory locations from 0x80 to 0xFF. SFRs with addresses ending in 0x0 or 0x8 (e.g. P0, TCON, IE, etc.) are bit-addressable as well as byte-addressable. All other SFRs are byte-addressable only. Unoccupied addresses in the SFR space are reserved for future use. Accessing these areas will have an indeterminate effect and should be avoided. Refer to the corresponding pages of the data sheet, as indicated in Table 9.2, for a detailed description of each register.

Table 9.1. Special Function Register (SFR) Memory Map

F8	SPI0CN	PCA0L	PCA0H	PCA0CPL0	PCA0CPH0			VDDMON
F0	B	P0MDIN	P1MDIN				EIP1	
E8	ADC0CN	PCA0CPL1	PCA0CPH1	PCA0CPL2	PCA0CPH2			RSTSRC
E0	ACC	XBR0	XBR1		IT01CF		EIE1	
D8	PCA0CN	PCA0MD	PCA0CPM0	PCA0CPM1	PCA0CPM2			
D0	PSW	REF0CN			P0SKIP	P1SKIP		P0MAT
C8	TMR2CN	REG0CN	TMR2RLL	TMR2RLH	TMR2L	TMR2H		P1MAT
C0				ADC0GTL	ADC0GTH	ADC0LTL	ADC0LTH	P0MASK
B8	IP		ADC0TK	ADC0MX	ADC0CF	ADC0L	ADC0	P1MASK
B0	OSCIFIN	OSCXCN	OSCICN	OSCICL				FLKEY
A8	IE	CLKSEL						
A0		SPI0CFG	SPI0CKR	SPI0DAT	P0MDOUT	P1MDOUT		
98	SCON0	SBUF0		CPT0CN		CPT0MD		CPT0MX
90	P1		LINADDR	LINDATA		LINCF		
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	PSCTL
80	P0	SP	DPL	DPH				PCON
	0(8) (bit addressable)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)

ramp or during a brownout condition even when V_{DD} is below the specified minimum of 2.0 V. There are two possible ways to handle this transitional period as described below:

If using the on-chip regulator (REG0) at the 2.6 V setting (default), it is recommended that user software set the VDDMON0 threshold to its high setting ($V_{RST\text{-}HIGH}$) as soon as possible after reset by setting the VDMLVL bit to 1 in SFR Definition 11.1 (VDDMON). In this typical configuration, no external hardware or additional software routines are necessary to monitor the V_{DD} level.

Note: Please refer to Section “20.5. VDD Monitor (VDDMON0) High Threshold Setting” on page 212 for important notes related to the VDD Monitor high threshold setting in older silicon revisions A and B.

If using the on-chip regulator (REG0) at the 2.1 V setting or if directly driving V_{DD} with REG0 disabled, the user system (software/hardware) should monitor V_{DD} at power-on and also during device operation. The two key parameters that can be affected when V_{DD} < 2.0 V are: internal oscillator frequency (Table 2.11 on page 34) and minimum ADC tracking time (Table 2.3 on page 28).

SFR Definition 11.1. VDDMON: V_{DD} Monitor Control

R/W	R	R/W	R	R	R	R	R	Reset Value
VDMEN	VDDSTAT	VDMLVL	VDM1EN	Reserved	Reserved	Reserved	Reserved	1v010000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xFF

Bit7: **VDMEN**: V_{DD} Monitor Enable (VDDMON0).
This bit turns the V_{DD} monitor circuit on/off. The V_{DD} Monitor cannot generate system resets until it is also selected as a reset source in register RSTSRC (SFR Definition 11.2). The V_{DD} Monitor can be allowed to stabilize before it is selected as a reset source. **Selecting the V_{DD} monitor as a reset source before it has stabilized may generate a system reset.** See Table 2.8 on page 32 for the minimum V_{DD} Monitor turn-on time.
0: V_{DD} Monitor Disabled.
1: V_{DD} Monitor Enabled (default).

Bit6: **VDDSTAT**: V_{DD} Status.
This bit indicates the current power supply status (V_{DD} Monitor output).
0: V_{DD} is at or below the V_{DD} Monitor (VDDMON0) Threshold.
1: V_{DD} is above the V_{DD} Monitor (VDDMON0) Threshold.

Bit5: **VDMLVL**: V_{DD} Level Select.
0: V_{DD} Monitor (VDDMON0) Threshold is set to $V_{RST\text{-}LOW}$ (default).
1: V_{DD} Monitor (VDDMON0) Threshold is set to $V_{RST\text{-}HIGH}$. This setting is **required** for any system that includes code that writes to and/or erases Flash.

Bit4: **VDM1EN***: Level-sensitive V_{DD} Monitor Enable (VDDMON1).
This bit turns the V_{DD} monitor circuit on/off. If turned on, it is also selected as a reset source, and can generate a system reset.
0: Level-sensitive VDD Monitor Disabled.
1: Level-sensitive VDD Monitor Enabled (default).

Bits3–0: **RESERVED**. Read = Variable. Write = don’t care.

***Note:** Available only on the C8051F52x-C/F53x-C devices

The level of Flash security depends on the Flash access method. The three Flash access methods that can be restricted are reads, writes, and erases from the C2 debug interface, user firmware executing on unlocked pages, and user firmware executing on locked pages. Table 12.1 summarizes the Flash security features of the ’F52x/’F52xA/’F53x/’F53xA devices.

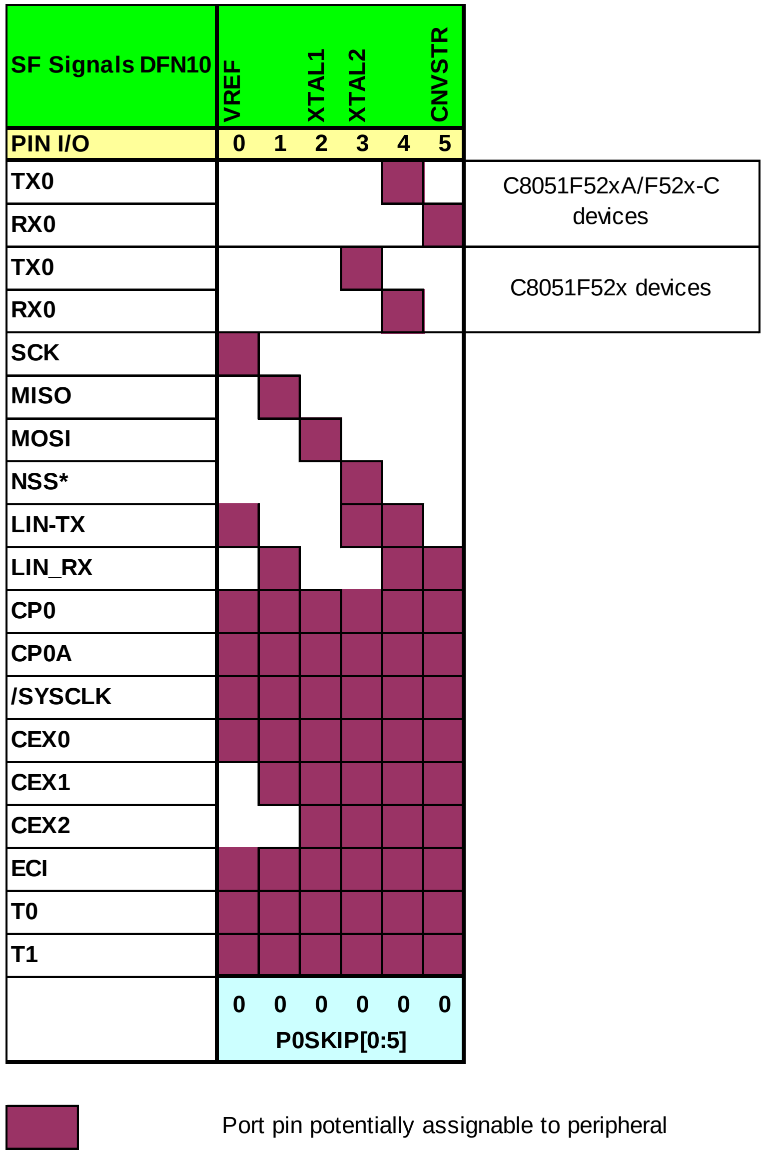
Table 12.1. Flash Security Summary

Action	C2 Debug Interface	User Firmware executing from:	
		an unlocked page	a locked page
Read, Write or Erase unlocked pages (except page with Lock Byte)	Permitted	Permitted	Permitted
Read, Write or Erase locked pages (except page with Lock Byte)	Not Permitted	Flash Error Reset	Permitted
Read or Write page containing Lock Byte (if no pages are locked)	Permitted	Permitted	Permitted
Read or Write page containing Lock Byte (if any page is locked)	Not Permitted	Flash Error Reset	Permitted
Read contents of Lock Byte (if no pages are locked)	Permitted	Permitted	Permitted
Read contents of Lock Byte (if any page is locked)	Not Permitted	Flash Error Reset	Permitted
Erase page containing Lock Byte (if no pages are locked)	Permitted	Flash Error Reset	Flash Error Reset
Erase page containing Lock Byte—Unlock all pages (if any page is locked)	C2 Device Erase Only	Flash Error Reset	Flash Error Reset
Lock additional pages (change 1s to 0s in the Lock Byte)	Not Permitted	Flash Error Reset	Flash Error Reset
Unlock individual pages (change 0s to 1s in the Lock Byte)	Not Permitted	Flash Error Reset	Flash Error Reset
Read, Write or Erase Reserved Area	Not Permitted	Flash Error Reset	Flash Error Reset

C2 Device Erase—Erases all Flash pages including the page containing the Lock Byte.

Flash Error Reset—Not permitted; Causes Flash Error Device Reset (FERROR bit in RSTSRC is 1 after reset).

- All prohibited operations that are performed via the C2 interface are ignored (do not cause device reset).
- Locking any Flash page also locks the page containing the Lock Byte.
- Once written to, the Lock Byte cannot be modified except by performing a C2 Device Erase.
- If user code writes to the Lock Byte, the Lock does not take effect until the next device reset.



Port pin potentially assignable to peripheral

SF Signals	Special Function Signals are not assigned by the crossbar. When these signals are enabled, the Crossbar must be manually configured to skip their corresponding port pins.

Note: 4-Wire SPI Only.

Figure 13.5. Crossbar Priority Decoder with No Pins Skipped (DFN 10)

SFR Definition 14.4. OSCXCN: External Oscillator Control

R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
XTLVLD	XOSCMD2	XOSCMD1	XOSCMD0	Reserved	XFCN2	XFCN1	XFCN0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xB1

Bit7: **XTLVLD**: Crystal Oscillator Valid Flag. (Read only when XOSCMD = 11x.)
0: Crystal Oscillator is unused or not yet stable.
1: Crystal Oscillator is running and stable.

Bits6–4: **XOSCMD2–0**: External Oscillator Mode Bits.
00x: External Oscillator circuit off.
010: External CMOS Clock Mode.
011: External CMOS Clock Mode with divide by 2 stage.
100: RC Oscillator Mode.
101: Capacitor Oscillator Mode.
110: Crystal Oscillator Mode.
111: Crystal Oscillator Mode with divide by 2 stage.

Bit3: **RESERVED**. Read = 0b; Must write 0b.

Bits2–0: **XFCN2–0**: External Oscillator Frequency Control Bits.
000-111: See table below:

XFCN	Crystal (XOSCMD = 11x)	RC (XOSCMD = 10x)	C (XOSCMD = 10x)
000	f ≤ 20 kHz	f ≤ 25 kHz	K Factor = 0.87
001	20 kHz < f ≤ 58 kHz	25 kHz < f ≤ 50 kHz	K Factor = 2.6
010	58 kHz < f ≤ 155 kHz	50 kHz < f ≤ 100 kHz	K Factor = 7.7
011	155 kHz < f ≤ 415 kHz	100 kHz < f ≤ 200 kHz	K Factor = 22
100	415 kHz < f ≤ 1.1 MHz	200 kHz < f ≤ 400 kHz	K Factor = 65
101	1.1 MHz < f ≤ 3.1 MHz	400 kHz < f ≤ 800 kHz	K Factor = 180
110	3.1 MHz < f ≤ 8.2 MHz	800 kHz < f ≤ 1.6 MHz	K Factor = 664
111	8.2 MHz < f ≤ 25 MHz	1.6 MHz < f ≤ 3.2 MHz	K Factor = 1590

Crystal Mode (Circuit from Figure 14.1, Option 1; XOSCMD = 11x)
Choose XFCN value to match crystal or resonator frequency.

RC Mode (Circuit from Figure 14.1, Option 2; XOSCMD = 10x)
Choose XFCN value to match frequency range:
$\mathbf{f = 1.23(10^3) / (R \times C)}$, where
f = frequency of clock in MHz
C = capacitor value in pF
R = Pullup resistor value in kΩ

C Mode (Circuit from Figure 14.1, Option 3; XOSCMD = 10x)
Choose K Factor (KF) for the oscillation frequency desired:
$\mathbf{f = KF / (C \times V_{DD})}$, where
f = frequency of clock in MHz
C = capacitor value the XTAL2 pin in pF
V_{DD} = Power Supply on MCU in volts

16.2. SPI0 Master Mode Operation

A SPI master device initiates all data transfers on a SPI bus. SPI0 is placed in master mode by setting the Master Enable flag (MSTEN, SPI0CN.6). Writing a byte of data to the SPI0 data register (SPI0DAT) when in master mode writes to the transmit buffer. If the SPI shift register is empty, the byte in the transmit buffer is moved to the shift register, and a data transfer begins. The SPI0 master immediately shifts out the data serially on the MOSI line while providing the serial clock on SCK. The SPIF (SPI0CN.7) flag is set to logic 1 at the end of the transfer. If interrupts are enabled, an interrupt request is generated when the SPIF flag is set. While the SPI0 master transfers data to a slave on the MOSI line, the addressed SPI slave device simultaneously transfers data to the SPI master on the MISO line in a full-duplex operation. Therefore, the SPIF flag serves as both a transmit-complete and receive-data-ready flag. The data byte received from the slave is transferred MSB-first into the master's shift register. When a byte is fully shifted into the register, it is moved to the receive buffer where it can be read by the processor by reading SPI0DAT.

When configured as a master, SPI0 can operate in one of three different modes: multi-master mode, 3-wire single-master mode, and 4-wire single-master mode. The default, multi-master mode is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 1. In this mode, NSS is an input to the device, and is used to disable the master SPI0 when another master is accessing the bus. When NSS is pulled low in this mode, MSTEN (SPI0CN.6) and SPIEN (SPI0CN.0) are set to 0 to disable the SPI master device, and a Mode Fault is generated (MODF, SPI0CN.5 = 1). Mode Fault will generate an interrupt if enabled. SPI0 must be manually re-enabled in software under these circumstances. In multi-master systems, devices will typically default to being slave devices while they are not acting as the system master device. In multi-master mode, slave devices can be addressed individually (if needed) using general-purpose I/O pins. Figure 16.2 shows a connection diagram between two master devices in multiple-master mode.

3-wire single-master mode is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 0. In this mode, NSS is not used and is not mapped to an external port pin through the crossbar. Any slave devices that must be addressed in this mode should be selected using general-purpose I/O pins. Figure 16.3 shows a connection diagram between a master device in 3-wire master mode and a slave device.

4-wire single-master mode is active when NSSMD1 (SPI0CN.3) = 1. In this mode, NSS is configured as an output pin and can be used as a slave-select signal for a single SPI device. In this mode, the output value of NSS is controlled (in software) with the bit NSSMD0 (SPI0CN.2). Additional slave devices can be addressed using general-purpose I/O pins. Figure 16.4 shows a connection diagram for a master device in 4-wire master mode and two slave devices.

SFR Definition 16.4. SPI0DAT: SPI0 Data

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xA3

Bits7–0: **SPI0DAT**: SPI0 Transmit and Receive Data.
The SPI0DAT register is used to transmit and receive SPI0 data. Writing data to SPI0DAT places the data into the transmit buffer and initiates a transfer when in Master Mode. A read of SPI0DAT returns the contents of the receive buffer.

17.7.2. LIN Indirect Access SFR Registers Definition

Table 17.4. LIN Registers* (Indirectly Addressable)

Name	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LIN0DT1	0x00	DATA1[7:0]							
LIN0DT2	0x01	DATA2[7:0]							
LIN0DT3	0x02	DATA3[7:0]							
LIN0DT4	0x03	DATA4[7:0]							
LIN0DT5	0x04	DATA5[7:0]							
LIN0DT6	0x05	DATA6[7:0]							
LIN0DT7	0x06	DATA7[7:0]							
LIN0DT8	0x07	DATA8[7:0]							
LIN0CTRL	0x08	STOP(s)	SLEEP(s)	TXRX	DTACK(s)	RSTINT	RSTERR	WUPREQ	STREQ(m)
LIN0ST	0x09	ACTIVE	IDLTOUT	ABORT(s)	DTREQ(s)	LININT	ERROR	WAKEUP	DONE
LIN0ERR	0x0A				SYNCH(s)	PRTY(s)	TOUT	CHK	BITERR
LIN0SIZE	0x0B	ENHCHK				LINSIZE[3:0]			
LIN0DIV	0x0C	DIVLSB[7:0]							
LIN0MUL	0x0D	PRESCL[1:0]		LINMUL[4:0]					DIV9
LIN0ID	0x0E			ID[5:0]					

*These registers are used in both master and slave mode. The register bits marked with (m) are accessible only in Master mode while the register bits marked with (s) are accessible only in slave mode. All other registers are accessible in both modes.

SFR Definition 17.4. LIN0DT1: LIN0 Data Byte 1

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Address: 0x00 (indirect)

Bit7–0: **LIN0DT1**: LIN Data Byte 1.
Serial Data Byte 1 that is received or transmitted across the LIN interface.

clocked by the system clock. When T0M is cleared, Timer 0 is clocked by the source selected by the Clock Scale bits in CKCON (see SFR Definition 18.3).

Setting the TR0 bit (TCON.4) enables the timer when either GATE0 (TMOD.3) is logic 0 or the input signal $\overline{\text{INT0}}$ is active as defined by bit IN0PL in register IT01CF (see SFR Definition 10.5. IT01CF: $\overline{\text{INT0}}$/INT1 Configuration). Setting GATE0 to 1 allows the timer to be controlled by the external input signal $\overline{\text{INT0}}$ (see Section “10.4. Interrupt Register Descriptions” on page 100), facilitating pulse width measurements.

TR0	GATE0	$\overline{\text{INT0}}$	Counter/Timer
0	X	X	Disabled
1	0	X	Enabled
1	1	0	Disabled
1	1	1	Enabled
X = Don't Care			

Setting TR0 does not force the timer to reset. The timer registers should be loaded with the desired initial value before the timer is enabled.

TL1 and TH1 form the 13-bit register for Timer 1 in the same manner as described above for TL0 and TH0. Timer 1 is configured and controlled using the relevant TCON and TMOD bits just as with Timer 0. The input signal $\overline{\text{INT0}}$ is used with Timer 1; the $\overline{\text{INT0}}$ polarity is defined by bit IN1PL in register IT01CF (see SFR Definition 10.5. IT01CF: INT0/INT1 Configuration).

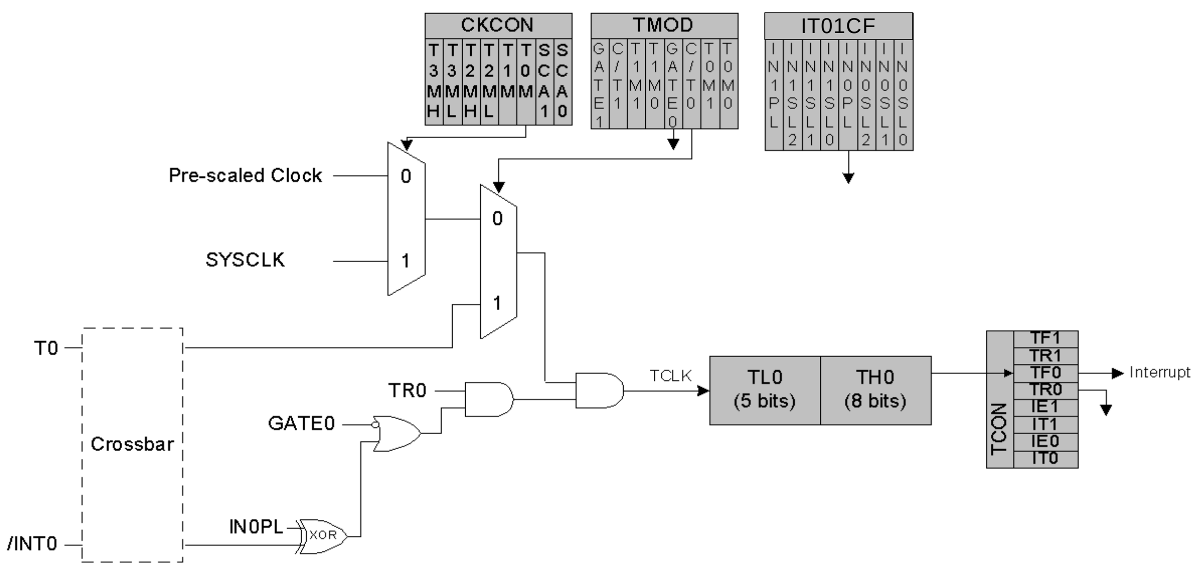


Figure 18.1. T0 Mode 0 Block Diagram

SFR Definition 18.2. TMOD: Timer Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
GATE1	C/T1	T1M1	T1M0	GATE0	C/T0	T0M1	T0M0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x89

Bit7: **GATE1**: Timer 1 Gate Control.
0: Timer 1 enabled when TR1 = 1 irrespective of $\overline{\text{INT0}}$ logic level.
1: Timer 1 enabled only when TR1 = 1 AND $\overline{\text{INT0}}$ is active as defined by bit IN1PL in register IT01CF (see SFR Definition 10.5. "IT01CF: INT0/INT1 Configuration" on page 105).

Bit6: **C/T1**: Counter/Timer 1 Select.
0: Timer Function: Timer 1 incremented by clock defined by T1M bit (CKCON.4).
1: Counter Function: Timer 1 incremented by high-to-low transitions on external input pin (T1).

Bits5–4: **T1M1–T1M0**: Timer 1 Mode Select.
These bits select the Timer 1 operation mode.

T1M1	T1M0	Mode
0	0	Mode 0: 13-bit counter/timer
0	1	Mode 1: 16-bit counter/timer
1	0	Mode 2: 8-bit counter/timer with auto-reload
1	1	Mode 3: Timer 1 inactive

Bit3: **GATE0**: Timer 0 Gate Control.
0: Timer 0 enabled when TR0 = 1 irrespective of $\overline{\text{INT0}}$ logic level.
1: Timer 0 enabled only when TR0 = 1 AND $\overline{\text{INT0}}$ is active as defined by bit IN0PL in register IT01CF (see SFR Definition 10.5. "IT01CF: INT0/INT1 Configuration" on page 105).

Bit2: **C/T0**: Counter/Timer Select.
0: Timer Function: Timer 0 incremented by clock defined by T0M bit (CKCON.3).
1: Counter Function: Timer 0 incremented by high-to-low transitions on external input pin (T0).

Bits1–0: **T0M1–T0M0**: Timer 0 Mode Select.
These bits select the Timer 0 operation mode.

T0M1	T0M0	Mode
0	0	Mode 0: 13-bit counter/timer
0	1	Mode 1: 16-bit counter/timer
1	0	Mode 2: 8-bit counter/timer with auto-reload
1	1	Mode 3: Two 8-bit counter/timers

19.2. Capture/Compare Modules

Each module can be configured to operate independently in one of six operation modes: Edge-triggered Capture, Software Timer, High Speed Output, Frequency Output, 8-Bit Pulse Width Modulator, or 16-Bit Pulse Width Modulator. Each module has Special Function Registers (SFRs) associated with it in the CIP-51 system controller. These registers are used to exchange data with a module and configure the module's mode of operation.

Table 19.2 summarizes the bit settings in the PCA0CPMn registers used to select the PCA capture/compare module's operating modes. Setting the ECCFn bit in a PCA0CPMn register enables the module's CCFn interrupt. Note that PCA0 interrupts must be globally enabled before individual CCFn interrupts are recognized. PCA0 interrupts are globally enabled by setting the EA bit and the EPCA0 bit to logic 1. See Figure 19.3 for details on the PCA interrupt configuration.

Table 19.2. PCA0CPM Register Settings for PCA Capture/Compare Modules

PWM16	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	Operation Mode
X	X	1	0	0	0	0	X	Capture triggered by positive edge on CEXn
X	X	0	1	0	0	0	X	Capture triggered by negative edge on CEXn
X	X	1	1	0	0	0	X	Capture triggered by transition on CEXn
X	1	0	0	1	0	0	X	Software Timer
X	1	0	0	1	1	0	X	High Speed Output
X	1	0	0	X	1	1	X	Frequency Output
0	1	0	0	X	0	1	X	8-Bit Pulse Width Modulator
1	1	0	0	X	0	1	X	16-Bit Pulse Width Modulator
X = Don't Care								

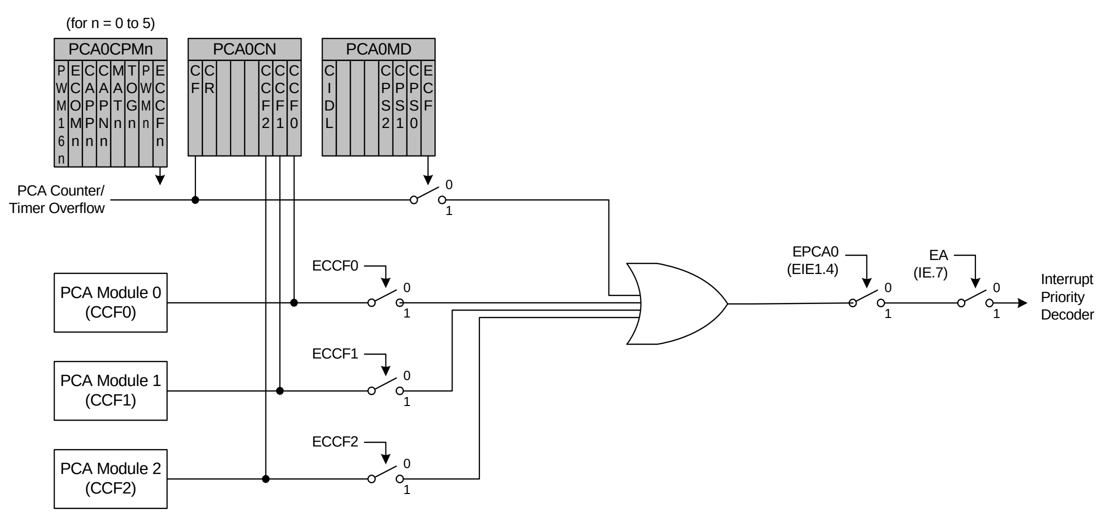


Figure 19.3. PCA Interrupt Block Diagram

21.2. C2 Pin Sharing

The C2 protocol allows the C2 pins to be shared with user functions so that in-system debugging and Flash programming functions may be performed. This is possible because C2 communication is typically performed when the device is in the halt state, where all on-chip peripherals and user software are stalled. In this halted state, the C2 interface can safely ‘borrow’ the C2CK (/RST) and C2D (P0.1 or P0.6) pins. In most applications, external resistors are required to isolate C2 interface traffic from the user application. A typical isolation configuration is shown in Figure 21.1.

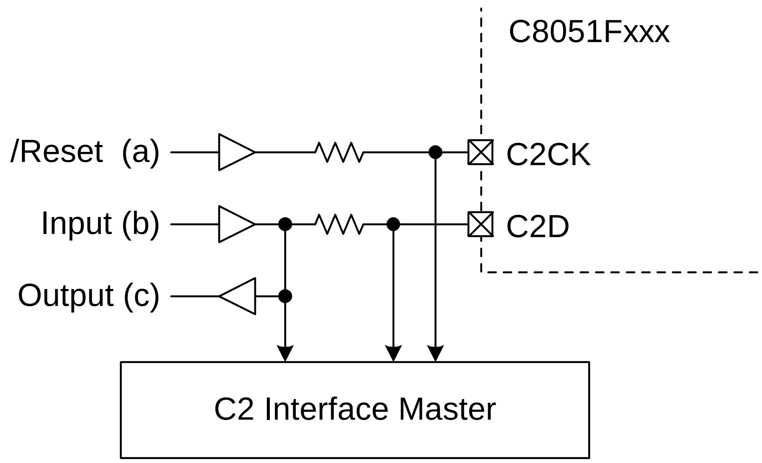


Figure 21.1. Typical C2 Pin Sharing

The configuration in Figure 21.1 assumes the following:

1. The user input (b) cannot change state while the target device is halted.
2. The /RST pin on the target device is used as an input only.

Additional resistors may be necessary depending on the specific application.