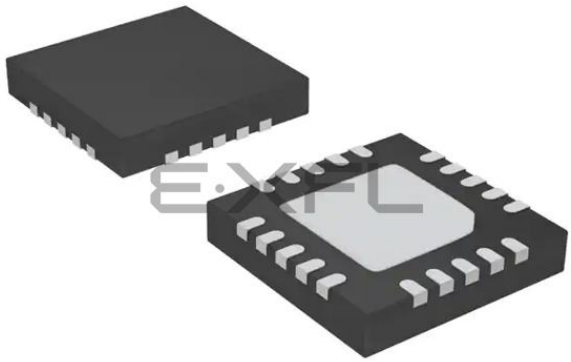

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f530a-imr

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1.4. Operating Modes

The C8051F52x/F52xA/F53x/F53xA devices have four operating modes: Active (Normal), Idle, Suspend, and Stop. Active mode occurs during normal operation when the oscillator and peripherals are active. Idle mode halts the CPU while leaving the peripherals and internal clocks active. In Suspend and Stop mode, the CPU is halted, all interrupts and timers are inactive, and the internal oscillator is stopped. The various operating modes are described in Table 1.3 below:

Table 1.3. Operating Modes Summary

	Properties	Power Consumption	How Entered?	How Exited?
Active	■ SYSCLK active ■ CPU active (accessing Flash) ■ Peripherals active or inactive depending on user settings	Full	—	—
Idle	■ SYSCLK active ■ CPU inactive (not accessing Flash) ■ Peripherals active or inactive depending on user settings	Less than Full	IDLE (PCON.0)	Any enabled interrupt or device reset
Suspend	■ Internal oscillator inactive ■ If SYSCLK is derived from the internal oscillator, the peripherals and the CIP-51 will be stopped	Low	SUSPEND (OSCICN.5)	Port 0 event match Port 1 event match Comparator 0 enabled and output is logic 0
Stop	■ SYSCLK inactive ■ CPU inactive (not accessing Flash) ■ Digital peripherals inactive; analog peripherals active or inactive depending on user settings	Very low	STOP (PCON.1)	Device Reset

See Section “8.3. Power Management Modes” on page 89 for Idle and Stop mode details. See Section “14.1.1. Internal Oscillator Suspend Mode” on page 136 for more information on Suspend mode.

1.5. 12-Bit Analog to Digital Converter

The C8051F52x/F52xA/F53x/F53xA devices include an on-chip 12-bit SAR ADC with a maximum throughput of 200 ksps. The ADC system includes a configurable analog multiplexer that selects the positive ADC input, which is measured with respect to GND. Ports 0 and 1 are available as ADC inputs; additionally, the ADC includes an innovative programmable gain stage which allows the ADC to sample inputs sources greater than the VREF voltage. The on-chip Temperature Sensor output and the core supply voltage (V_{DD}) are also available as ADC inputs. User firmware may shut down the ADC or use it in Burst Mode to save power.

Conversions can be initiated in four ways: a software command, an overflow of Timer 1, an overflow of Timer 2, or an external convert start signal. This flexibility allows the start of conversion to be triggered by software events, a periodic signal (timer overflows), or external HW signals. Conversion completions are indicated by a status bit and an interrupt (if enabled) and occur after 1, 4, 8, or 16 samples have been accumulated by a hardware accumulator. The resulting 12-bit to 16-bit data word is latched into the ADC data SFRs upon completion of a conversion. When the system clock is slow, Burst Mode allows ADC0 to automatically wake from a low power shutdown state, acquire and accumulate samples, then re-enter the low power shutdown state without CPU intervention.

Window compare registers for the ADC data can be configured to interrupt the controller when ADC data is either within or outside of a specified range. The ADC can monitor a key voltage continuously in background mode, but not interrupt the controller unless the converted data is within/outside the specified range.

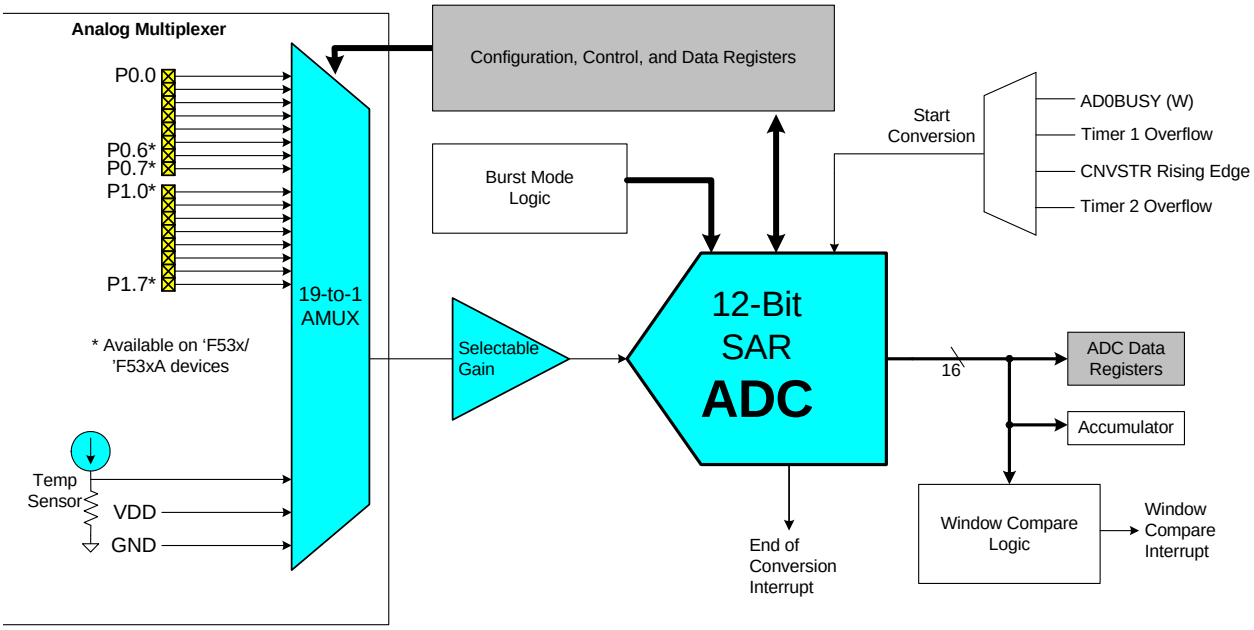


Figure 1.7. 12-Bit ADC Block Diagram

Table 2.3. ADC0 Electrical Characteristics

V_{DD} = 2.1 V, V_{REF} = 1.5 V (REFSL=0), –40 to +125 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
DC Accuracy					
Resolution			12		bits
Integral Nonlinearity		—	—	±3	LSB
Differential Nonlinearity	Guaranteed Monotonic	—	—	±1	LSB
Offset Error[1]		–10	±1	+10	LSB
Full Scale Error		–20	±1	+20	LSB
Dynamic Performance (10 kHz sine-wave Single-ended input, 0 to 1 dB below Full Scale, 200 ksps)					
Signal-to-Noise Plus Distortion		60	66	—	dB
Total Harmonic Distortion	Up to the 5th harmonic	—	74	—	dB
Spurious-Free Dynamic Range		—	88	—	dB
Conversion Rate					
SAR Conversion Clock		—	—	3	MHz
Burst Mode Oscillator		—	—	27	MHz
Conversion Time in SAR Clocks[2]		—	13	—	clocks
Track/Hold Acquisition Time[3,6]		1	—	—	µs
Throughput Rate[4]		—	—	200	ksps
Analog Inputs					
ADC Input Voltage Range[5]	gain = 1.0 (default) gain = n	0 0	— —	V_{REF} V_{REF} / n	V
Absolute Pin Voltage wrt to GND		0	—	V_{REGIN}	V
Sampling Capacitance		—	24	—	pF
Input Multiplexer Impedance		—	1.5	—	kΩ
Power Specifications					
Power Supply Current (from VDD)	Operating Mode, 200 ksps	—	1050	1400	µA
Burst Mode (Idle)		—	930	—	µA
Power-on Time		—	5	—	µs
Power Supply Rejection		—	1	—	mV/V

Notes:

1. Represents one standard deviation from the mean. Offset and full-scale error can be removed through calibration.
2. An additional 2 FCLK cycles are required to start and complete a conversion.
3. Additional tracking time may be required depending on the output impedance connected to the ADC input. See Section “4.3.6. Settling Time Requirements” on page 60.
4. An increase in tracking time will decrease the ADC throughput.
5. See Section “4.4. Selectable Gain” on page 60 for more information about setting the gain.
6. Additional tracking time might be needed ifVDD < 2.0 V; See Section “11.2.1. VDD Monitor Thresholds and Minimum VDD” on page 108 for minimum V_{DD} requirements.

Table 2.11. Internal Oscillator Electrical Characteristics

V_{DD} = 1.8 to 2.75 V, –40 to +125 °C unless otherwise specified; Using factory-calibrated settings.

Parameter	Conditions	Min	Typ	Max	Units
Oscillator Frequency[1]	IFCN = 111b VDD ≥ VREGMIN[2]	24.5 – 0.5%	24.5[3]	24.5 + 0.5%	MHz
	IFCN = 111b VDD < VREGMIN[2]	24.5 – 1.0%	24.5[3]	24.5 + 1.0%	
Oscillator Supply Current (from V_{DD})	Oscillator On OSCICN[7:6] = 11b	—	800	1100	µA
	Oscillator Suspend OSCICN[7:6] = 00b ZTCEN = 1				
	T = 25 °C	—	67	—	µA
	T = 85 °C	—	77	—	µA
	T = 125 °C	—	117	300	µA
	Oscillator Suspend OSCICN[7:6] = 00b ZTCEN = 0				
	T = 25 °C	—	2	—	µA
	T = 85 °C	—	3	—	µA
	T = 125 °C	—	50	—	µA
Wake-Up Time From Suspend	OSCICN[7:6] = 00b ZTCEN = 0[4]	—	—	1	µs
	OSCICN[7:6] = 00b ZTCEN = 1	—	5	—	Instruction Cycles
Power Supply Sensitivity	Constant Temperature	—	0.10	—	%/V
Temperature Sensitivity[5]	Constant Supply				
	TC_1	—	5.0	—	ppm/°C
	TC_2	—	–0.65	—	ppm/°C^2

Notes:

1. See Section “11.2.1. VDD Monitor Thresholds and Minimum VDD” on page 108 for minimum V_{DD} requirements.
2. VREGMIN is the minimum output of the voltage regulator for its low setting (REG0CN: REG0MD = 0b). See Table 2.6, “Voltage Regulator Electrical Specifications,” on page 30.
3. This is the average frequency across the operating temperature range.
4. See “20.7. Internal Oscillator Suspend Mode” on page 212 for ZTCEN setting in older silicon revisions.
5. Use temperature coefficients TC_1 and TC_2 to calculate the new internal oscillator frequency using the following equation:

$$f(T) = f0 \times (1 + TC_1 \times (T - T0) + TC_2 \times (T - T0)^2)$$

where f0 is the internal oscillator frequency at 25 °C and T0 is 25 °C.

Table 3.4. Pin Definitions for the C8051F53x and C805153xA (TSSOP 20) (Continued)

Name	Pin Numbers		Type	Description
	'F53xA 'F53x-C	'F53x		
V_{REGIN}	7	7		On-Chip Voltage Regulator Input.
P1.7	8	8	D I/O or A In	Port 1.7. See Port I/O Section for a complete description.
P1.6	9	9	D I/O or A In	Port 1.6. See Port I/O Section for a complete description.
P1.5	10	10	D I/O or A In	Port 1.5. See Port I/O Section for a complete description.
P1.4	11	11	D I/O or A In	Port 1.4. See Port I/O Section for a complete description.
P1.3	12	12	D I/O or A In	Port 1.3. See Port I/O Section for a complete description.
P1.2/ CNVSTR	13	13	D I/O or A In D In	Port 1.2. See Port I/O Section for a complete description. External Converter start input for the ADC0, see Section "4. 12-Bit ADC (ADC0)" on page 52 for a complete description.
P1.1	14	14	D I/O or A In	Port 1.1. See Port I/O Section for a complete description.
P1.0/ XTAL2	15	15	D I/O or A In D I/O	Port 1.0. See Port I/O Section for a complete description. External Clock Output. For an external crystal or resonator, this pin is the excitation driver. This pin is the external clock input for CMOS, capacitor, or RC oscillator configurations. See Section "14. Oscillators" on page 135.
P0.7/ XTAL1	16	16	D I/O or A In A In	Port 0.7. See Port I/O Section for a complete description. External Clock Input. This pin is the external oscillator return for a crystal or resonator. Section "14. Oscillators" on page 135.
P0.6/ C2D	17	17	D I/O or A In D I/O	Port 0.6. See Port I/O Section for a complete description. Bi-directional data signal for the C2 Debug Interface.
P0.5/RX*	18	—	D I/O or A In	Port 0.5. See Port I/O Section for a complete description.
P0.5	—	18	D I/O or A In	Port 0.5. See Port I/O Section for a complete description.
***Note:** Please refer to Section "20. Device Specific Behavior" on page 210.				

Table 3.7. Pin Definitions for the C8051F53x and C805153xA (QFN 20)

Name	Pin Numbers		Type	Description
	‘F53xA ‘F53x-C	‘F53x		
$\overline{RST}$/ C2CK	1	1	D I/O D I/O	Device Reset. Open-drain output of internal POR or V_{DD} monitor. An external source can initiate a system reset by driving this pin low for at least the minimum $\overline{RST}$ low time to generate a system reset, as defined in Table 2.8 on page 32. A 1 kΩ pullup to V_{REGIN} is recommended. See Reset Sources Section for a complete description. Clock signal for the C2 Debug Interface.
P0.0/ V_{REF}	2	2	D I/O or A In A O or D In	Port 0.0. See Port I/O Section for a complete description. External V_{REF} Input. See V_{REF} Section.
GND	3	3		Ground.
V_{DD}	4	4		Core Supply Voltage.
V_{REGIN}	5	5		On-Chip Voltage Regulator Input.
P1.7	6	6	D I/O or A In	Port 1.7. See Port I/O Section for a complete description.
P1.6	7	7	D I/O or A In	Port 1.6. See Port I/O Section for a complete description.
P1.5	8	8	D I/O or A In	Port 1.5. See Port I/O Section for a complete description.
P1.4	9	9	D I/O or A In	Port 1.4. See Port I/O Section for a complete description.
P1.3	10	10	D I/O or A In	Port 1.3. See Port I/O Section for a complete description.
P1.2/ CNVSTR	11	11	D I/O or A In D In	Port 1.2. See Port I/O Section for a complete description. External Converter start input for the ADC0, see Section “4. 12-Bit ADC (ADC0)” on page 52 for a complete description.
P1.1	12	12	D I/O or A In	Port 1.1. See Port I/O Section for a complete description.
Note: Please refer to Section “20. Device Specific Behavior” on page 210.				

Table 3.9. QFN-20 Landing Diagram Dimensions

Symbol	Min	Max
C1	3.90	4.00
C2	3.90	4.00
E	0.50 BSC.	
X1	0.20	0.30
X2	2.75	2.85
Y1	0.65	0.75
Y2	2.75	2.85

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

Solder Mask Design

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 2x2 array of 1.10 x 1.10 mm openings on 1.30 mm pitch should be used for the center ground pad.

Card Assembly

8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

4.5. Programmable Window Detector

The ADC Programmable Window Detector continuously compares the ADC0 output registers to user-programmed limits, and notifies the system when a desired condition is detected. This is especially effective in an interrupt-driven system, saving code space and CPU bandwidth while delivering faster system response times. The window detector interrupt flag (AD0WINT in register ADC0CN) can also be used in polled mode. The ADC0 Greater-Than (ADC0GTH, ADC0GTL) and Less-Than (ADC0LTH, ADC0LTL) registers hold the comparison values. The window detector flag can be programmed to indicate when measured data is inside or outside of the user-programmed limits, depending on the contents of the ADC0 Less-Than and ADC0 Greater-Than registers.

SFR Definition 4.10. ADC0GTH: ADC0 Greater-Than Data High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xC4

Bits7–0: High byte of ADC0 Greater-Than Data Word.

SFR Definition 4.11. ADC0GTL: ADC0 Greater-Than Data Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xC3

Bits7–0: Low byte of ADC0 Greater-Than Data Word.

SFR Definition 10.2. IP: Interrupt Priority

R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	PSPI0	PT2	PS0	PT1	PX1	PT0	PX0	10000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable
							SFR Address:	0xB8

Bit7: **UNUSED**. Read = 1b; Write = don't care.
Bit6: **PSPI0**: Serial Peripheral Interface (SPI0) Interrupt Priority Control.
This bit sets the priority of the SPI0 interrupt.
0: SPI0 interrupt set to low priority level.
1: SPI0 interrupt set to high priority level.
Bit5: **PT2**: Timer 2 Interrupt Priority Control.
This bit sets the priority of the Timer 2 interrupt.
0: Timer 2 interrupt set to low priority level.
1: Timer 2 interrupt set to high priority level.
Bit4: **PS0**: UART0 Interrupt Priority Control.
This bit sets the priority of the UART0 interrupt.
0: UART0 interrupt set to low priority level.
1: UART0 interrupt set to high priority level.
Bit3: **PT1**: Timer 1 Interrupt Priority Control.
This bit sets the priority of the Timer 1 interrupt.
0: Timer 1 interrupt set to low priority level.
1: Timer 1 interrupt set to high priority level.
Bit2: **PX1**: External Interrupt 0 Priority Control.
This bit sets the priority of the external interrupt 1.
0: INT1 interrupt set to low priority level.
1: INT1 interrupt set to high priority level.
Bit1: **PT0**: Timer 0 Interrupt Priority Control.
This bit sets the priority of the Timer 0 interrupt.
0: Timer 0 interrupt set to low priority level.
1: Timer 0 interrupt set to high priority level.
Bit0: **PX0**: External Interrupt 0 Priority Control.
This bit sets the priority of the external interrupt 0.
0: INT0 interrupt set to low priority level.
1: INT0 interrupt set to high priority level.

11.1. Power-On Reset

During power-up, the device is held in a reset state and the $\overline{RST}$ pin is driven low until V_{DD} settles above V_{RST}. V_{DD} ramp time is defined as how fast V_{DD} ramps from 0 V to V_{RST}. An additional delay ($T_{PORDelay}$) occurs before the device is released from reset. The V_{RST} threshold and $T_{PORDelay}$ are specified in Table 2.8, “Reset Electrical Characteristics,” on page 32. Figure 11.2 plots the power-on and V_{DD} monitor reset timing.

Note: Please refer to Section “20.4. VDD Monitors and VDD Ramp Time” on page 211 for definition of V_{RST} and V_{DD} ramp time in older silicon revisions A and B.

On exit from a power-on reset, the PORSF flag (RSTSRC.1) is set by hardware to logic 1. When PORSF is set, all of the other reset flags in the RSTSRC Register are indeterminate (PORSF is cleared by all other resets). Since all resets cause program execution to begin at the same location (0x0000), software can read the PORSF flag to determine if a power-up was the cause of reset. The contents of internal data memory should be assumed to be undefined after a power-on reset. Both the V_{DD} monitors (VDDMON0 and VDDMON1) are enabled following a power-on reset.

Note: Please refer to Section “11.2.1. VDD Monitor Thresholds and Minimum VDD” on page 108 for recommendations related to minimum V_{DD}.

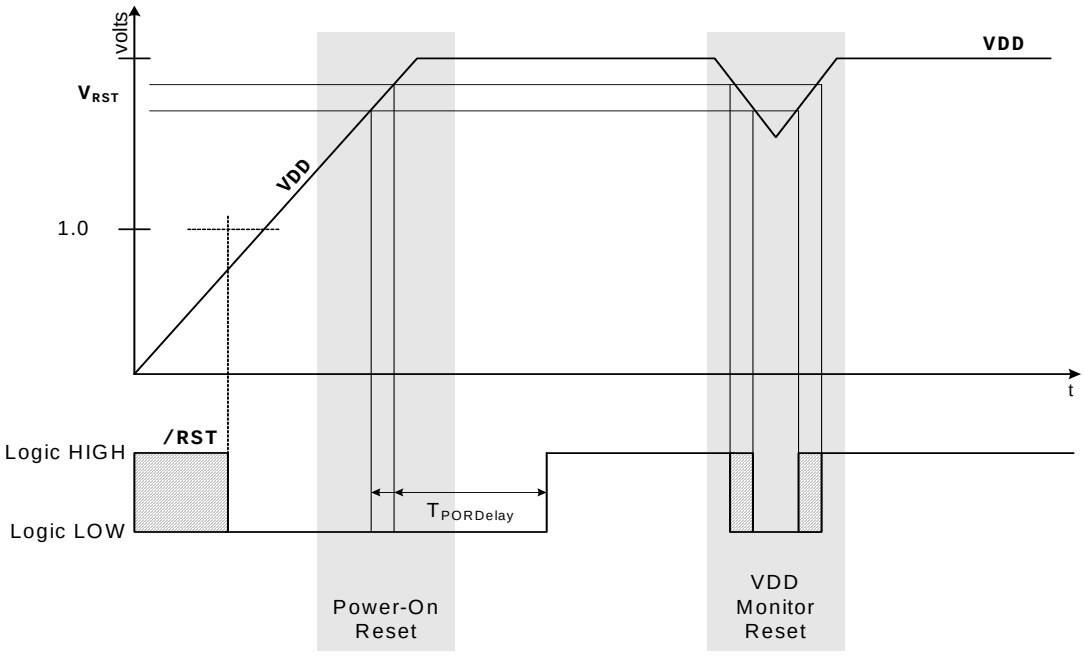
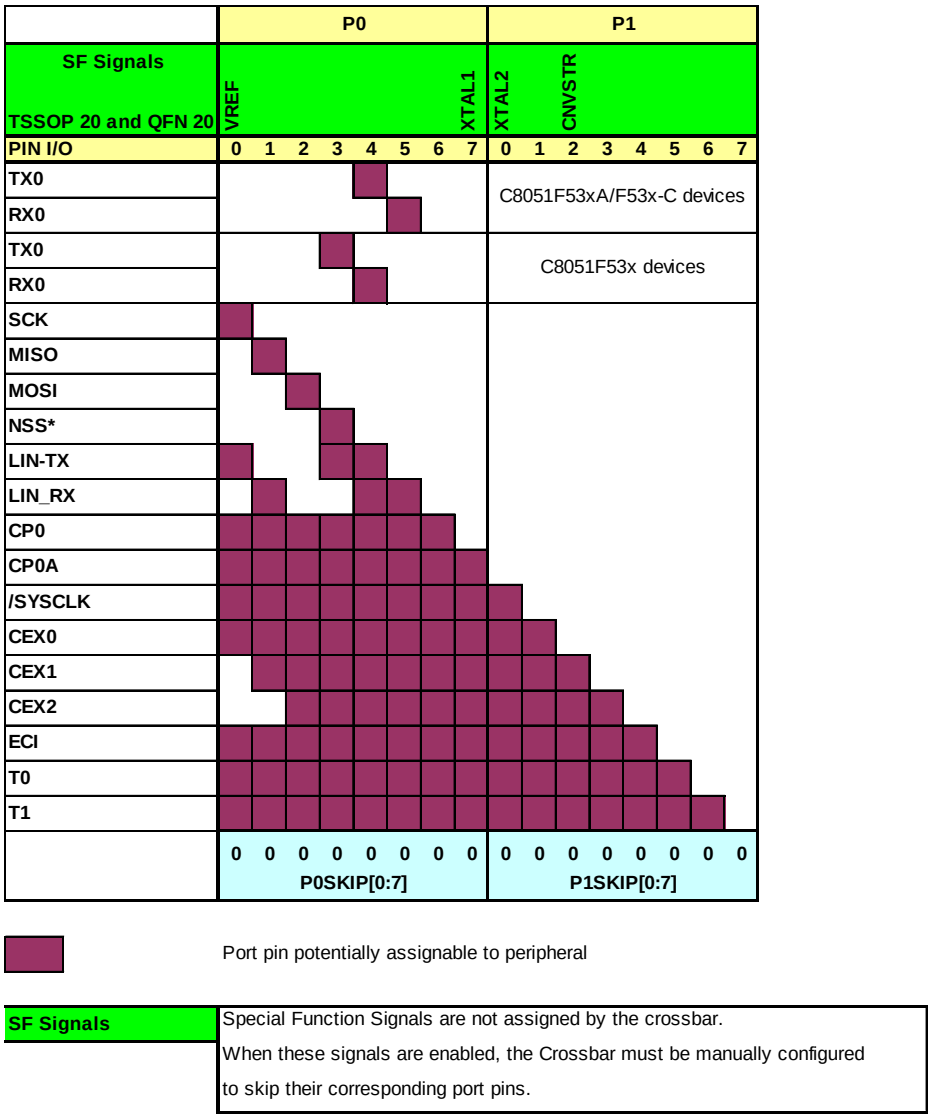


Figure 11.2. Power-On and V_{DD} Monitor Reset Timing

13.1. Priority Crossbar Decoder

The Priority Crossbar Decoder (Figure 13.3) assigns a priority to each I/O function, starting at the top with UART0. When a digital resource is selected, the least-significant unassigned Port pin is assigned to that resource (excluding UART0, which will be assigned to pins P0.4 and P0.5). If a Port pin is assigned, the Crossbar skips that pin when assigning the next selected resource. Additionally, the Crossbar will skip Port pins whose associated bits in the PnSKIP registers are set. The PnSKIP registers allow software to skip Port pins that are to be used for analog input, dedicated functions, or GPIO.



Note: 4-Wire SPI Only.

Figure 13.3. Crossbar Priority Decoder with No Pins Skipped (TSSOP 20 and QFN 20)

Important Note on Crossbar Configuration: If a Port pin is claimed by a peripheral without use of the Crossbar, its corresponding PnSKIP bit should be set. This applies to P1.0 and/or P0.7 (F53x/F53xA) or P0.2 and/or P0.3 (F52x/F52xA) for the external oscillator, P0.0 for V_{REF}, P1.2 (F53x/F53xA) or P0.5

SFR Definition 13.1. XBR0: Port I/O Crossbar Register 0

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	CP0AE	CP0E	SYSCKE	LINE	SPI0E	URT0E	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xE1

Bit7–6: **RESERVED**. Read = 00b; Must write 00b.
Bit5: **CP0AE**: Comparator0 Asynchronous Output Enable
0: Asynchronous CP0 unavailable at Port pin.
1: Asynchronous CP0 routed to Port pin.
Bit4: **CP0E**: Comparator0 Output Enable
0: CP0 unavailable at Port pin.
1: CP0 routed to Port pin.
Bit3: **SYSCKE**: /SYSCLK Output Enable
0: /SYSCLK unavailable at Port pin.
1: /SYSCLK output routed to Port pin.
Bit2: **LINE**. Lin Output Enable
Bit1: **SPI0E**: SPI I/O Enable
0: SPI I/O unavailable at Port pins.
1: SPI I/O routed to Port pins. Note that the SPI can be assigned either 3 or 4 GPIO pins.
Bit0: **URT0E**: UART I/O Output Enable
0: UART I/O unavailable at Port pin.
1: UART TX0, RX0 routed to Port pins (P0.3 and P0.4) or (P0.4 and P0.5).*

Note: Refer to Section “20. Device Specific Behavior” on page 210.

SFR Definition 13.13. P0SKIP: Port0 Skip

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xD4

Bits7–0: **P1SKIP[7:0]**: Port1 Crossbar Skip Enable Bits.
These bits select Port pins to be skipped by the Crossbar Decoder. Port pins used as analog inputs (for ADC or Comparator) or used as special functions (V_{REF} input, external oscillator circuit, CNVSTR input) should be skipped by the Crossbar.
0: Corresponding P1.n pin is not skipped by the Crossbar.
1: Corresponding P1.n pin is skipped by the Crossbar.

SFR Definition 13.14. P1MAT: Port1 Match

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xCF

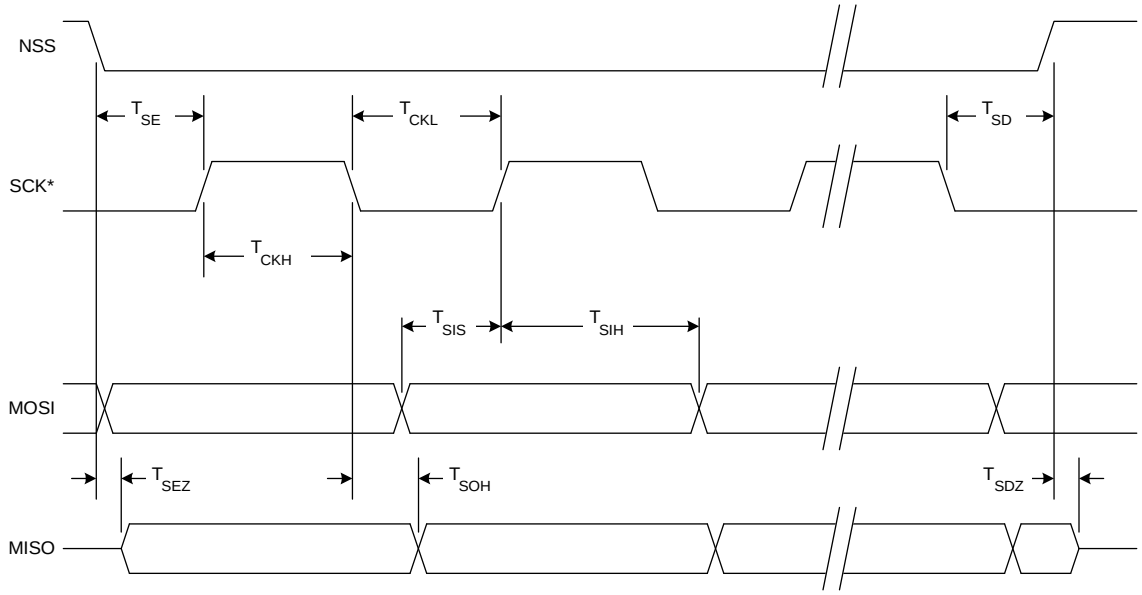
Bits7–0: **P1MAT[7:0]**: Port1 Match Value.
These bits control the value that unmasked P0 Port pins are compared against. A Port Match event is generated if (P1 & P1MASK) does not equal (P1MAT & P1MASK).

SFR Definition 13.15. P1MASK: Port1 Mask

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

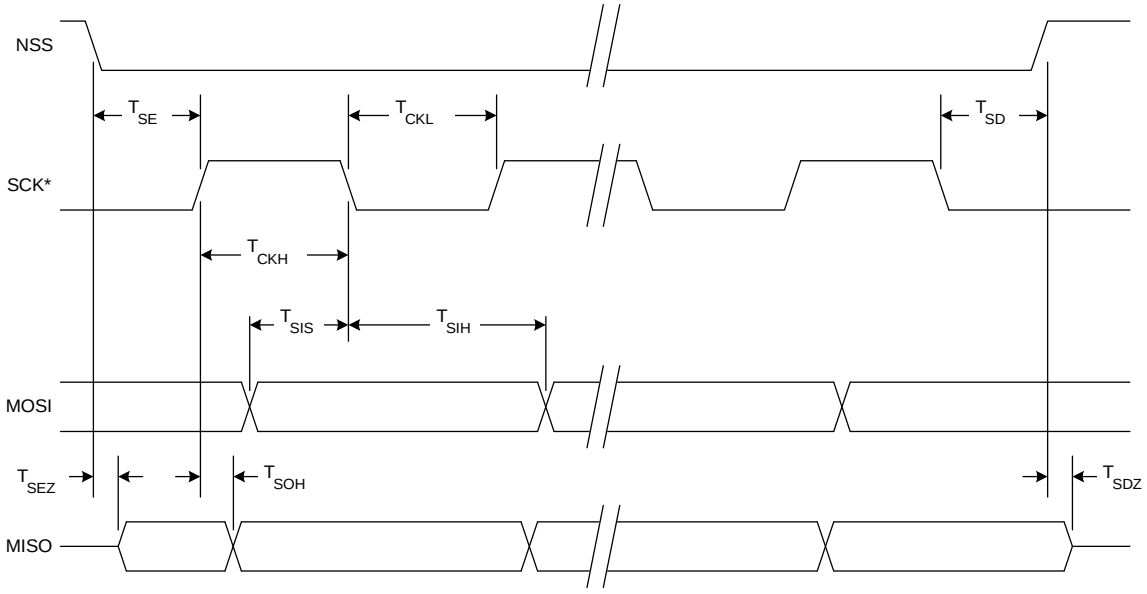
SFR Address: 0xBF

Bits7–0: **P1MASK[7:0]**: Port1 Mask Value.
These bits select which Port pins will be compared to the value stored in P1MAT.
0: Corresponding P1.n pin is ignored and cannot cause a Port Match event.
1: Corresponding P1.n pin is compared to the corresponding bit in P1MAT.



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 16.8. SPI Slave Timing (CKPHA = 0)



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 16.9. SPI Slave Timing (CKPHA = 1)

Table 17.1. Baud-Rate Calculation Variable Ranges

Factor	Range
prescaler	0…3
multiplier	0…31
divider	200…511

Important: The minimum system clock (SYSCLK) to operate the LIN peripheral is 8 MHz.

Use the following equations to calculate the values for the variables for the baud-rate equation:

$$multiplier = \frac{20000}{baud\_rate} - 1$$

$$prescaler = ln\left[\frac{SYSCLK}{(multiplier + 1) \times baud\_rate \times 200}\right] \times \frac{1}{ln2} - 1$$

$$divider = \frac{SYSCLK}{(2^{(\text{prescaler} + 1)} \times (multiplier + 1) \times baud\_rate)}$$

It is important to note that in all these equations, the results must be rounded down to the nearest integer.

The following example shows the steps for calculating the baud rate values for a Master node running at 24.5 MHz and communicating at 19200 bits/sec. First, calculate the multiplier:

$$multiplier = \frac{20000}{19200} - 1 = 0.0417 \cong 0$$

Next, calculate the prescaler:

$$prescaler = ln\frac{24500000}{(0 + 1) \times 19200 \times 200} \times \frac{1}{ln2} - 1 = 1.674 \cong 1$$

Finally, calculate the divider:

$$divider = \frac{24500000}{2^{(1 + 1)} \times (0 + 1) \times 19200} = 319.010 \cong 319$$

These values lead to the following baud rate:

$$baud\_rate = \frac{24500000}{2^{(1 + 1)} \times (0 + 1) \times 319} \cong 19200.63$$

17.2.4. Baud Rate Calculations—Automatic Mode

If the LIN peripheral is configured for slave mode, only the prescaler and divider need to be calculated:

$$prescaler = ln\left[\frac{SYSCLK}{4000000}\right] \times \frac{1}{ln2} - 1$$

$$divider = \frac{SYSCLK}{2^{(prescaler+1)} \times 20000}$$

The following example calculates the values of these variables for a 24 MHz system clock:

$$prescaler = ln\left[\frac{24500000}{4000000}\right] \times \frac{1}{ln2} - 1 = 1.615 \cong 1$$

$$divider = \frac{24500000}{2^{(1+1)} \times 20000} = 306.25 \cong 306$$

Table 17.3 presents some typical values of system clock and baud rate along with their factors.

Table 17.3. Autobaud Parameters Examples

System Clock (MHz)	Prescaler	Divider
25	1	312
24.5	1	306
24	1	300
22.1184	1	276
16	1	200
12.25	0	306
12	0	300
11.0592	0	276
8	0	200

19.2.1. Edge-triggered Capture Mode

In this mode, a valid transition on the CEXn pin causes the PCA to capture the value of the PCA counter/timer and load it into the corresponding module's 16-bit capture/compare register (PCA0CPLn and PCA0CPHn). The CAPPn and CAPNn bits in the PCA0CPMn register are used to select the type of transition that triggers the capture: low-to-high transition (positive edge), high-to-low transition (negative edge), or either transition (positive or negative edge). When a capture occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1 and an interrupt request is generated if CCF interrupts are enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. If both CAPPn and CAPNn bits are set to logic 1, then the state of the Port pin associated with CEXn can be read directly to determine whether a rising-edge or falling-edge caused the capture.

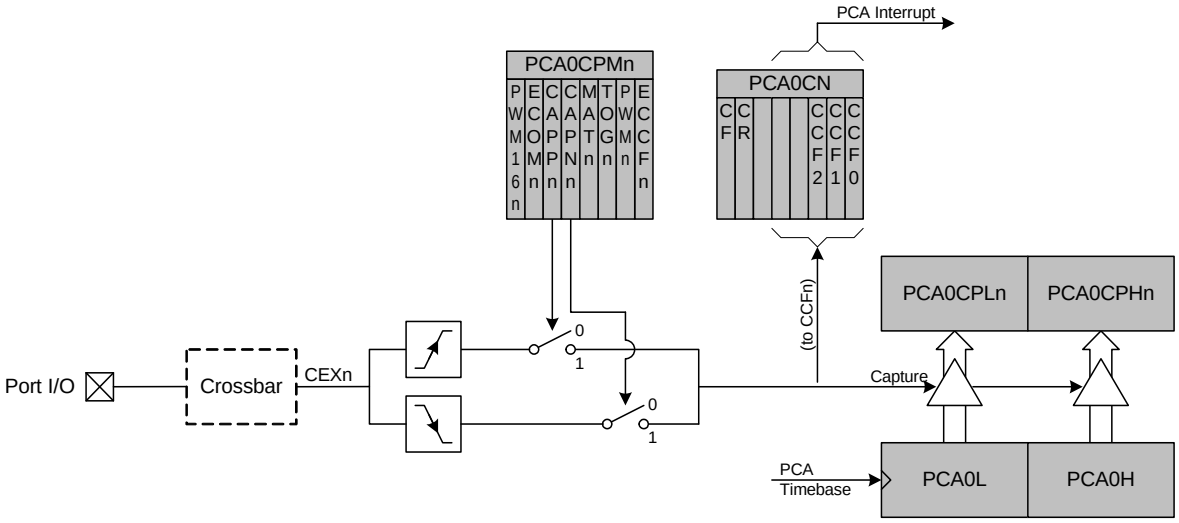


Figure 19.4. PCA Capture Mode Diagram

Note: The CEXn input signal must remain high or low for at least 2 system clock cycles to be recognized by the hardware.

20. Device Specific Behavior

This chapter contains behavioral differences between the silicon revisions of C8051F52x/52xA/F53x/53xA devices.

These differences do not affect the functionality or performance of most systems and are described below.

20.1. Device Identification

The Part Number Identifier on the top side of the device package can be used for decoding device information. The first character of the trace code identifies the silicon revision. On C8051F52x-C/53x-C devices, the trace code (second line on the TSSOP-20 and DFN-10 packages; third line on the QFN-20 package) will begin with the letter "C". The "A" suffix at the end of the part number such as "C8051F530A" is only present on Revision B devices. All other revisions do not include this suffix. Figures 20.1, 20.2, and 20.3 show how to find the part number on the top side of the device package.

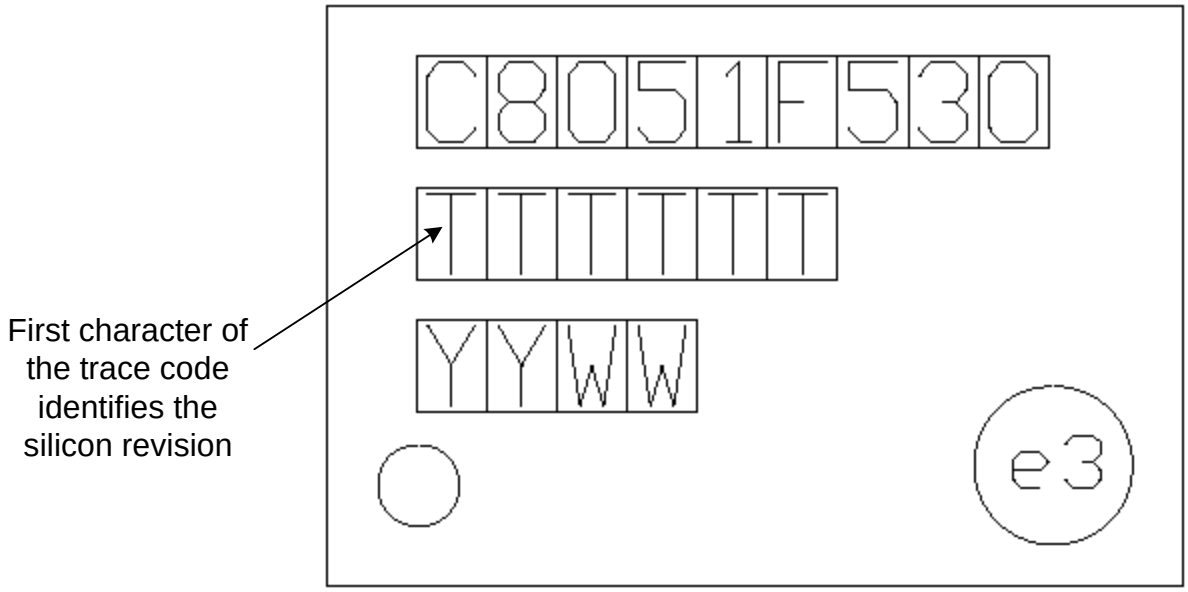


Figure 20.1. Device Package—TSSOP 20

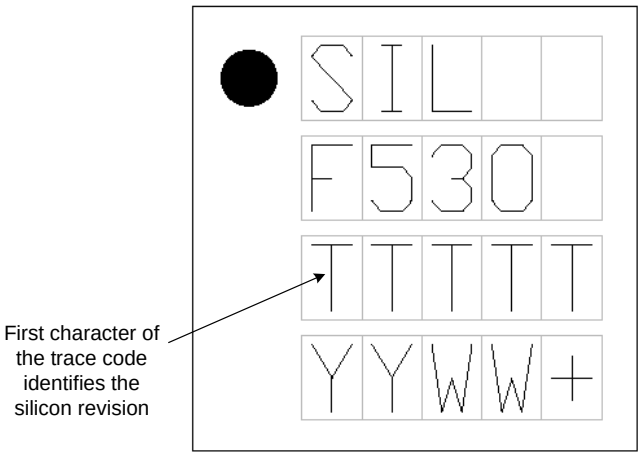


Figure 20.2. Device Package—QFN 20

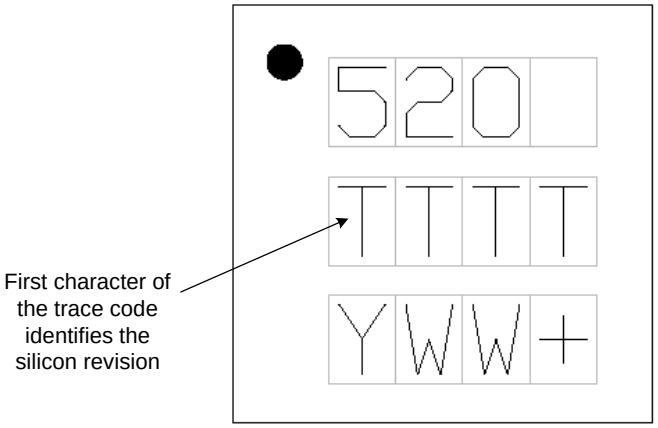


Figure 20.3. Device Package—DFN 10

20.2. Reset Pin Behavior

The reset behavior differs between the silicon revisions of C8051F52x/52xA/F53x/F53xA devices. The differences affect the state of the $\overline{\text{RST}}$ pin during a VDD Monitor reset.

On Revision A devices, a V_{DD} Monitor reset does not affect the state of the $\overline{\text{RST}}$ pin. On Revision B and Revision C devices, a V_{DD} Monitor reset will pull the $\overline{\text{RST}}$ pin low for the duration of the brownout condition.

20.3. Reset Time Delay

The reset time delay differs between the silicon revisions of C8051F52x/52xA/F53x/F53xA devices.

On Revision A devices, the reset time delay will be as long as 80 ms following a power-on reset, meaning it can take up to 80 ms to begin code execution. Subsequent resets will not cause the long delay. On Revision B and Revision C devices, the startup time is around 350 µs, specified as $T_{PORDELAY}$ in Table 2.8, “Reset Electrical Characteristics,” on page 32.

20.4. V_{DD} Monitors and V_{DD} Ramp Time

The number of V_{DD} monitors and definition of “V_{DD} ramp time” differs between the silicon revisions of C8051F52x/52xA/F53x/F53xA devices.

On Revision A and Revision B devices, the only V_{DD} monitor present is the standard V_{DD} monitor (VDDMON0). On these devices, the V_{DD} ramp time is defined as how fast V_{DD} ramps from 0 V to V_{RST}. Here, V_{RST} is the $V_{RST-LOW}$ threshold of VDDMON0 specifed in Table 2.8, “Reset Electrical Characteristics,” on page 32. The maximum V_{DD} ramp time for these devices is 1 ms; slower ramp times may cause the device to be released from reset before V_{DD} reaches the $V_{RST-LOW}$ level.

Revision C devices include two V_{DD} monitors: a standard V_{DD} monitor (VDDMON0) and a level-sensitive V_{DD} monitor (VDDMON1). See Section 11.2 on page 108 for more details. On these devices, the V_{DD} ramp time is defined as how fast V_{DD} ramps from 0 V to V_{RST1}. V_{RST1} is specified in Table 2.8, “Reset Electrical Characteristics,” on page 32 as the threshold of the new level-sensitive V_{DD} monitor (VDDMON1). This new V_{DD} monitor will hold the device in reset until V_{DD} reaches the V_{RST1} level irrespective of the length of the V_{DD} ramp time.

Note: Please refer to Section “11.2.1. VDD Monitor Thresholds and Minimum VDD” on page 108 for recommendations related to minimum V_{DD}.