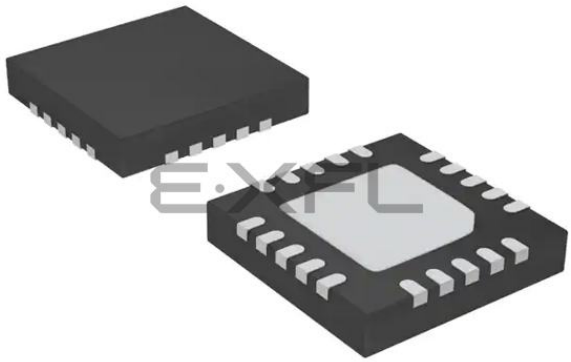


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f531a-imr

Table of Contents

Table 2.4. Temperature Sensor Electrical Characteristics

V_{DD} = 2.1 V, V_{REF} = 1.5 V (REFSL=0), –40 to +125 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Linearity[1]		—	0.1	—	°C
Gain[1]		—	3.33	—	mV/°C
Gain Error[2]		—	±100	—	µV/°C
Offset[1]	Temp = 0 °C	—	890	—	mV
Offset Error[2]	Temp = 0 °C	—	±15	—	mV
Tracking Time		12	—	—	µs
Power Supply Current		—	17	—	µA

Notes:
1. Includes ADC offset, gain, and linearity variations.
2. Represents one standard deviation from the mean.

Table 2.5. Voltage Reference Electrical Characteristics

V_{DD} = 2.1 V; –40 to +125 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Internal Reference (REFBE = 1)					
Output Voltage	I_{DD} ≈ 1 mA; No load on VREF pin and all other GPIO pins. 25 °C ambient (REFLV = 0) 25 °C ambient (REFLV = 1), V_{DD} = 2.6 V	 1.45 2.15	 1.5 2.2	 1.55 2.25	 V
V_{REF} Short-Circuit Current		—	2.5	—	mA
V_{REF} Temperature Coefficient		—	33	—	ppm/°C
Load Regulation	Load = 0 to 200 µA to GND	—	10	—	ppm/µA
V_{REF} Turn-on Time 1	4.7 µF, 0.1 µF bypass	—	21	—	ms
V_{REF} Turn-on Time 2	0.1 µF bypass	—	230	—	µs
Power Supply Rejection		—	2.1	—	mV/V
External Reference (REFBE = 0)					
Input Voltage Range		0	—	V_{DD}	V
Input Current	Sample Rate = 200 ksps; V_{REF} = 1.5 V	—	2.4	—	µA
Bias Generators					
ADC Bias Generator	BIASE = 1	—	22	—	µA
Power Consumption (Internal)		—	35	—	µA

Table 2.6. Voltage Regulator Electrical Specifications

V_{DD} = 2.1 or 2.6 V; –40 to +125 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Input Voltage Range (V_{REGIN})	C8051F52x/53x	2.7[1]	—	5.25	V
	C8051F52xA/53xA				
	V_{DD} connected to V_{REGIN}	1.8	—	2.7	
	V_{DD} not connected to V_{REGIN}	2.2[2]	—	5.25	
	C8051F52x-C/53x-C				
	V_{DD} connected to V_{REGIN}	2.0	—	2.75	
	V_{DD} not connected to V_{REGIN}	2.2[2]	—	5.25	
Dropout Voltage (V_{DO})	Output Current = 1-50 mA	—	10	—	mV/mA
Output Voltage (V_{DD})	Output Current = 1 to 50 mA				V
	REG0MD = 0	2.0	2.1	2.25	
	REG0MD = 1	2.5	2.6	2.75	
Bias Current	2.1 V operation (REG0MD = 0; T = 25 °C)	—	1	5	µA
	2.6 V operation (REG0MD = 1; T = 25 °C)	—	1	5	
Dropout Indicator Detection Threshold		—	75	—	mV
Output Voltage Temperature Coefficient		—	0.25	—	mV/ºC
VREG Settling Time	50 mA load with V_{REGIN} = 2.4 V and V_{DD} load capacitor of 4.8 µF	—	250	—	µs

Notes:

1. The minimum input voltage is 2.7 V or V_{DD} + V_{DO}(max load), whichever is greater.
2. The minimum input voltage is 2.2 V or V_{DD} + V_{DO}(max load), whichever is greater.

Table 2.11. Internal Oscillator Electrical Characteristics

V_{DD} = 1.8 to 2.75 V, –40 to +125 °C unless otherwise specified; Using factory-calibrated settings.

Parameter	Conditions	Min	Typ	Max	Units
Oscillator Frequency[1]	IFCN = 111b VDD ≥ VREGMIN[2]	24.5 – 0.5%	24.5[3]	24.5 + 0.5%	MHz
	IFCN = 111b VDD < VREGMIN[2]	24.5 – 1.0%	24.5[3]	24.5 + 1.0%	
Oscillator Supply Current (from V_{DD})	Oscillator On OSCICN[7:6] = 11b	—	800	1100	µA
	Oscillator Suspend OSCICN[7:6] = 00b ZTCEN = 1				
	T = 25 °C	—	67	—	µA
	T = 85 °C	—	77	—	µA
	T = 125 °C	—	117	300	µA
	Oscillator Suspend OSCICN[7:6] = 00b ZTCEN = 0				
	T = 25 °C	—	2	—	µA
	T = 85 °C	—	3	—	µA
	T = 125 °C	—	50	—	µA
Wake-Up Time From Suspend	OSCICN[7:6] = 00b ZTCEN = 0[4]	—	—	1	µs
	OSCICN[7:6] = 00b ZTCEN = 1	—	5	—	Instruction Cycles
Power Supply Sensitivity	Constant Temperature	—	0.10	—	%/V
Temperature Sensitivity[5]	Constant Supply				
	TC_1	—	5.0	—	ppm/°C
	TC_2	—	–0.65	—	ppm/°C^2

Notes:

1. See Section “11.2.1. VDD Monitor Thresholds and Minimum VDD” on page 108 for minimum V_{DD} requirements.
2. VREGMIN is the minimum output of the voltage regulator for its low setting (REG0CN: REG0MD = 0b). See Table 2.6, “Voltage Regulator Electrical Specifications,” on page 30.
3. This is the average frequency across the operating temperature range.
4. See “20.7. Internal Oscillator Suspend Mode” on page 212 for ZTCEN setting in older silicon revisions.
5. Use temperature coefficients TC_1 and TC_2 to calculate the new internal oscillator frequency using the following equation:

$$f(T) = f0 \times (1 + TC_1 \times (T - T0) + TC_2 \times (T - T0)^2)$$

where f0 is the internal oscillator frequency at 25 °C and T0 is 25 °C.

Table 3.1. Pin Definitions for the C8051F52x and C8051F52xA (DFN 10)

Name	Pin Numbers		Type	Description
	'F52xA 'F52x-C	'F52x		
$\overline{RST}$/	1	1	D I/O	Device Reset. Open-drain output of internal POR or V_{DD} monitor. An external source can initiate a system reset by driving this pin low for at least the minimum $\overline{RST}$ low time to generate a system reset, as defined in Table 2.8 on page 32. A 1 kΩ pullup to V_{REGIN} is recommended. See Reset Sources Section for a complete description.
C2CK			D I/O	Clock signal for the C2 Debug Interface.
P0.0/	2	2	D I/O or A In	Port 0.0. See Port I/O Section for a complete description.
V_{REF}			A O or D In	External V_{REF} Input. See V_{REF} Section.
GND	3	3		Ground.
V_{DD}	4	4		Core Supply Voltage.
V_{REGIN}	5	5		On-Chip Voltage Regulator Input.
P0.5/RX*/	6	—	D I/O or A In	Port 0.5. See Port I/O Section for a complete description.
CNVSTR			D In	External Converter start input for the ADC0, see Section "4. 12-Bit ADC (ADC0)" on page 52 for a complete description.
P0.5/	—	6	D I/O or A In	Port 0.5. See Port I/O Section for a complete description.
CNVSTR			D In	External Converter start input for the ADC0, see Section "4. 12-Bit ADC (ADC0)" on page 52 for a complete description.
P0.4/TX*	7	—	D I/O or A In	Port 0.4. See Port I/O Section for a complete description.
P0.4/RX*	—	7	D I/O or A In	Port 0.4. See Port I/O Section for a complete description.
P0.3	8	—	D I/O or A In	Port 0.3. See Port I/O Section for a complete description.
XTAL2			D I/O	External Clock Output. For an external crystal or resonator, this pin is the excitation driver. This pin is the external clock input for CMOS, capacitor, or RC oscillator configurations. See Section "14. Oscillators" on page 135.

Note: Please refer to Section "20. Device Specific Behavior" on page 210.

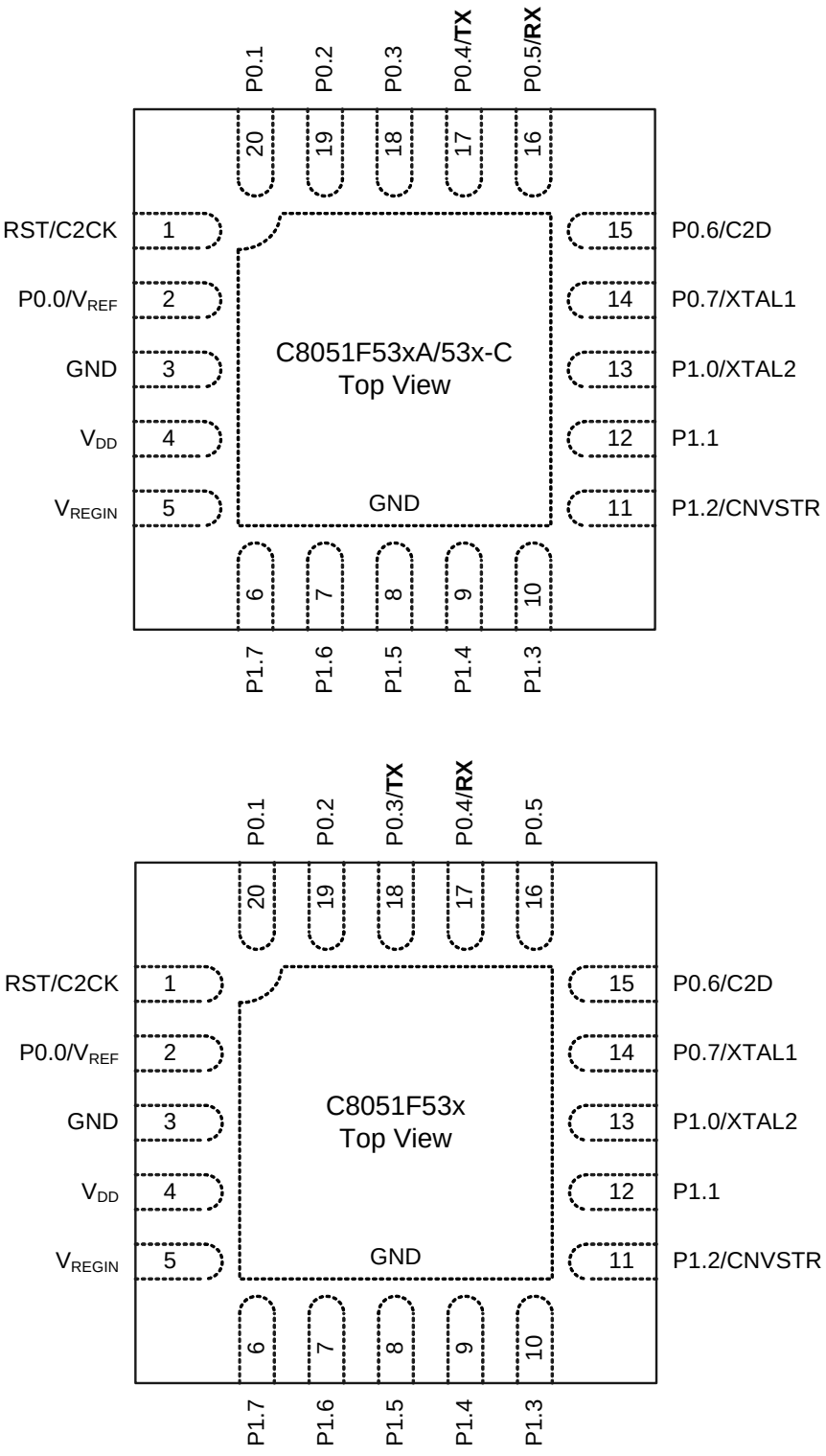


Figure 3.7. QFN-20 Pinout Diagram (Top View)

Table 3.8. QFN-20 Package Diagram Dimensions

Dimension	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D	4.00 BSC.		
D2	2.55	2.70	2.85
e	0.50 BSC.		
E	4.00 BSC.		
E2	2.55	2.70	2.85
L	0.30	0.40	0.50
L1	0.00	—	0.15
aaa	—	—	0.15
bbb	—	—	0.10
ddd	—	—	0.05
eee	—	—	0.08
Z	—	0.43	—
Y	—	0.18	—

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VGGD except for custom features D2, E2, Z, Y, L, and L1, which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

4.2. Temperature Sensor

An on-chip temperature sensor is included on the C8051F52x/F52xA/F53x/F53xA devices which can be directly accessed via the ADC0 multiplexer. To use ADC0 to measure the temperature sensor, the ADC multiplexer channel should be configured to connect to the temperature sensor. The temperature sensor transfer function is shown in Figure 5.2. The output voltage (V_{TEMP}) is the positive ADC input selected by bits AD0MX[4:0] in register ADC0MX. The TEMPE bit in register REF0CN enables/disables the temperature sensor, as described in SFR Definition 5.1. While disabled, the temperature sensor defaults to a high impedance state and any ADC measurements performed on the sensor will result in meaningless data. Refer to Table 5.1 for the slope and offset parameters of the temperature sensor.

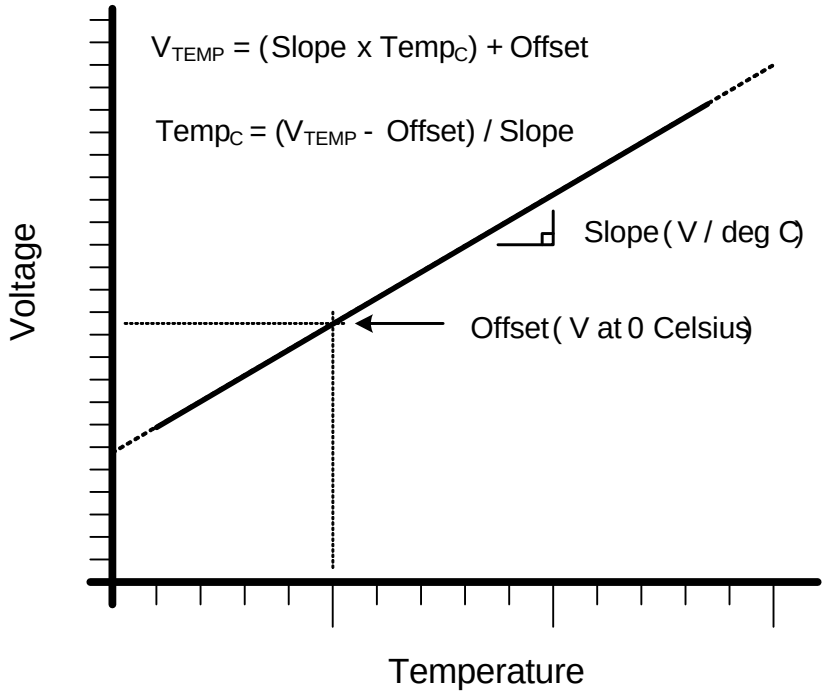


Figure 4.2. Typical Temperature Sensor Transfer Function

4.3.5. Output Conversion Code

The registers ADC0H and ADC0L contain the high and low bytes of the output conversion code. When the repeat count is set to 1, conversion codes are represented in 12-bit unsigned integer format and the output conversion code is updated after each conversion. Inputs are measured from 0 to V_{REF} x 4095/4096. Data can be right-justified or left-justified, depending on the setting of the AD0LJST bit (ADC0CN.2). Unused bits in the ADC0H and ADC0L registers are set to 0. Example codes are shown below for both right-justified and left-justified data.

Input Voltage	Right-Justified ADC0H:ADC0L (AD0LJST = 0)	Left-Justified ADC0H:ADC0L (AD0LJST = 1)
V_{REF} x 4095/4096	0x0FFF	0xFFF0
V_{REF} x 2048/4096	0x0800	0x8000
V_{REF} x 2047/4096	0x07FF	0x7FF0
0	0x0000	0x0000

When the ADC0 Repeat Count is greater than 1, the output conversion code represents the accumulated result of the conversions performed and is updated after the last conversion in the series is finished. Sets of 4, 8, or 16 consecutive samples can be accumulated and represented in unsigned integer format. The repeat count can be selected using the AD0RPT bits in the ADC0CF register. The value must be right-justified (AD0LJST = “0”), and unused bits in the ADC0H and ADC0L registers are set to '0'. The following example shows right-justified codes for repeat counts greater than 1. Notice that accumulating 2^n samples is equivalent to left-shifting by *n* bit positions when all samples returned from the ADC have the same value.

Input Voltage	Repeat Count = 4	Repeat Count = 8	Repeat Count = 16
V_{REF} x 4095/4096	0x3FFC	0x7FF8	0xFFF0
V_{REF} x 2048/4096	0x2000	0x4000	0x8000
V_{REF} x 2047/4096	0x1FFC	0x3FF8	0x7FF0
0	0x0000	0x0000	0x0000

7. Comparator

C8051F52x/F52xA/F53x/F53xA devices include one on-chip programmable voltage comparator. The Comparator is shown in Figure 7.1.

The Comparator offers programmable response time and hysteresis, an analog input multiplexer, and two outputs that are optionally available at the Port pins: a synchronous “latched” output (CP0), or an asynchronous “raw” output (CP0A). The asynchronous CP0A signal is available even when the system clock is not active. This allows the Comparator to operate and generate an output with the device in STOP or SUSPEND mode. When assigned to a Port pin, the Comparator output may be configured as open drain or push-pull (see Section “13.2. Port I/O Initialization” on page 126). The Comparator may also be used as a reset source (see Section “11.5. Comparator Reset” on page 110).

The Comparator inputs are selected in the CPT0MX register (SFR Definition 7.2). The CMX0P3–CMX0P0 bits select the Comparator0 positive input; the CMX0N3–CMX0N0 bits select the Comparator0 negative input.

Important Note About Comparator Inputs: The Port pins selected as Comparator inputs should be configured as analog inputs in their associated Port configuration register and configured to be skipped by the Crossbar (for details on Port configuration, see Section “13.3. General Purpose Port I/O” on page 128).

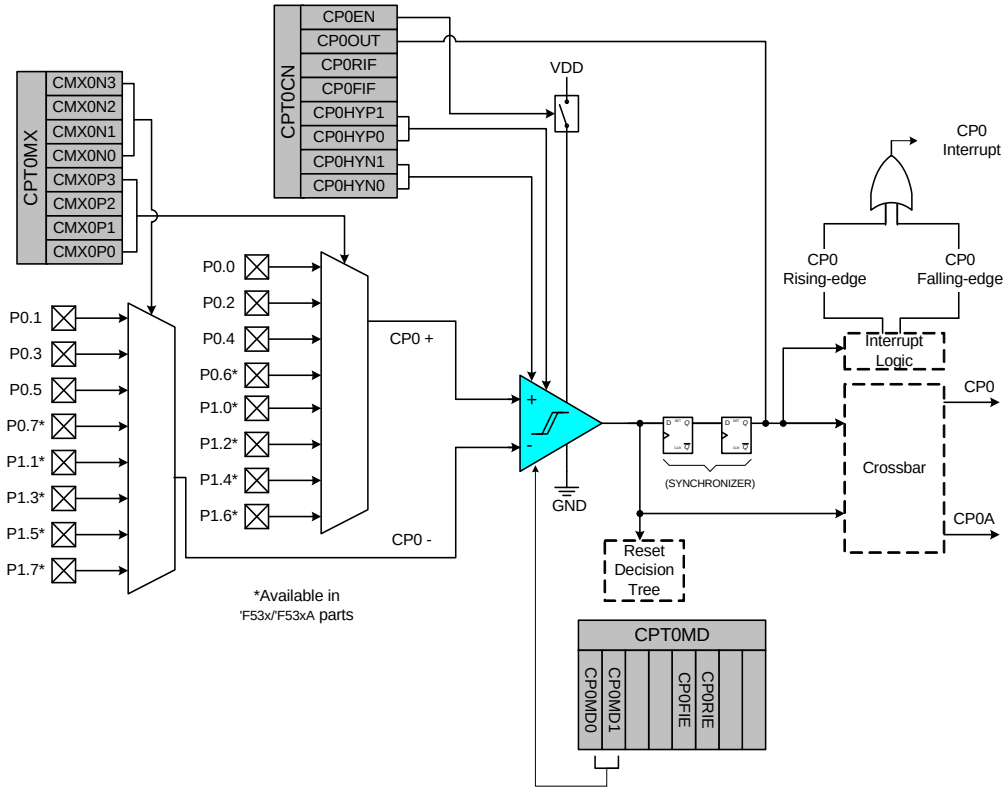


Figure 7.1. Comparator Functional Block Diagram

The Comparator output can be polled in software, used as an interrupt source, internal oscillator suspend awakening source and/or routed to a Port pin. When routed to a Port pin, the Comparator output is available asynchronous or synchronous to the system clock; the asynchronous output is available even in STOP or SUSPEND mode (with no system clock active). When disabled, the Comparator output (if assigned to a Port I/O pin via the Crossbar) defaults to the logic low state, and its supply current falls to

SFR Definition 8.7. PCON: Power Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	STOP	IDLE	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x87

Bits7–2: **RESERVED**.

Bit1: **STOP**: STOP Mode Select.
Writing a 1 to this bit will place the CIP-51 into STOP mode. This bit will always read 0.
1: CIP-51 forced into power-down mode. (Turns off internal oscillator).

Bit0: **IDLE**: IDLE Mode Select.
Writing a 1 to this bit will place the CIP-51 into IDLE mode. This bit will always read 0.
1: CIP-51 forced into IDLE mode. (Shuts off clock to CPU, but clock to Timers, Interrupts, and all peripherals remain active.)

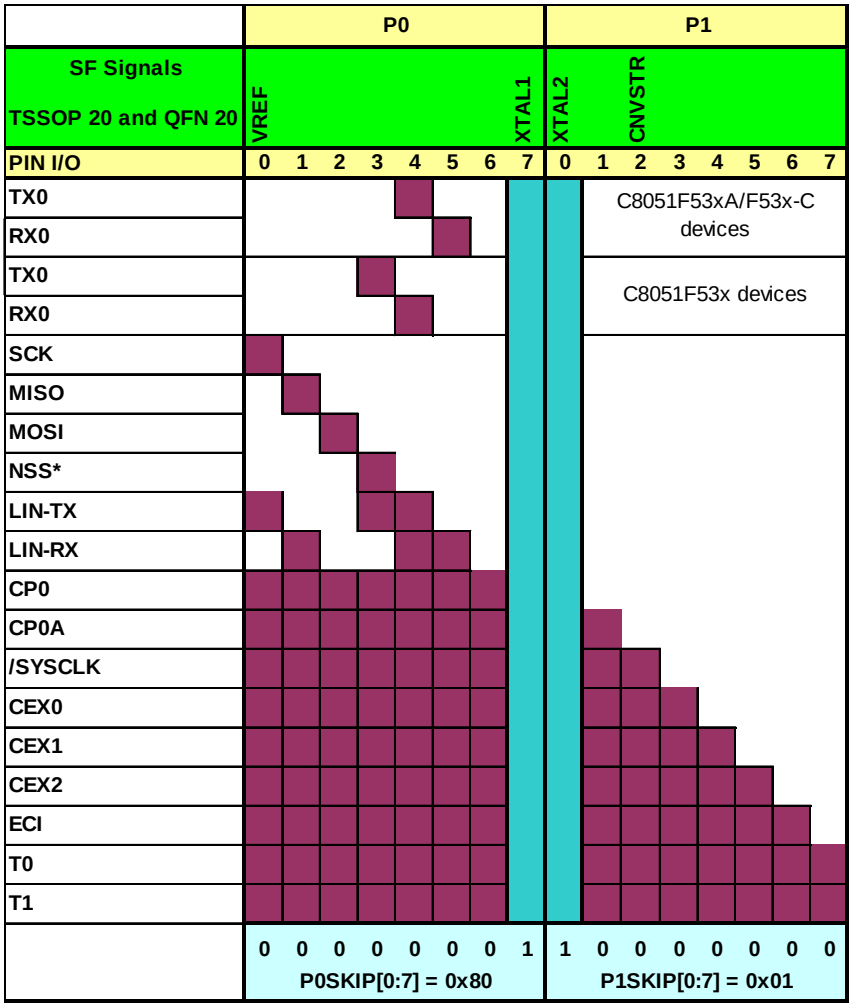
Table 9.2. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Description	Page
OSCICN	0xB2	Internal Oscillator Control	137
OSCXCN	0xB1	External Oscillator Control	142
P0	0x80	Port 0 Latch	129
P0MASK	0xC7	Port 0 Mask	131
P0MAT	0xD7	Port 0 Match	131
P0MDIN	0xF1	Port 0 Input Mode Configuration	129
P0MDOUT	0xA4	Port 0 Output Mode Configuration	130
P0SKIP	0xD4	Port 0 Skip	130
P1	0x90	Port 1 Latch	132
P1MASK	0xBF	Port 1 Mask	134
P1MAT	0xCF	Port 1 Match	134
P1MDIN	0xF2	Port 1 Input Mode Configuration	132
P1MDOUT	0xA5	Port 1 Output Mode Configuration	133
P1SKIP	0xD5	Port 1 Skip	133
PCA0CN	0xD8	PCA Control	206
PCA0CPH0	0xFC	PCA Capture 0 High	209
PCA0CPH1	0xEA	PCA Capture 1 High	209
PCA0CPH2	0xEC	PCA Capture 2 High	209
PCA0CPL0	0xFB	PCA Capture 0 Low	209
PCA0CPL1	0xE9	PCA Capture 1 Low	209
PCA0CPL2	0xEB	PCA Capture 2 Low	209
PCA0CPM0	0xDA	PCA Module 0 Mode	208
PCA0CPM1	0xDB	PCA Module 1 Mode	208
PCA0CPM2	0xDC	PCA Module 2 Mode	208
PCA0H	0xFA	PCA Counter High	209
PCA0L	0xF9	PCA Counter Low	209
PCA0MD	0xD9	PCA Mode	207
PCON	0x87	Power Control	91
PSCTL	0x8F	Program Store R/W Control	119
PSW	0xD0	Program Status Word	88

(F52x/F52xA) for the external CNVSTR signal, and any selected ADC or comparator inputs. The Crossbar skips selected pins as if they were already assigned, and moves to the next unassigned pin. Figure 13.3 shows the Crossbar Decoder priority with no Port pins skipped (P0SKIP, P1SKIP); Figure 13.4 shows the Crossbar Decoder priority with the XTAL1 (P1.0) and XTAL2 (P1.1) pins skipped (P1SKIP = 0x03).

Important Note on UART Pins: On C8051F52xA/F52x-C/F53xA/F53x-C devices, the UART pins must be skipped if the UART is enabled in order for peripherals to appear on port pins beyond the UART on the crossbar. For example, with the SPI and UART enabled on the crossbar with the SPI on P1.0-P1.3, the UART pins must be skipped using P0SKIP for the SPI pins to appear correctly.



Note: 4-Wire SPI Only.

Figure 13.4. Crossbar Priority Decoder with Crystal Pins Skipped (TSSOP 20 and QFN 20)

Note: The load capacitance depends upon the crystal and the manufacturer. Please refer to the crystal data sheet when completing these calculations.

The equation for determining the load capacitance for two capacitors is:

$$C_L = \frac{C_A \times C_B}{C_A + C_B} + C_S$$

Where:
C_A and C_B are the capacitors connected to the crystal leads.
C_S is the total stray capacitance of the PCB.
The stray capacitance for a typical layout where the crystal is as close as possible to the pins is 2–5 pF per pin.

If C_A and C_B are the same (C), then the equation becomes:

$$C_L = \frac{C}{2} + C_S$$

For example, a tuning-fork crystal of 32 kHz with a recommended load capacitance of 12.5 pF should use the configuration shown in Figure 14.1, Option 1. With a stray capacitance of 3 pF per pin (6 pF total), the 13 pF capacitors yield an equivalent capacitance of 12.5 pF across the crystal, as shown in Figure 14.2.

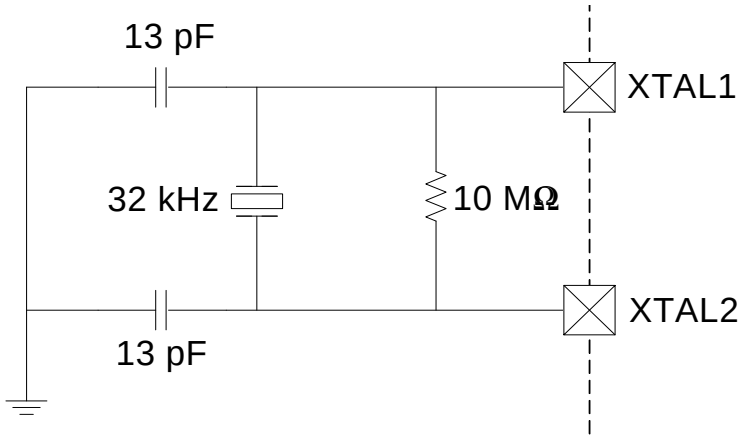


Figure 14.2. 32 kHz External Crystal Example

Important Note on External Crystals: Crystal oscillator circuits are quite sensitive to PCB layout. The crystal should be placed as close as possible to the XTAL pins on the device. The traces should be as short as possible and shielded with ground plane from any other traces which could introduce noise or interference.

16.2. SPI0 Master Mode Operation

A SPI master device initiates all data transfers on a SPI bus. SPI0 is placed in master mode by setting the Master Enable flag (MSTEN, SPI0CN.6). Writing a byte of data to the SPI0 data register (SPI0DAT) when in master mode writes to the transmit buffer. If the SPI shift register is empty, the byte in the transmit buffer is moved to the shift register, and a data transfer begins. The SPI0 master immediately shifts out the data serially on the MOSI line while providing the serial clock on SCK. The SPIF (SPI0CN.7) flag is set to logic 1 at the end of the transfer. If interrupts are enabled, an interrupt request is generated when the SPIF flag is set. While the SPI0 master transfers data to a slave on the MOSI line, the addressed SPI slave device simultaneously transfers data to the SPI master on the MISO line in a full-duplex operation. Therefore, the SPIF flag serves as both a transmit-complete and receive-data-ready flag. The data byte received from the slave is transferred MSB-first into the master's shift register. When a byte is fully shifted into the register, it is moved to the receive buffer where it can be read by the processor by reading SPI0DAT.

When configured as a master, SPI0 can operate in one of three different modes: multi-master mode, 3-wire single-master mode, and 4-wire single-master mode. The default, multi-master mode is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 1. In this mode, NSS is an input to the device, and is used to disable the master SPI0 when another master is accessing the bus. When NSS is pulled low in this mode, MSTEN (SPI0CN.6) and SPIEN (SPI0CN.0) are set to 0 to disable the SPI master device, and a Mode Fault is generated (MODF, SPI0CN.5 = 1). Mode Fault will generate an interrupt if enabled. SPI0 must be manually re-enabled in software under these circumstances. In multi-master systems, devices will typically default to being slave devices while they are not acting as the system master device. In multi-master mode, slave devices can be addressed individually (if needed) using general-purpose I/O pins. Figure 16.2 shows a connection diagram between two master devices in multiple-master mode.

3-wire single-master mode is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 0. In this mode, NSS is not used and is not mapped to an external port pin through the crossbar. Any slave devices that must be addressed in this mode should be selected using general-purpose I/O pins. Figure 16.3 shows a connection diagram between a master device in 3-wire master mode and a slave device.

4-wire single-master mode is active when NSSMD1 (SPI0CN.3) = 1. In this mode, NSS is configured as an output pin and can be used as a slave-select signal for a single SPI device. In this mode, the output value of NSS is controlled (in software) with the bit NSSMD0 (SPI0CN.2). Additional slave devices can be addressed using general-purpose I/O pins. Figure 16.4 shows a connection diagram for a master device in 4-wire master mode and two slave devices.

17. LIN (C8051F520/0A/3/3A/6/6A and C8051F530/0A/3/3A/6/6A)

Important Note: This chapter assumes an understanding of the Local Interconnect Network (LIN) protocol. For more information about the LIN protocol, including specifications, please refer to the LIN consortium (http://www.lin-subbus.org/).

LIN is an asynchronous, serial communications interface used primarily in automotive networks. The Silicon Laboratories LIN controller is compliant to the 2.1 Specification, implements a complete hardware LIN interface, and includes the following features:

- Selectable Master and Slave modes.
- Automatic baud rate option in slave mode
- The internal oscillator is accurate to within 0.5% of 24.5 MHz across the entire temperature range and for VDD voltages greater than or equal to the minimum output of the on-chip voltage regulator, so an external oscillator is not necessary for master mode operation for most systems.

Note: The minimum system clock (SYSCLK) required when using the LIN peripheral is 8 MHz.

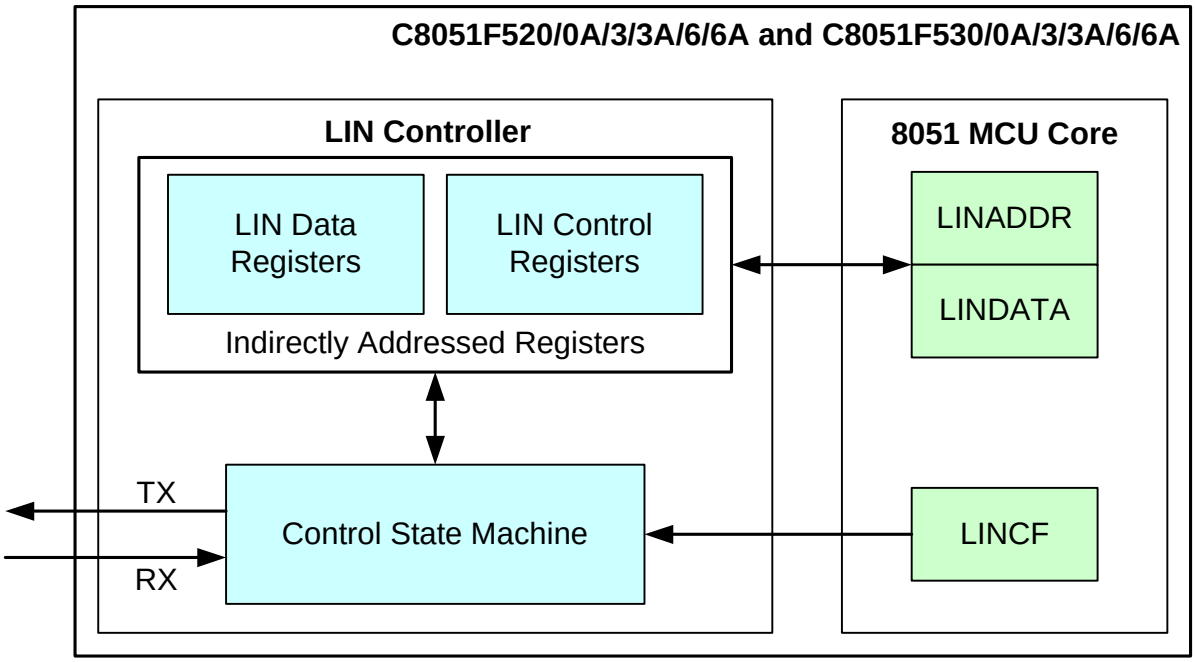


Figure 17.1. LIN Block Diagram

The LIN peripheral has four main components:

1. LIN Access Registers—Provide the interface between the MCU core and the LIN peripheral.
2. LIN Data Registers—Where transmitted and received message data bytes are stored.
3. LIN Control Registers—Control the functionality of the LIN interface.
4. Control State Machine and Bit Streaming Logic—Contains the hardware that serializes messages and controls the bus timing of the controller.

clocked by the system clock. When T0M is cleared, Timer 0 is clocked by the source selected by the Clock Scale bits in CKCON (see SFR Definition 18.3).

Setting the TR0 bit (TCON.4) enables the timer when either GATE0 (TMOD.3) is logic 0 or the input signal INT0 is active as defined by bit IN0PL in register IT01CF (see SFR Definition 10.5. IT01CF: INT0/INT1 Configuration). Setting GATE0 to 1 allows the timer to be controlled by the external input signal INT0 (see Section “10.4. Interrupt Register Descriptions” on page 100), facilitating pulse width measurements.

TR0	GATE0	INT0	Counter/Timer
0	X	X	Disabled
1	0	X	Enabled
1	1	0	Disabled
1	1	1	Enabled
X = Don't Care			

Setting TR0 does not force the timer to reset. The timer registers should be loaded with the desired initial value before the timer is enabled.

TL1 and TH1 form the 13-bit register for Timer 1 in the same manner as described above for TL0 and TH0. Timer 1 is configured and controlled using the relevant TCON and TMOD bits just as with Timer 0. The input signal INT0 is used with Timer 1; the INT0 polarity is defined by bit IN1PL in register IT01CF (see SFR Definition 10.5. IT01CF: INT0/INT1 Configuration).

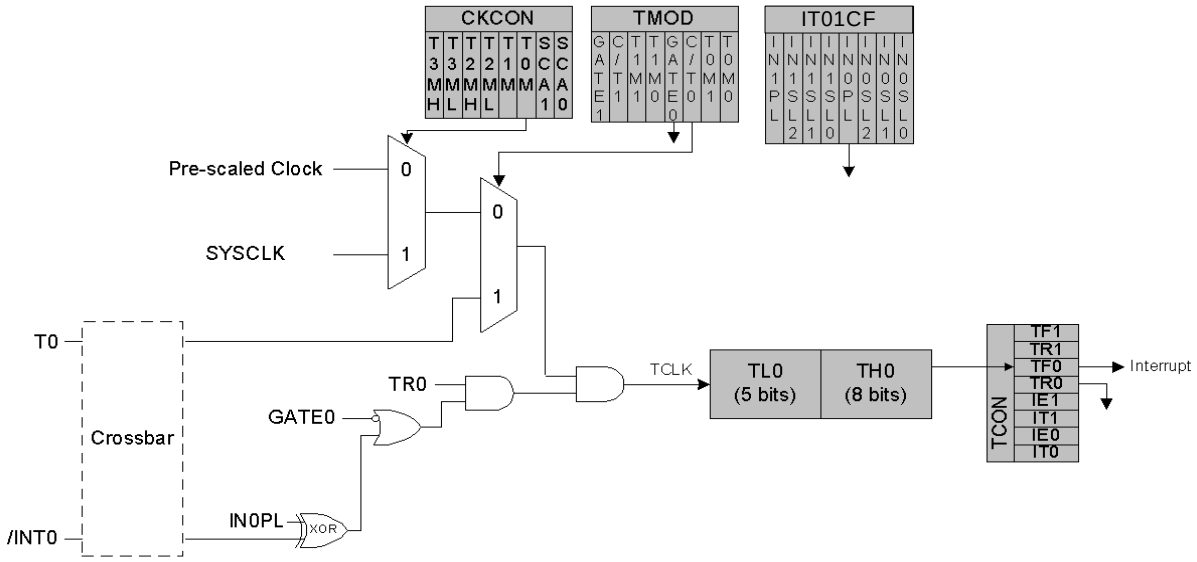


Figure 18.1. T0 Mode 0 Block Diagram

19. Programmable Counter Array (PCA0)

The Programmable Counter Array (PCA0) provides enhanced timer functionality while requiring less CPU intervention than the standard 8051 counter/timers. The PCA consists of a dedicated 16-bit counter/timer and three 16-bit capture/compare modules. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the Crossbar to Port I/O when enabled (See Section “13.1. Priority Crossbar Decoder” on page 122 for details on configuring the Crossbar). The counter/timer is driven by a programmable timebase that can select between six sources: system clock, system clock divided by four, system clock divided by twelve, the external oscillator clock source divided by 8, Timer 0 overflow, or an external clock signal on the ECI input pin. Each capture/compare module may be configured to operate independently in one of three modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, 8-Bit PWM, or 16-Bit PWM (each mode is described in Section “19.2. Capture/Compare Modules” on page 197). The PCA is configured and controlled through the system controller's Special Function Registers. The PCA block diagram is shown in Figure 19.1.

Important Note: The PCA Module 2 may be used as a watchdog timer (WDT), and is enabled in this mode following a system reset. **Access to certain PCA registers is restricted while WDT mode is enabled**. See Section “19.3. Watchdog Timer Mode” on page 203 for details.

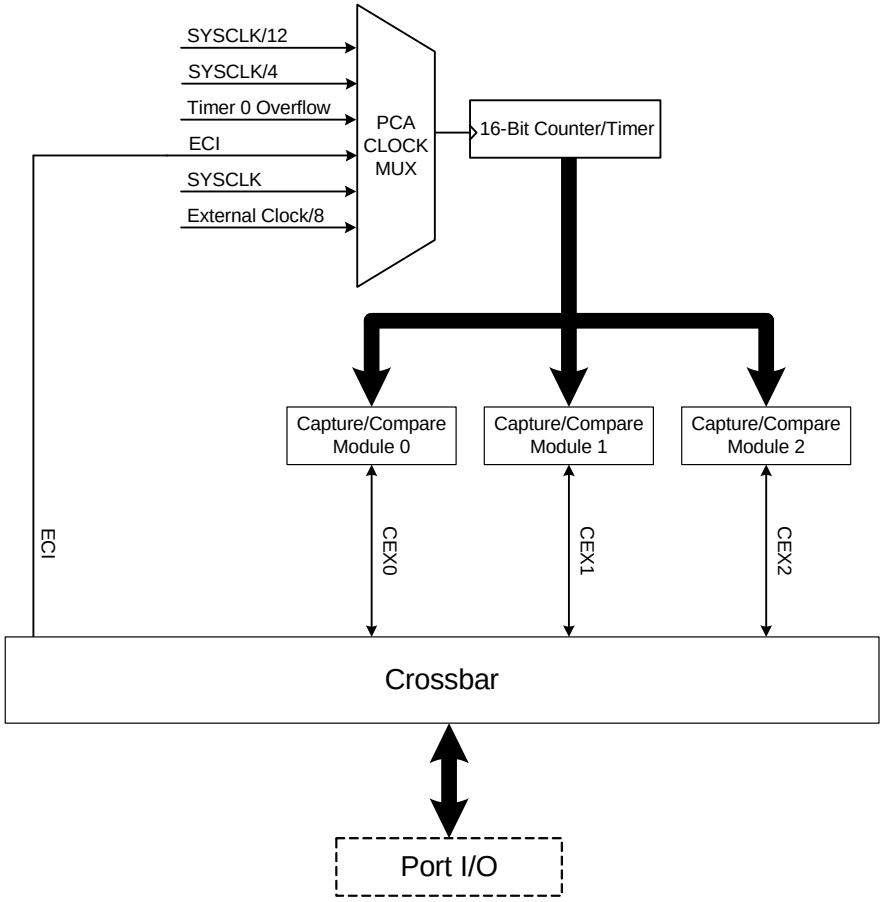


Figure 19.1. PCA Block Diagram

19.1. PCA Counter/Timer

The 16-bit PCA counter/timer consists of two 8-bit SFRs: PCA0L and PCA0H. PCA0H is the high byte (MSB) of the 16-bit counter/timer and PCA0L is the low byte (LSB). Reading PCA0L automatically latches the value of PCA0H into a “snapshot” register; the following PCA0H read accesses this “snapshot” register. **Reading the PCA0L Register first guarantees an accurate reading of the entire 16-bit PCA0 counter.** Reading PCA0H or PCA0L does not disturb the counter operation. The CPS2-CPS0 bits in the PCA0MD register select the timebase for the counter/timer as shown in Table 19.1.

When the counter/timer overflows from 0xFFFF to 0x0000, the Counter Overflow Flag (CF) in PCA0MD is set to logic 1 and an interrupt request is generated if CF interrupts are enabled. Setting the ECF bit in PCA0MD to logic 1 enables the CF flag to generate an interrupt request. The CF bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software (Note: PCA0 interrupts must be globally enabled before CF interrupts are recognized. PCA0 interrupts are globally enabled by setting the EA bit (IE.7) and the EPCA0 bit in EIE1 to logic 1). Clearing the CIDL bit in the PCA0MD register allows the PCA to continue normal operation while the CPU is in Idle mode.

Table 19.1. PCA Timebase Input Options

CPS2	CPS1	CPS0	Timebase
0	0	0	System clock divided by 12
0	0	1	System clock divided by 4
0	1	0	Timer 0 overflow
0	1	1	High-to-low transitions on ECI (max rate = system clock divided by 4)
1	0	0	System clock
1	0	1	External oscillator source divided by 8*

Note: External clock divided by 8 is synchronized with the system clock.

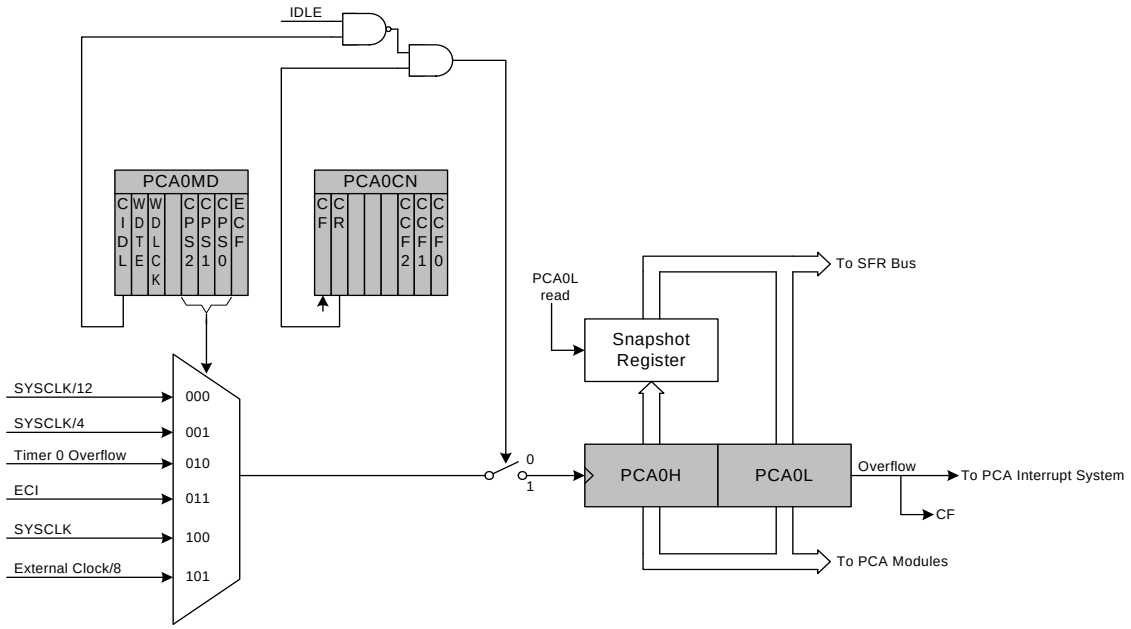


Figure 19.2. PCA Counter/Timer Block Diagram