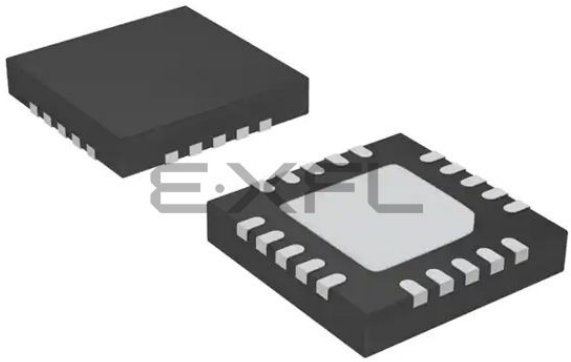

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.25V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f533-c-im

Table 2.7. Comparator Electrical Characteristics

V_{REGIN} = 2.7–5.25 V, –40 to +125 °C unless otherwise noted.
All specifications apply to both Comparator0 and Comparator1 unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
Response Time: Mode 0, Vcm[1] = 1.5 V	CP0+ – CP0– = 100 mV	—	780	—	ns
	CP0+ – CP0– = –100 mV	—	980	—	ns
Response Time: Mode 1, Vcm[1] = 1.5 V	CP0+ – CP0– = 100 mV	—	850	—	ns
	CP0+ – CP0– = –100 mV	—	1120	—	ns
Response Time: Mode 2, Vcm[1] = 1.5 V	CP0+ – CP0– = 100 mV	—	870	—	ns
	CP0+ – CP0– = –100 mV	—	1310	—	ns
Response Time: Mode 3, Vcm[1] = 1.5 V	CP0+ – CP0– = 100 mV	—	1980	—	ns
	CP0+ – CP0– = –100 mV	—	4770	—	ns
Common-Mode Rejection Ratio		—	3	9	mV/V
Positive Hysteresis 1	CP0HYP1-0 = 00	—	0.7	2	mV
Positive Hysteresis 2	CP0HYP1-0 = 01	2	5	10	mV
Positive Hysteresis 3	CP0HYP1-0 = 10	5	10	20	mV
Positive Hysteresis 4	CP0HYP1-0 = 11	13	20	40	mV
Negative Hysteresis 1	CP0HYN1-0 = 00	—	0.7	2	mV
Negative Hysteresis 2	CP0HYN1-0 = 01	2	5	10	mV
Negative Hysteresis 3	CP0HYN1-0 = 10	5	10	20	mV
Negative Hysteresis 4	CP0HYN1-0 = 11	13	20	40	mV
Inverting or Non-Inverting Input Voltage Range[2]		–0.25	—	V_{DD} + 0.25	V
Input Capacitance[2]		—	4	—	pF
Input Bias Current		—	0.5	—	nA
Input Offset Voltage		–15	—	15	mV
Input Impedance		—	1.5	—	kΩ
Power Supply					
Power Supply Rejection[2]		—	0.2	4	mV/V
Power-up Time		—	2.3	—	µs
Supply Current at DC	Mode 0	—	6	30	µA
	Mode 1	—	3	15	µA
	Mode 2	—	2	7.5	µA
	Mode 3	—	0.3	3.8	µA

Notes:
1. Vcm is the common-mode voltage on CP0+ and CP0–.
2. Guaranteed by design and/or characterization.

3. Pinout and Package Definitions

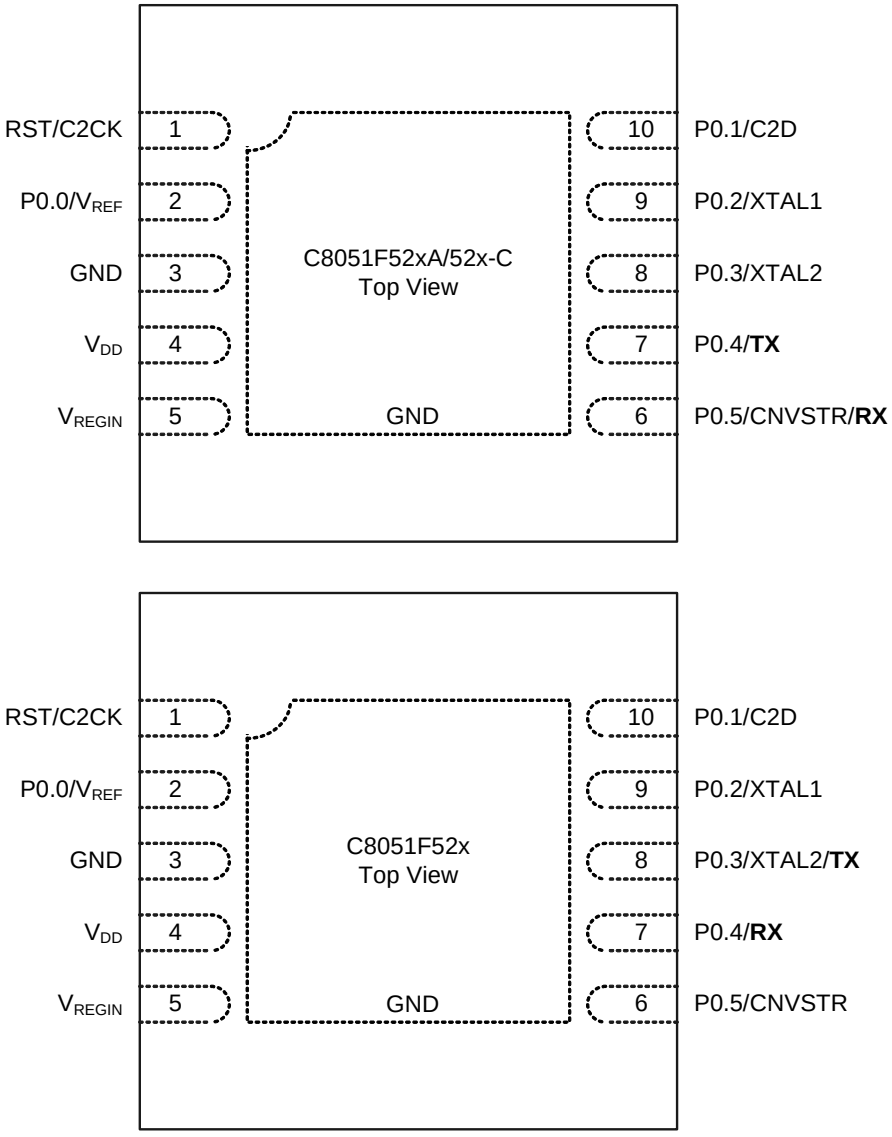


Figure 3.1. DFN-10 Pinout Diagram (Top View)

Table 3.4. Pin Definitions for the C8051F53x and C805153xA (TSSOP 20) (Continued)

Name	Pin Numbers		Type	Description
	'F53xA 'F53x-C	'F53x		
V_{REGIN}	7	7		On-Chip Voltage Regulator Input.
P1.7	8	8	D I/O or A In	Port 1.7. See Port I/O Section for a complete description.
P1.6	9	9	D I/O or A In	Port 1.6. See Port I/O Section for a complete description.
P1.5	10	10	D I/O or A In	Port 1.5. See Port I/O Section for a complete description.
P1.4	11	11	D I/O or A In	Port 1.4. See Port I/O Section for a complete description.
P1.3	12	12	D I/O or A In	Port 1.3. See Port I/O Section for a complete description.
P1.2/ CNVSTR	13	13	D I/O or A In D In	Port 1.2. See Port I/O Section for a complete description. External Converter start input for the ADC0, see Section "4. 12-Bit ADC (ADC0)" on page 52 for a complete description.
P1.1	14	14	D I/O or A In	Port 1.1. See Port I/O Section for a complete description.
P1.0/ XTAL2	15	15	D I/O or A In D I/O	Port 1.0. See Port I/O Section for a complete description. External Clock Output. For an external crystal or resonator, this pin is the excitation driver. This pin is the external clock input for CMOS, capacitor, or RC oscillator configurations. See Section "14. Oscillators" on page 135.
P0.7/ XTAL1	16	16	D I/O or A In A In	Port 0.7. See Port I/O Section for a complete description. External Clock Input. This pin is the external oscillator return for a crystal or resonator. Section "14. Oscillators" on page 135.
P0.6/ C2D	17	17	D I/O or A In D I/O	Port 0.6. See Port I/O Section for a complete description. Bi-directional data signal for the C2 Debug Interface.
P0.5/RX*	18	—	D I/O or A In	Port 0.5. See Port I/O Section for a complete description.
P0.5	—	18	D I/O or A In	Port 0.5. See Port I/O Section for a complete description.
***Note:** Please refer to Section "20. Device Specific Behavior" on page 210.				

Table 3.7. Pin Definitions for the C8051F53x and C805153xA (QFN 20) (Continued)

Name	Pin Numbers		Type	Description
	'F53xA 'F53x-C	'F53x		
P1.0/	13	13	D I/O or A In	Port 1.0. See Port I/O Section for a complete description.
XTAL2			D I/O	External Clock Output. For an external crystal or resonator, this pin is the excitation driver. This pin is the external clock input for CMOS, capacitor, or RC oscillator configurations. Section "14. Oscillators" on page 135.
P0.7/	14	14	D I/O or	Port 0.7. See Port I/O Section for a complete description.
XTAL1			A In	External Clock Input. This pin is the external oscillator return for a crystal or resonator. See Oscillator Section.
P0.6/	15	15	D I/O or A In	Port 0.6. See Port I/O Section for a complete description.
C2D			D I/O	Bi-directional data signal for the C2 Debug Interface.
P0.5/RX*	16	—	D I/O or A In	Port 0.5. See Port I/O Section for a complete description.
P0.5	—	16	D I/O or A In	Port 0.5. See Port I/O Section for a complete description.
P0.4/TX*	17	—	D I/O or A In	Port 0.4. See Port I/O Section for a complete description.
P0.4/RX*	—	17	D I/O or A In	Port 0.4. See Port I/O Section for a complete description.
P0.3	18	—	D I/O or A In	Port 0.3. See Port I/O Section for a complete description.
P0.3/TX*	—	18	D I/O or A In	Port 0.3. See Port I/O Section for a complete description.
P0.2	19	19	D I/O or A In	Port 0.2. See Port I/O Section for a complete description.
P0.1	20	20	D I/O or A In	Port 0.1. See Port I/O Section for a complete description.
Note: Please refer to Section "20. Device Specific Behavior" on page 210.				

SFR Definition 7.3. CPT0MD: Comparator0 Mode Selection

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
Reserved	—	CP0RIE	CP0FIE	—	—	CP0MD1	CP0MD0	00000010
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x9D

Bit7: **RESERVED**. Read = 0b. Must write 0b.
Bit6: **UNUSED**. Read = 0b. Write = don't care.
Bit5: **CP0RIE**: Comparator Rising-Edge Interrupt Enable.
0: Comparator rising-edge interrupt disabled.
1: Comparator rising-edge interrupt enabled.
Bit4: **CP0FIE**: Comparator Falling-Edge Interrupt Enable.
0: Comparator falling-edge interrupt disabled.
1: Comparator falling-edge interrupt enabled.
Note: It is necessary to enable both CP0xIE and the correspondent ECPx bit located in EIE1 SFR.
Bits3–2: **UNUSED**. Read = 00b. Write = don't care.
Bits1–0: **CP0MD1–CP0MD0**: Comparator0 Mode Select
These bits select the response time for Comparator0.

Mode	CP0MD1	CP0MD0	CP0 Falling Edge Response Time (TYP)
0	0	0	Fastest Response Time
1	0	1	—
2	1	0	—
3	1	1	Lowest Power Consumption

Note: Rising Edge response times are approximately double the Falling Edge response times.

Performance

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute, and usually have a maximum system clock of 12 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with no instructions taking more than eight system clock cycles.

With the CIP-51's system clock running at 25 MHz, it has a peak throughput of 25 MIPS. The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
Number of Instructions	26	50	5	14	7	3	1	2	1

Programming and Debugging Support

In-system programming of the Flash program memory and communication with on-chip debug support logic is accomplished via the Silicon Labs 2-Wire (C2) interface. Note that the re-programmable Flash can also be read and written a single byte at a time by the application software using the MOVC and MOVX instructions. This feature allows program memory to be used for non-volatile data storage as well as updating program code under software control.

The on-chip debug support logic facilitates full speed in-circuit debugging, allowing the setting of hardware breakpoints, starting, stopping and single stepping through program execution (including interrupt service routines), examination of the program's call stack, and reading/writing the contents of registers and memory. This method of on-chip debugging is completely non-intrusive, requiring no RAM, Stack, timers, or other on-chip resources.

The CIP-51 is supported by development tools from Silicon Laboratories, Inc. and third party vendors. Silicon Laboratories provides an integrated development environment (IDE) including editor, evaluation compiler, assembler, debugger and programmer. The IDE's debugger and programmer interface to the CIP-51 via the on-chip debug logic to provide fast and efficient in-system device programming and debugging. Third party macro assemblers and C compilers are also available.

8.1. Instruction Set

The instruction set of the CIP-51 System Controller is fully compatible with the standard MCS-51™ instruction set. Standard 8051 development tools can be used to develop software for the CIP-51. All CIP-51 instructions are the binary and functional equivalent of their MCS-51™ counterparts, including opcodes, addressing modes and effect on PSW flags. However, instruction timing is different than that of the standard 8051.

8.1.1. Instruction and CPU Timing

In many 8051 implementations, a distinction is made between machine cycles and clock cycles, with machine cycles varying from 2 to 12 clock cycles in length. However, the CIP-51 implementation is based solely on clock cycle timing. All instruction timings are specified in terms of clock cycles.

Due to the pipelined architecture of the CIP-51, most instructions execute in the same number of clock cycles as there are program bytes in the instruction. Conditional branch instructions take one less clock cycle to complete when the branch is not taken as opposed to when the branch is taken. Table 8.1 is the CIP-51 Instruction Set Summary, which includes the mnemonic, number of bytes, and number of clock cycles for each instruction.

11.1. Power-On Reset

During power-up, the device is held in a reset state and the $\overline{RST}$ pin is driven low until V_{DD} settles above V_{RST}. V_{DD} ramp time is defined as how fast V_{DD} ramps from 0 V to V_{RST}. An additional delay ($T_{PORDelay}$) occurs before the device is released from reset. The V_{RST} threshold and $T_{PORDelay}$ are specified in Table 2.8, “Reset Electrical Characteristics,” on page 32. Figure 11.2 plots the power-on and V_{DD} monitor reset timing.

Note: Please refer to Section “20.4. VDD Monitors and VDD Ramp Time” on page 211 for definition of V_{RST} and V_{DD} ramp time in older silicon revisions A and B.

On exit from a power-on reset, the PORSF flag (RSTSRC.1) is set by hardware to logic 1. When PORSF is set, all of the other reset flags in the RSTSRC Register are indeterminate (PORSF is cleared by all other resets). Since all resets cause program execution to begin at the same location (0x0000), software can read the PORSF flag to determine if a power-up was the cause of reset. The contents of internal data memory should be assumed to be undefined after a power-on reset. Both the V_{DD} monitors (VDDMON0 and VDDMON1) are enabled following a power-on reset.

Note: Please refer to Section “11.2.1. VDD Monitor Thresholds and Minimum VDD” on page 108 for recommendations related to minimum V_{DD}.

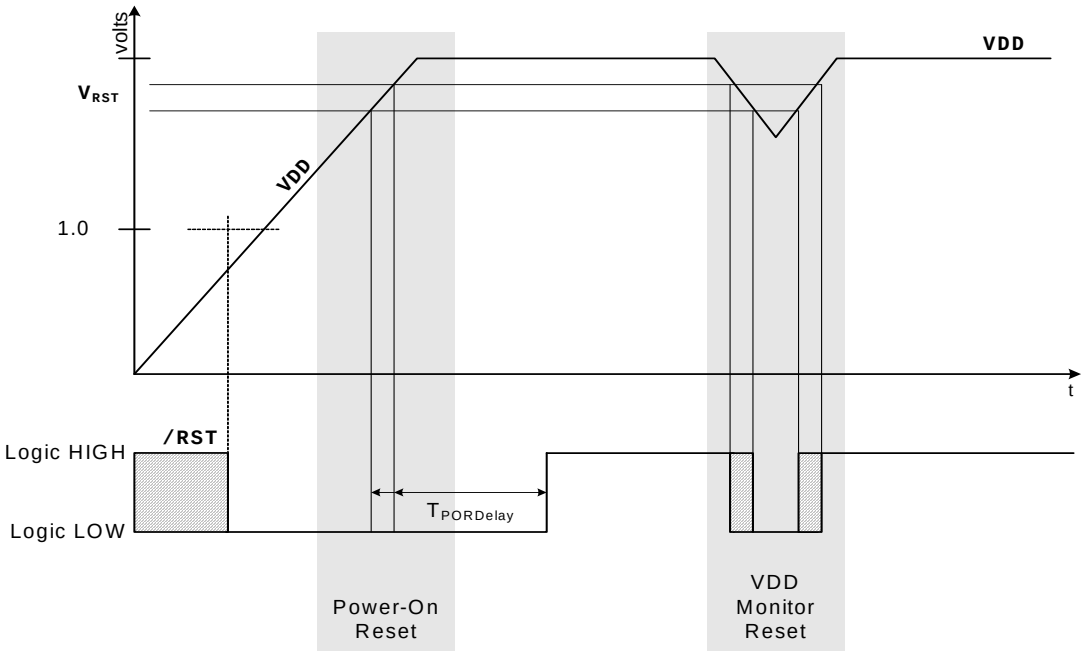


Figure 11.2. Power-On and V_{DD} Monitor Reset Timing

SFR Definition 11.2. RSTSRC: Reset Source

R/W	R	R/W	R/W	R	R/W	R/W	R	Reset Value
—	FERROR	C0RSEF	SWRSF	WDTRSF	MCDRSF	PORSF	PINRSF	Variable
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
							SFR Address:	0xEF

Note: Software should avoid read modify write instructions when writing values to RSTSRC.

Bit7: **UNUSED**. Read = 1, Write = don't care.
Bit6: **FERROR**: Flash Error Indicator.
0: Source of last reset was not a Flash read/write/erase error.
1: Source of last reset was a Flash read/write/erase error.
Bit5: **C0RSEF**: Comparator0 Reset Enable and Flag.
0: **Read:** Source of last reset was not Comparator0.
Write: Comparator0 is not a reset source.
1: **Read:** Source of last reset was Comparator0.
Write: Comparator0 is a reset source (active-low).
Bit4: **SWRSF**: Software Reset Force and Flag.
0: **Read:** Source of last reset was not a write to the SWRSF bit.
Write: No Effect.
1: **Read:** Source of last reset was a write to the SWRSF bit.
Write: Forces a system reset.
Bit3: **WDTRSF**: Watchdog Timer Reset Flag.
0: Source of last reset was not a WDT timeout.
1: Source of last reset was a WDT timeout.
Bit2: **MCDRSF**: Missing Clock Detector Flag.
0: **Read:** Source of last reset was not a Missing Clock Detector timeout.
Write: Missing Clock Detector disabled.
1: **Read:** Source of last reset was a Missing Clock Detector timeout.
Write: Missing Clock Detector enabled; triggers a reset if a missing clock condition is detected.
Bit1: **PORSF**: Power-On Reset Force and Flag.
This bit is set anytime a power-on reset occurs. Writing this bit enables/disables the V_{DD} monitor (VDDMON0) as a reset source. **Note: writing 1 to this bit before the V_{DD} monitor is enabled and stabilized may cause a system reset.** See register VDDMON (SFR Definition 11.1)
0: **Read:** Last reset was not a power-on or V_{DD} monitor reset.
Write: V_{DD} monitor (VDDMON0) is not a reset source.
1: **Read:** Last reset was a power-on or V_{DD} monitor reset; all other reset flags indeterminate.
Write: V_{DD} monitor (VDDMON0) is a reset source.
Bit0: **PINRSF**: HW Pin Reset Flag.
0: Source of last reset was not $\overline{\text{RST}}$ pin.
1: Source of last reset was $\overline{\text{RST}}$ pin.

12.2. Flash Write and Erase Guidelines

Any system which contains routines which write or erase Flash memory from software involves some risk that the write or erase routines will execute unintentionally if the CPU is operating outside its specified operating range of V_{DD}, system clock frequency, or temperature. This accidental execution of Flash modifying code can result in alteration of Flash memory contents causing a system failure that is only recoverable by re-Flashing the code in the device.

The following guidelines are recommended for any system which contains routines which write or erase Flash from code.

12.2.1. V_{DD} Maintenance and the V_{DD} monitor

1. If the system power supply is subject to voltage or current "spikes," add sufficient transient protection devices to the power supply to ensure that the supply voltages listed in the Absolute Maximum Ratings table are not exceeded.
2. Make certain that the maximum V_{DD} ramp time specification (if applicable) is met. See Section 20.4 on page 211 for more details on V_{DD} ramp time. If the system cannot meet this ramp time specification, then add an external V_{DD} brownout circuit to the $\overline{RST}$ pin of the device that holds the device in reset until V_{DD} reaches the minimum specified V_{DD} and re-asserts $\overline{RST}$ if V_{DD} drops belowthat level. V_{DD} (min) is specified in Table 2.2 on page 26.
3. Enable the on-chip V_{DD} monitor (VDDMON0) and enable it as a reset source as early in code as possible. This should be the first set of instructions executed after the Reset Vector. For C-based systems, this will involve modifying the startup code added by the C compiler. See your compiler documentation for more details. Make certain that there are no delays in software between enabling the V_{DD} monitor (VDDMON0) and enabling it as a reset source. Code examples showing this can be found in “AN201: Writing to Flash from Firmware", available from the Silicon Laboratories web site.
4. As an added precaution, explicitly enable the V_{DD} monitor (VDDMON0) and enable the V_{DD} monitor as a reset source inside the functions that write and erase Flash memory. The V_{DD} monitor enable instructions should be placed just after the instruction to set PSWE to a 1, but before the Flash write or erase operation instruction.
5. Make certain that all writes to the RSTSRC (Reset Sources) register use direct assignment operators and explicitly DO NOT use the bit-wise operators (such as AND or OR). For example, "RSTSRC = 0x02" is correct. "RSTSRC |= 0x02" is incorrect.
6. Make certain that all writes to the RSTSRC register explicitly set the PORSF bit to a 1. Areas to check are initialization code which enables other reset sources, such as the Missing Clock Detector or Comparator, for example, and instructions which force a Software Reset. A global search on "RSTSRC" can quickly verify this.

12.2.2. PSWE Maintenance

1. Reduce the number of places in code where the PSWE bit (PSCTL.0) is set to a 1. There should be exactly one routine in code that sets PSWE to a 1 to write Flash bytes and one routine in code that sets PSWE and PSEE both to a 1 to erase Flash pages.
2. Minimize the number of variable accesses while PSWE is set to a 1. Handle pointer address updates and loop variable maintenance outside the "PSWE = 1;... PSWE = 0;" area. Code examples showing this can be found in “AN201: Writing to Flash from Firmware,” available from the Silicon Laboratories web site.
3. Disable interrupts prior to setting PSWE to a 1 and leave them disabled until after PSWE has been reset to '0'. Any interrupts posted during the Flash write or erase operation will be serviced in priority order after the Flash operation has been completed and interrupts have been re-enabled by software.
4. Make certain that the Flash write and erase pointer variables are not located in XRAM. See your compiler documentation for instructions regarding how to explicitly locate variables in different memory areas.

SFR Definition 12.1. PSCTL: Program Store R/W Control

R	R	R	R	R	R	R/W	R/W	Reset Value
—	—	—	—	—	—	PSEE	PSWE	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x8F

Bits7–2: **UNUSED**: Read = 000000b, Write = don't care.

Bit1: **PSEE**: Program Store Erase Enable
Setting this bit (in combination with PSWE) allows an entire page of Flash program memory to be erased. If this bit is logic 1 and Flash writes are enabled (PSWE is logic 1), a write to Flash memory using the MOVX instruction will erase the entire page that contains the location addressed by the MOVX instruction. The value of the data byte written does not matter.
0: Flash program memory erasure disabled.
1: Flash program memory erasure enabled.

Bit0: **PSWE**: Program Store Write Enable
Setting this bit allows writing a byte of data to the Flash program memory using the MOVX write instruction. The Flash location should be erased before writing data.
0: Writes to Flash program memory disabled.
1: Writes to Flash program memory enabled; the MOVX write instruction targets Flash memory.

Note: See Section "12.1. Programming The Flash Memory" on page 113 for minimum V_{DD} and temperature requirements for flash erase and write operations.

SFR Definition 12.2. FLKEY: Flash Lock and Key

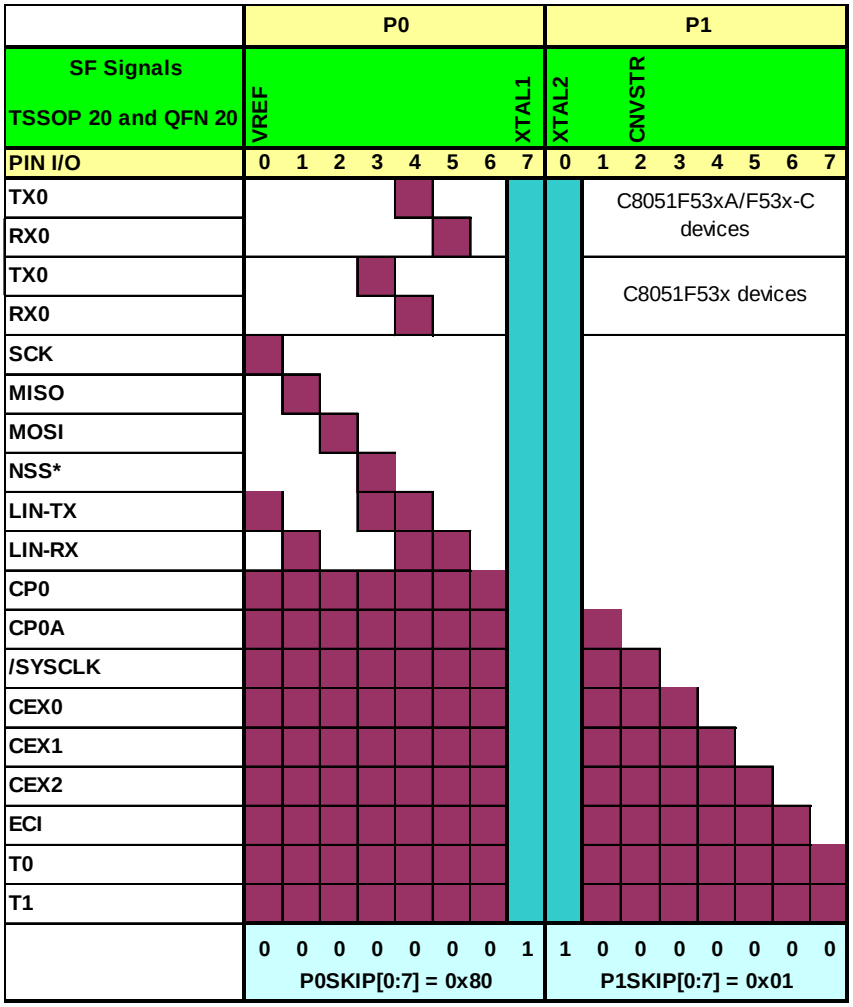
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xB7

Bits7–0: **FLKEY**: Flash Lock and Key Register
Write:
This register provides a lock and key function for Flash erasures and writes. Flash writes and erases are enabled by writing 0xA5 followed by 0xF1 to the FLKEY register. Flash writes and erases are automatically disabled after the next write or erase is complete. If any writes to FLKEY are performed incorrectly, or if a Flash write or erase operation is attempted while these operations are disabled, the Flash will be permanently locked from writes or erasures until the next device reset. If an application never writes to Flash, it can intentionally lock the Flash by writing a non-0xA5 value to FLKEY from software.
Read:
When read, bits 1–0 indicate the current Flash lock state.
00: Flash is write/erase locked.
01: The first key code has been written (0xA5).
10: Flash is unlocked (writes/erases allowed).
11: Flash writes/erases disabled until the next reset.

(F52x/F52xA) for the external CNVSTR signal, and any selected ADC or comparator inputs. The Crossbar skips selected pins as if they were already assigned, and moves to the next unassigned pin. Figure 13.3 shows the Crossbar Decoder priority with no Port pins skipped (P0SKIP, P1SKIP); Figure 13.4 shows the Crossbar Decoder priority with the XTAL1 (P1.0) and XTAL2 (P1.1) pins skipped (P1SKIP = 0x03).

Important Note on UART Pins: On C8051F52xA/F52x-C/F53xA/F53x-C devices, the UART pins must be skipped if the UART is enabled in order for peripherals to appear on port pins beyond the UART on the crossbar. For example, with the SPI and UART enabled on the crossbar with the SPI on P1.0-P1.3, the UART pins must be skipped using P0SKIP for the SPI pins to appear correctly.



Note: 4-Wire SPI Only.

Figure 13.4. Crossbar Priority Decoder with Crystal Pins Skipped (TSSOP 20 and QFN 20)

17.1. Software Interface with the LIN Peripheral

The selection of the mode (Master or Slave) and the automatic baud rate feature are done though the LIN0 Control Mode (LIN0CF) register. The other LIN registers are accessed indirectly through the two SFRs LIN0 Address (LINADDR) and LIN0 Data (LINDATA). The LINADDR register selects which LIN register is targeted by reads/writes of the LINDATA register. The full list of indirectly-accessible LIN register is given in Table 17.4 on page 174.

17.2. LIN Interface Setup and Operation

The hardware based LIN peripheral allows for the implementation of both Master and Slave nodes with minimal firmware overhead and complete control of the interface status while allowing for interrupt and polled mode operation.

The first step to use the peripheral is to define the basic characteristics of the node:

- Mode—Master or Slave
- Baud Rate—Either defined manually or using the autobaud feature (slave mode only).
- Checksum Type—Select between classic or enhanced checksum, both of which are implemented in hardware.

17.2.1. Mode Definition

Following the LIN specification, the peripheral implements both the Slave and Master operating modes in hardware. The mode is configured using the MODE bit (LIN0CF.6).

17.2.2. Baud Rate Options: Manual or Autobaud

The LIN peripheral can be selected to have its baud rate calculated manually or automatically. A master node must always have its baud rate set manually, but slave nodes can choose between a manual or automatic setup. The configuration is selected using the ABAUD bit (LIN0CF.5).

Both the manual and automatic baud rate configurations require additional setup. The following sections explain the different options available and their relation with the baud rate, along with the steps necessary to achieve the required baud rate.

17.2.3. Baud Rate Calculations—Manual Mode

The baud rate used by the peripheral is a function of the System Clock (SYSCLK) and the bit-timing Registers according to the following equation:

$$baud\_rate = \frac{SYSCLK}{2^{(\text{prescaler} + 1)} \times divider \times (multiplier + 1)}$$

The prescaler, divider and multiplier factors are part of the LIN0DIV and LIN0MUL registers and can assume values in the following range:

SFR Definition 17.3. LINCF Control Mode Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
LINEN	MODE	ABAUD						00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x95

Bit7: **LINEN**: LIN Interface Enable bit
0: LIN0 is disabled.
1: LIN0 is enabled.

Bit6: **MODE**: LIN Mode Selection
0: LIN0 operates in Slave mode.
1: LIN0 operates in Master mode.

Bit5: **ABAUD**: LIN Mode Automatic Baud Rate Selection (**slave mode only**).
0: Manual baud rate selection is enabled.
1: Automatic baud rate selection is enabled.

SFR Definition 17.8. LIN0DT5: LIN0 Data Byte 5

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Address: 0x04 (indirect)

Bit7–0: **LIN0DT5**: LIN Data Byte 5.
Serial Data Byte 5 that is received or transmitted across the LIN interface.

SFR Definition 17.9. LIN0DT6: LIN0 Data Byte 6

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Address: 0x05 (indirect)

Bit7–0: **LIN0DT6**: LIN Data Byte 6.
Serial Data Byte 6 that is received or transmitted across the LIN interface.

SFR Definition 17.10. LIN0DT7: LIN0 Data Byte 7

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Address: 0x06 (indirect)

Bit7–0: **LIN0DT7**: LIN Data Byte 7.
Serial Data Byte 7 that is received or transmitted across the LIN interface.

SFR Definition 17.11. LIN0DT8: LIN0 Data Byte 8

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Address: 0x07 (indirect)

Bit7–0: **LIN0DT8**: LIN Data Byte 8.
Serial Data Byte 8 that is received or transmitted across the LIN interface.

SFR Definition 17.13. LIN0ST: LIN0 STATUS Register

R	R	R	R	R/W	R	R	R	Reset Value
ACTIVE	IDLTOUT	ABORT	DTREQ	LININT	ERROR	WAKEUP	DONE	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Address: 0x09 (indirect)

Bit7: **ACTIVE**: LIN Bus Activity Bit.
0: No transmission activity detected on the LIN bus.
1: Transmission activity detected on the LIN bus.

Bit6: **IDLTOUT**: Bus Idle Timeout Bit (**slave mode only**).
0: The bus has not been idle for four seconds.
1: No bus activity has been detected for four seconds, but the bus is not yet in Sleep mode.

Bit5: **ABORT**: Aborted transmission signal (**slave mode only**).
0: The current transmission has not been interrupted or stopped. This bit is reset to 0 after receiving a SYNCH BREAK that does not interrupt a pending transmission.
1: New SYNCH BREAK detected before the end of the last transmission or the STOP bit (LIN0CTRL.7) has been set.

Bit4: **DTREQ**: Data Request bit (**slave mode only**).
0: Data identifier has not been received.
1: Data identifier has been received.

Bit3: **LININT**: Interrupt Request bit.
0: An interrupt is not pending. This bit is cleared by setting RSTINT (LIN0CTRL.3)
1: There is a pending LIN0 interrupt.

Bit2: **ERROR**: Communication Error Bit.
0: No error has been detected. This bit is cleared by setting RSTERR (LIN0CTRL.2)
1: An error has been detected.

Bit1: **WAKEUP**: Wakeup Bit.
0: A wakeup signal is not being transmitted and has not been received.
1: A wakeup signal is being transmitted or has been received.

Bit0: **DONE**: Transmission Complete Bit.
0: A transmission is not in progress or has not been started. This bit is cleared at the start of a transmission.
1: The current transmission is complete.

19.2.2. Software Timer (Compare) Mode

In Software Timer mode, the PCA counter/timer value is compared to the module's 16-bit capture/compare register (PCA0CPHn and PCA0CPLn). When a match occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1 and an interrupt request is generated if CCF interrupts are enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Setting the ECOMn and MATn bits in the PCA0CPMn register enables Software Timer mode.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

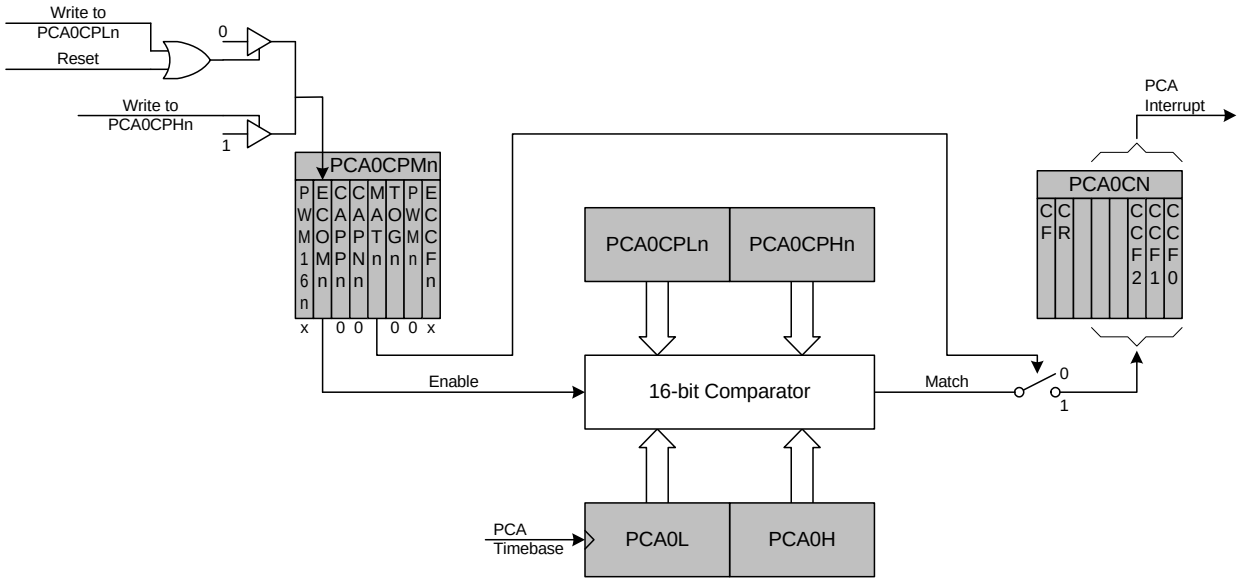


Figure 19.5. PCA Software Timer Mode Diagram

19.2.6. 16-Bit Pulse Width Modulator Mode

A PCA module may also be operated in 16-Bit PWM mode. In this mode, the 16-bit capture/compare module defines the number of PCA clocks for the low time of the PWM signal. When the PCA counter matches the module contents, the output on CEXn is asserted high; when the counter overflows, CEXn is asserted low. To output a varying duty cycle, new value writes should be synchronized with PCA CCFn match interrupts. 16-Bit PWM Mode is enabled by setting the ECOMn, PWMn, and PWM16n bits in the PCA0CPMn register. For a varying duty cycle, match interrupts should be enabled (ECCFn = 1 AND MATn = 1) to help synchronize the capture/compare register writes. The duty cycle for 16-Bit PWM Mode is given by Equation 19.3.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

$$DutyCycle = \frac{(65536 - PCA0CPn)}{65536}$$

Equation 19.3. 16-Bit PWM Duty Cycle

Using Equation 19.3, the largest duty cycle is 100% (PCA0CPn = 0), and the smallest duty cycle is 0.0015% (PCA0CPn = 0xFFFF). A 0% duty cycle may be generated by clearing the ECOMn bit to 0.

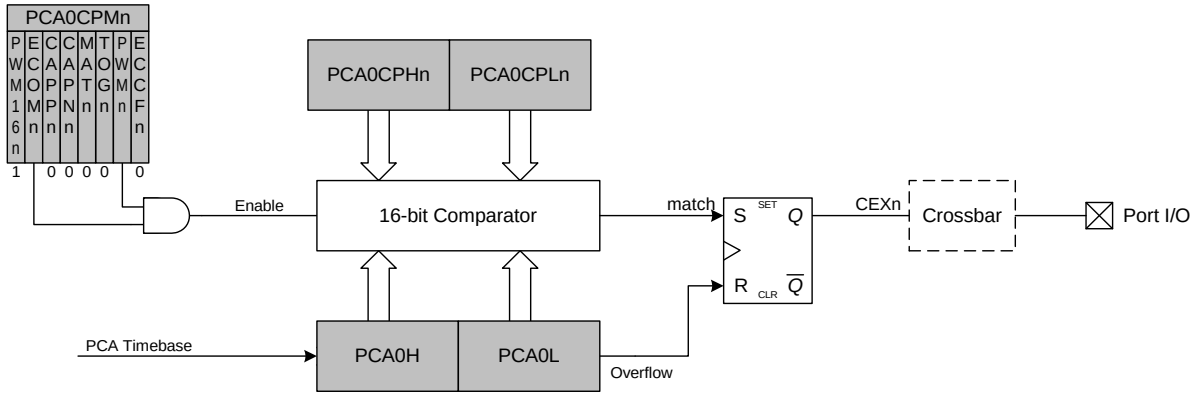


Figure 19.9. PCA 16-Bit PWM Mode

19.3. Watchdog Timer Mode

A programmable watchdog timer (WDT) function is available through the PCA Module 2. The WDT is used to generate a reset if the time between writes to the WDT update register (PCA0CPH2) exceed a specified limit. The WDT can be configured and enabled/disabled as needed by software.

With the WDTE bit set in the PCA0MD register, Module 2 operates as a watchdog timer (WDT). The Module 2 high byte is compared to the PCA counter high byte; the Module 2 low byte holds the offset to be used when WDT updates are performed. **The Watchdog Timer is enabled on reset. Writes to some PCA registers are restricted while the Watchdog Timer is enabled.**

SFR Definition 19.4. PCA0L: PCA Counter/Timer Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xF9

Bits7–0: **PCA0L**: PCA Counter/Timer Low Byte.
The PCA0L register holds the low byte (LSB) of the 16-bit PCA Counter/Timer.

SFR Definition 19.5. PCA0H: PCA Counter/Timer High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:

SFR Address: 0xFA

Bits7–0: **PCA0H**: PCA Counter/Timer High Byte.
The PCA0H register holds the high byte (MSB) of the 16-bit PCA Counter/Timer.

SFR Definition 19.6. PCA0CPLn: PCA Capture Module Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: PCA0CPL0: 0xFB, PCA0CPL1: 0xE9, PCA0CPL2: 0xEB

Bits7–0: **PCA0CPLn**: PCA Capture Module Low Byte.
The PCA0CPLn register holds the low byte (LSB) of the 16-bit capture module n.

SFR Definition 19.7. PCA0CPHn: PCA Capture Module High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: PCA0CPH0: 0xFC, PCA0CPH1: 0xE9, PCA0CPH2: 0xEC

Bits7–0: **PCA0CPHn**: PCA Capture Module High Byte.
The PCA0CPHn register holds the high byte (MSB) of the 16-bit capture module n.

Revision 1.2 to 1.3

- Updated “System Overview” on page 13 with a voltage range specification for the internal oscillator.
- Updated Table 2.11 on page 34 with new conditions for the internal oscillator accuracy. The internal oscillator accuracy is dependent on the operating voltage range.
- Updated Section 2 to remove the internal oscillator curve across temperature diagram.
- Updated Figure “4.5 12-Bit ADC Burst Mode Example with Repeat Count Set to 4” on page 58 with new timing diagram when using CNVSTR pin.
- Updated SFR Definition 5.1 (REF0CN) with oscillator suspend requirement for ZTCEN.
- Updated SFR Definition 6.1 (REG0CN) with a new definition for Bit 6. The bit 6 reset value is 1b and must be written to 1b.
- Updated Section “8.3.3. Suspend Mode” on page 90 with note regarding ZTCEN.
- Updated Section “17. LIN (C8051F520/0A/3/3A/6/6A and C8051F530/0A/3/3A/6/6A)” on page 164 with a voltage range specification for the internal oscillator.

Revision 1.3 to 1.4

- Added ‘AEC-Q100’ qualification information on page 1.
- Changed page headers throughout the document from ‘C8051F52x/F52xA/F53x/F53xA’ to ‘C8051F52x/53x’.
- Updated supply voltage to "2.0 to 5.25 V" on page 1 and in Section 1 on page 13.
- Corrected reference to development kit (C8051F530DK) in Section “1.2.4. On-Chip Debug Circuitry” on page 18.
- Updated minimum Supply Input Voltage (V_{REGIN}) for C8051F52x-C/F53x-C devices in Table 2.2 on page 26 and Table 2.6 on page 30.
- Updated digital supply current (I_{DD} and Idle I_{DD}) typical values for condition ‘Clock = 25 MHz’ in Table 2.2 on page 26.
- Updated I_{DD} Frequency Sensitivity and Idle I_{DD} Frequency Sensitivity values in Table 2.2 on page 26; removed Figure 2.1 and Figure 2.2 that used to provide the same frequency sensitivity slopes. Also removed IDD Supply Sensitivity and Idle IDD Supply Sensitivity typical values.
- Added Digital Supply Current (Stop or Suspend Mode) values at multiple temperatures Table 2.2 on page 26.
- Added a note in Table 2.3, “ADC0 Electrical Characteristics,” on page 28 with reference to Section “4.4. Selectable Gain” on page 60; also added note to indicate that additional tracking time may be necessary if VDD is less than the minimum specified VDD.
- Split off temperature sensor specifications from Table 2.3 into a separate table Table 2.4; Updated temperature sensor gain and added supply current values.
- Added temperature condition for Bias Current specification in Table 2.6 on page 30.
- Updated Comparator Input Offset Voltage values in Table 2.7 on page 31.
- Updated VDD Monitor (VDDMON0) Low Threshold ($V_{RST-LOW}$) minimum value for C8051F52xA/F52x-C/F53xA/F53x-C devices in Table 2.8 on page 32.
- Updated VDD Monitor (VDDMON0) supply current values in Table 2.8 on page 32.
- Added specifications for the new level-sensitive VDD monitor (VDDMON1) to Table 2.8, “Reset Electrical Characteristics,” on page 32 and also added notes to clarify the applicable V_{RST} theshold level.
- Added note in Table 2.9, “Flash Electrical Characteristics,” on page 33 to describe the minimum flash programming temperature for –I (Industrial Grade) devices; Also added the same note and references to it in Section “12.1. Programming The Flash Memory” on page 113, Section “12.3. Non-volatile Data Storage” on page 117, and in SFR Definition 12.1 (PSCTL).