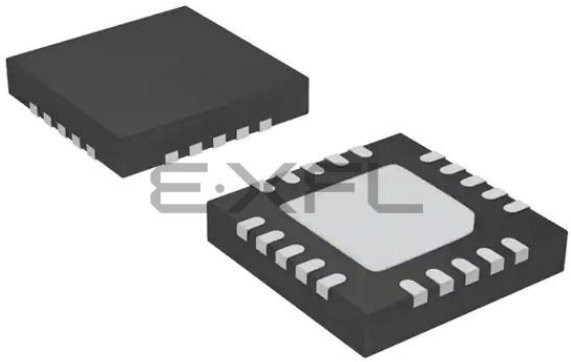

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f533a-imr

1.4. Operating Modes

The C8051F52x/F52xA/F53x/F53xA devices have four operating modes: Active (Normal), Idle, Suspend, and Stop. Active mode occurs during normal operation when the oscillator and peripherals are active. Idle mode halts the CPU while leaving the peripherals and internal clocks active. In Suspend and Stop mode, the CPU is halted, all interrupts and timers are inactive, and the internal oscillator is stopped. The various operating modes are described in Table 1.3 below:

Table 1.3. Operating Modes Summary

	Properties	Power Consumption	How Entered?	How Exited?
Active	■ SYSCLK active ■ CPU active (accessing Flash) ■ Peripherals active or inactive depending on user settings	Full	—	—
Idle	■ SYSCLK active ■ CPU inactive (not accessing Flash) ■ Peripherals active or inactive depending on user settings	Less than Full	IDLE (PCON.0)	Any enabled interrupt or device reset
Suspend	■ Internal oscillator inactive ■ If SYSCLK is derived from the internal oscillator, the peripherals and the CIP-51 will be stopped	Low	SUSPEND (OSCICN.5)	Port 0 event match Port 1 event match Comparator 0 enabled and output is logic 0
Stop	■ SYSCLK inactive ■ CPU inactive (not accessing Flash) ■ Digital peripherals inactive; analog peripherals active or inactive depending on user settings	Very low	STOP (PCON.1)	Device Reset

See Section “8.3. Power Management Modes” on page 89 for Idle and Stop mode details. See Section “14.1.1. Internal Oscillator Suspend Mode” on page 136 for more information on Suspend mode.

Table 2.8. Reset Electrical Characteristics
–40 to +125 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
$\overline{RST}$ Output Low Voltage	I_{OL} = 8.5 mA, V_{DD} = 2.1 V	—	—	0.8	V
$\overline{RST}$ Input High Voltage		0.7 x V_{REGIN}	—	—	V
$\overline{RST}$ Input Low Voltage		—	—	0.3 x V_{REGIN}	V
$\overline{RST}$ Input Pullup Impedance	V_{REGIN} = 1.8 V V_{REGIN} = 2.7 V V_{REGIN} = 3.3 V V_{REGIN} = 5 V	— — — —	330 160 130 80	— — — —	kΩ kΩ kΩ kΩ
Missing Clock Detector Timeout	Time from last system clock rising edge to reset initiation	100	350	650	µs
Reset Time Delay ($T_{PORDelay}$)[1]	Delay between release of any reset source and code execution at location 0x0000	—	—	350	µs
Minimum $\overline{RST}$ Low Time to Generate a System Reset		10	—	—	µs
V_{DD} Monitor (VDDMON0)					
Low Threshold ($V_{RST-LOW}$)[1,2,3]	C8051F52x/53x C8051F52xA/53xA C8051F52x-C/53x-C	1.8 1.65 1.65	1.9 1.75 1.75	2.0 1.8 1.8	V V V
High Threshold ($V_{RST-HIGH}$)[3]	C8051F52x/53x C8051F52xA/53xA C8051F52x-C/53x-C	2.1 2.25 2.25	2.2 2.3 2.3	2.3 2.4 2.45	V V V
Turn-on Time		—	83	—	µs
Supply Current	V_{DD} = 2.1 V	—	1	2	µA
Level-Sensitive V_{DD} Monitor (VDDMON1)[1]					
Threshold (V_{RST1})[1,2,3]	C8051F52x-C/53x-C	1.6	1.75	1.9	V
Supply Current	C8051F52x-C/53x-C	—	3	6	µA

Notes:
1. Refer to Section “20. Device Specific Behavior” on page 210.
2. The POR threshold (V_{RST}) is $V_{RST-LOW}$ or V_{RST1}, whichever is higher.
3. The V_{RST}threshold for power fail / brownout is the higher of VDDMON0 and VDDMON1 thresholds, if both are enabled.

Table 3.7. Pin Definitions for the C8051F53x and C805153xA (QFN 20) (Continued)

Name	Pin Numbers		Type	Description
	'F53xA 'F53x-C	'F53x		
P1.0/	13	13	D I/O or A In	Port 1.0. See Port I/O Section for a complete description.
XTAL2			D I/O	External Clock Output. For an external crystal or resonator, this pin is the excitation driver. This pin is the external clock input for CMOS, capacitor, or RC oscillator configurations. Section "14. Oscillators" on page 135.
P0.7/	14	14	D I/O or	Port 0.7. See Port I/O Section for a complete description.
XTAL1			A In	External Clock Input. This pin is the external oscillator return for a crystal or resonator. See Oscillator Section.
P0.6/	15	15	D I/O or A In	Port 0.6. See Port I/O Section for a complete description.
C2D			D I/O	Bi-directional data signal for the C2 Debug Interface.
P0.5/RX*	16	—	D I/O or A In	Port 0.5. See Port I/O Section for a complete description.
P0.5	—	16	D I/O or A In	Port 0.5. See Port I/O Section for a complete description.
P0.4/TX*	17	—	D I/O or A In	Port 0.4. See Port I/O Section for a complete description.
P0.4/RX*	—	17	D I/O or A In	Port 0.4. See Port I/O Section for a complete description.
P0.3	18	—	D I/O or A In	Port 0.3. See Port I/O Section for a complete description.
P0.3/TX*	—	18	D I/O or A In	Port 0.3. See Port I/O Section for a complete description.
P0.2	19	19	D I/O or A In	Port 0.2. See Port I/O Section for a complete description.
P0.1	20	20	D I/O or A In	Port 0.1. See Port I/O Section for a complete description.
Note: Please refer to Section "20. Device Specific Behavior" on page 210.				

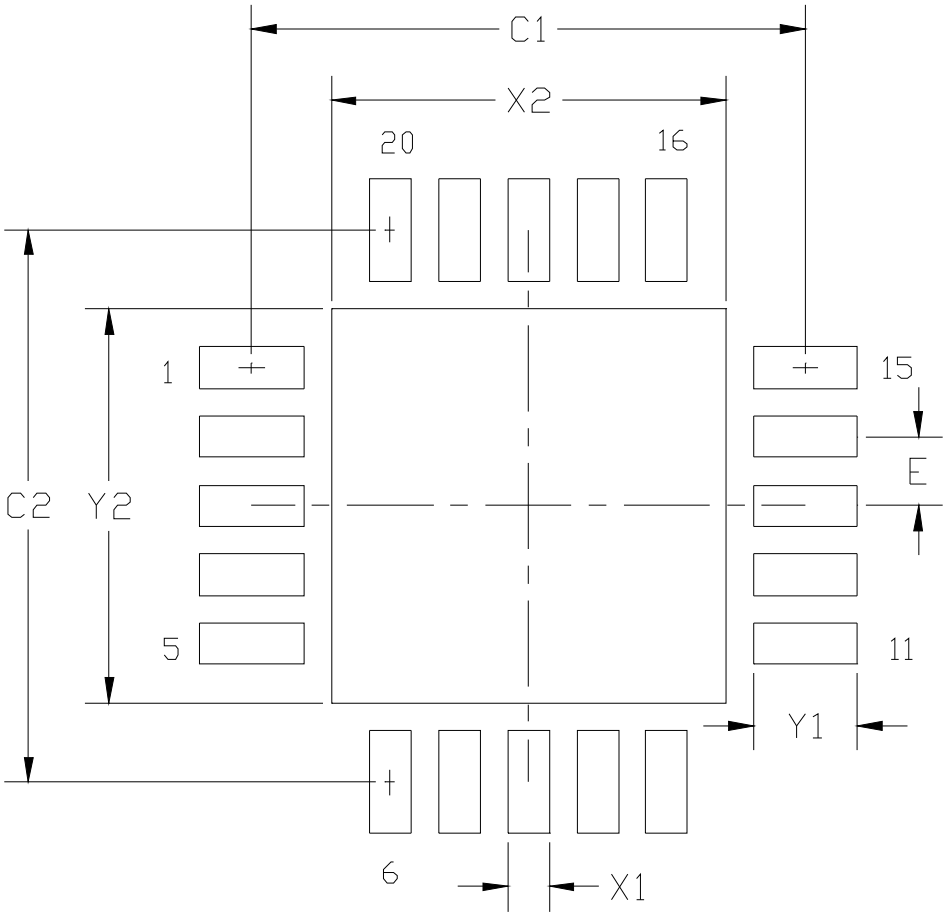


Figure 3.9. QFN-20 Landing Diagram*

Note: The Landing Dimensions are given in Table 3.9, “QFN-20 Landing Diagram Dimensions,” on page 51.

4.3.6. Settling Time Requirements

A minimum tracking time is required before an accurate conversion can be performed. This tracking time is determined by the AMUX0 resistance, the ADC0 sampling capacitance, any external source resistance, and the accuracy required for the conversion.

Figure 4.6 shows the equivalent ADC0 input circuit. The required ADC0 settling time for a given settling accuracy (SA) may be approximated by Equation 4.1. When measuring the Temperature Sensor output, use the settling time specified in Table 2.3 on page 28. See Table 2.3 on page 28 for ADC0 minimum settling time requirements.

$$t = \ln\left(\frac{2^n}{SA}\right) \times R_{TOTAL} C_{SAMPLE}$$

Equation 4.1. ADC0 Settling Time Requirements

Where:
SA is the settling accuracy, given as a fraction of an LSB (for example, 0.25 to settle within 1/4 LSB)
t is the required settling time in seconds
R_{TOTAL} is the sum of the AMUX0 resistance and any external source resistance.
n is the ADC resolution in bits (12).

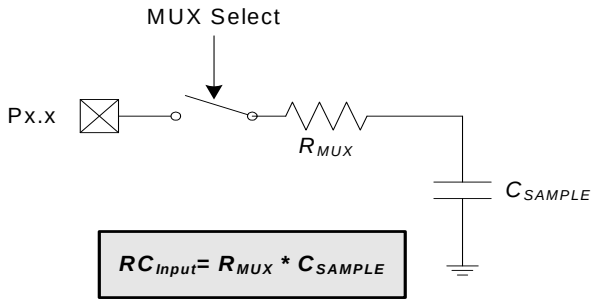


Figure 4.6. ADC0 Equivalent Input Circuits

4.4. Selectable Gain

ADC0 on the C8051F52x/52xA/53x/53xA family of devices implements a selectable gain adjustment option. By writing a value to the gain adjust address range, the user can select gain values between 0 and 1.016.

For example, three analog sources to be measured have full-scale outputs of 5.0 V, 4.0 V, and 3.0 V, respectively. Each ADC measurement would ideally use the full dynamic range of the ADC with an internal voltage reference of 1.5 V or 2.2 V (set to 2.2 V for this example). When selecting signal one (5.0 V full-scale), a gain value of 0.44 (5 V full scale * 0.44 = 2.2 V full scale) provides a full-scale signal of 2.2 V when the input signal is 5.0 V. Likewise, a gain value of 0.55 (4 V full scale * 0.55 = 2.2 V full scale) for the second source and 0.73 (3 V full scale * 0.73 = 2.2 V full scale) for the third source provide full-scale ADC0 measurements when the input signal is full-scale.

Additionally, some sensors or other input sources have small part-to-part variations that must be accounted for to achieve accurate results. In this case, the programmable gain value could be used as a calibration value to eliminate these part-to-part variations.

SFR Definition 4.9. ADC0TK: ADC0 Tracking Mode Select

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
AD0PWR				AD0TM		AD0TK		11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
							(bit addressable)	0xBA

Bits7–4: **AD0PWR3–0**: ADC0 Burst Power-Up Time.
For BURSTEN = 0:
ADC0 power state controlled by AD0EN.
For BURSTEN = 1 and AD0EN = 1;
ADC0 remains enabled and does not enter the very low power state.
For BURSTEN = 1 and AD0EN = 0:
ADC0 enters the very low power state as specified in Table 2.3 on page 28 and is enabled after each convert start signal. The Power Up time is programmed according to the following equation:

$$AD0PWR = \frac{Tstartup}{200ns} - 1 \quad \text{or} \quad Tstartup = (AD0PWR + 1)200ns$$

Bits3–2: **AD0TM1–0**: ADC0 Tracking Mode Select Bits.
00: Reserved.
01: ADC0 is configured to Post-Tracking Mode.
10: ADC0 is configured to Pre-Tracking Mode.
11: ADC0 is configured to Dual-Tracking Mode (default).

Bits1–0: **AD0TK1–0**: ADC0 Post-Track Time.
Post-Tracking time is controlled by AD0TK as follows:
00: Post-Tracking time is equal to 2 SAR clock cycles + 2 FCLK cycles.
01: Post-Tracking time is equal to 4 SAR clock cycles + 2 FCLK cycles.
10: Post-Tracking time is equal to 8 SAR clock cycles + 2 FCLK cycles.
11: Post-Tracking time is equal to 16 SAR clock cycles + 2 FCLK cycles.

SFR Definition 7.2. CPT0MX: Comparator0 MUX Selection

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
CMX0N3	CMX0N2	CMX0N1	CMX0N0	CMX0P3	CMX0P2	CMX0P1	CMX0P0	01110111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x9F

Bits7–4: **CMX0N3–CMX0N0**: Comparator0 Negative Input MUX Select.
These bits select which Port pin is used as the Comparator0 negative input.

CMX0N3	CMX0N2	CMX0N1	CMX0N0	Negative Input
0	0	0	0	P0.1
0	0	0	1	P0.3
0	0	1	0	P0.5
0	0	1	1	P0.7*
0	1	0	0	P1.1*
0	1	0	1	P1.3*
0	1	1	0	P1.5*
0	1	1	1	P1.7*

***Note:** Available only on the C8051F53x/53xA devices

Bits1–0: **CMX0P3–CMX0P0**: Comparator0 Positive Input MUX Select.
These bits select which Port pin is used as the Comparator0 positive input.

CMX0P3	CMX0P2	CMX0P1	CMX0P0	Positive Input
0	0	0	0	P0.0
0	0	0	1	P0.2
0	0	1	0	P0.4
0	0	1	1	P0.6*
0	1	0	0	P1.0*
0	1	0	1	P1.2*
0	1	1	0	P1.4*
0	1	1	1	P1.6*

***Note:** Available only on the C8051F53x/53xA devices.

8. CIP-51 Microcontroller

The MCU system controller core is the CIP-51 microcontroller. The CIP-51 is fully compatible with the MCS-51™ instruction set. Standard 803x/805x assemblers and compilers can be used to develop software. The C8051F52x/F52xA/F53x/F53xA family has a superset of all the peripherals included with a standard 8051. See Section “1. System Overview” on page 13 for more information about the available peripherals. The CIP-51 includes on-chip debug hardware which interfaces directly with the analog and digital subsystems, providing a complete data acquisition or control-system solution in a single integrated circuit.

The CIP-51 Microcontroller core implements the standard 8051 organization and peripherals as well as additional custom peripherals and functions to extend its capability (see Figure 8.1 for a block diagram). The CIP-51 core includes the following features:

- Fully Compatible with MCS-51 Instruction Set
- 25 MIPS Peak Throughput
- 256 Bytes of Internal RAM
- Extended Interrupt Handler
- Reset Input
- Power Management Modes
- Integrated Debug Logic
- Program and Data Memory Security

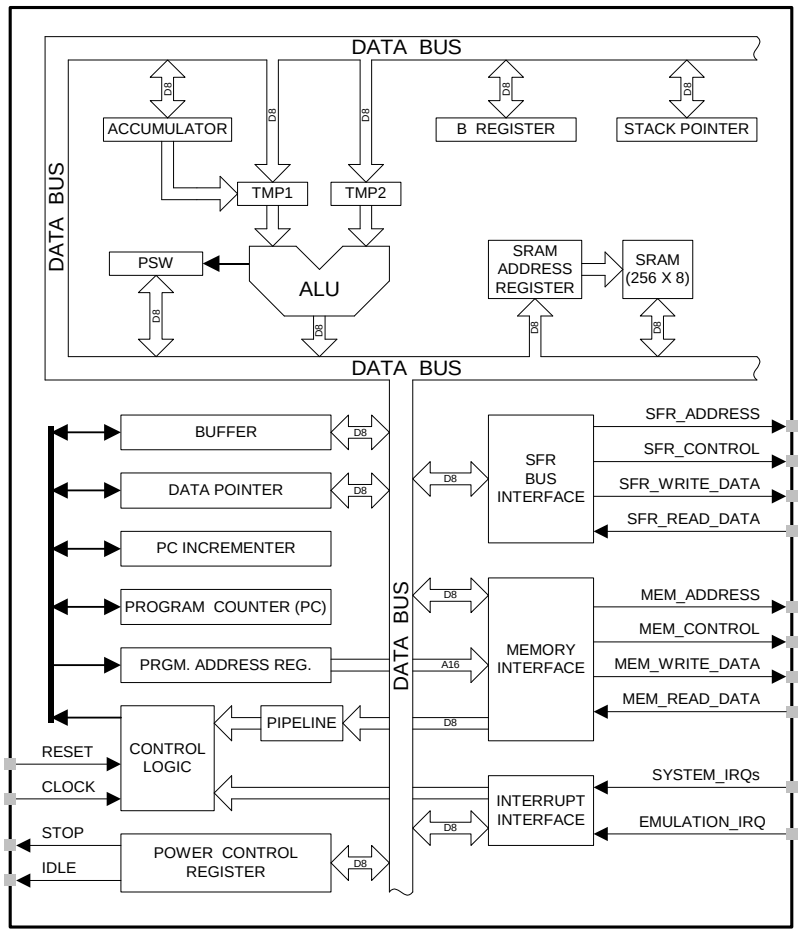


Figure 8.1. CIP-51 Block Diagram

SFR Definition 8.1. SP: Stack Pointer

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x81

Bits7–0: **SP**: Stack Pointer.
The Stack Pointer holds the location of the top of the stack. The stack pointer is incremented before every PUSH operation. The SP register defaults to 0x07 after reset.

SFR Definition 8.2. DPL: Data Pointer Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x82

Bits7–0: **DPL**: Data Pointer Low.
The DPL register is the low byte of the 16-bit DPTR. DPTR is used to access indirectly addressed XRAM and Flash memory.

SFR Definition 8.3. DPH: Data Pointer High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x83

Bits7–0: **DPH**: Data Pointer High.
The DPH register is the high byte of the 16-bit DPTR. DPTR is used to access indirectly addressed XRAM and Flash memory.

SFR Definition 8.4. PSW: Program Status Word

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	Reset Value
CY	AC	F0	RS1	RS0	OV	F1	PARITY	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0xD0

Bit7: **CY**: Carry Flag.
This bit is set when the last arithmetic operation resulted in a carry (addition) or a borrow (subtraction). It is cleared to 0 by all other arithmetic operations.

Bit6: **AC**: Auxiliary Carry Flag
This bit is set when the last arithmetic operation resulted in a carry into (addition) or a borrow from (subtraction) the high order nibble. It is cleared to 0 by all other arithmetic operations.

Bit5: **F0**: User Flag 0.
This is a bit-addressable, general purpose flag for use under software control.

Bits4–3: **RS1–RS0**: Register Bank Select.
These bits select which register bank is used during register accesses.

RS1	RS0	Register Bank	Address
0	0	0	0x00–0x07
0	1	1	0x08–0x0F
1	0	2	0x10–0x17
1	1	3	0x18–0x1F

Bit2: **OV**: Overflow Flag.
This bit is set to 1 under the following circumstances:
- An ADD, ADDC, or SUBB instruction causes a sign-change overflow.
- A MUL instruction results in an overflow (result is greater than 255).
- A DIV instruction causes a divide-by-zero condition.

The OV bit is cleared to 0 by the ADD, ADDC, SUBB, MUL, and DIV instructions in all other cases.

Bit1: **F1**: User Flag 1.
This is a bit-addressable, general purpose flag for use under software control.

Bit0: **PARITY**: Parity Flag.
This bit is set to 1 if the sum of the eight bits in the accumulator is odd and cleared if the sum is even.

8.3.1. Idle Mode

Setting the Idle Mode Select bit (PCON.0) causes the CIP-51 to halt the CPU and enter Idle mode as soon as the instruction that sets the bit completes execution. All internal registers and memory maintain their original data. All analog and digital peripherals can remain active during Idle mode.

Idle mode is terminated when an enabled interrupt is asserted or a reset occurs. The assertion of an enabled interrupt will cause the Idle Mode Selection bit (PCON.0) to be cleared and the CPU to resume operation. The pending interrupt will be serviced and the next instruction to be executed after the return from interrupt (RETI) will be the instruction immediately following the one that set the Idle Mode Select bit. If Idle mode is terminated by an internal or external reset, the CIP-51 performs a normal reset sequence and begins program execution at address 0x0000.

If enabled, the Watchdog Timer (WDT) will eventually cause an internal watchdog reset and thereby terminate the Idle mode. This feature protects the system from an unintended permanent shutdown in the event of an inadvertent write to the PCON register. If this behavior is not desired, the WDT may be disabled by software prior to entering the Idle mode if the WDT was initially configured to allow this operation. This provides the opportunity for additional power savings, allowing the system to remain in the Idle mode indefinitely, waiting for an external stimulus to wake up the system.

8.3.2. Stop Mode

Setting the Stop Mode Select bit (PCON.1) causes the CIP-51 to enter Stop mode as soon as the instruction that sets the bit completes execution. In Stop mode the internal oscillator, CPU, and all digital peripherals are stopped; the state of the external oscillator circuit is not affected. Each analog peripheral (including the external oscillator circuit) may be shut down individually prior to entering Stop Mode. Stop mode can only be terminated by an internal or external reset. On reset, the CIP-51 performs the normal reset sequence and begins program execution at address 0x0000.

If enabled, the Missing Clock Detector will cause an internal reset and thereby terminate the Stop mode. The Missing Clock Detector should be disabled if the CPU is to be put to in STOP mode for longer than the MCD timeout period of 100 µs.

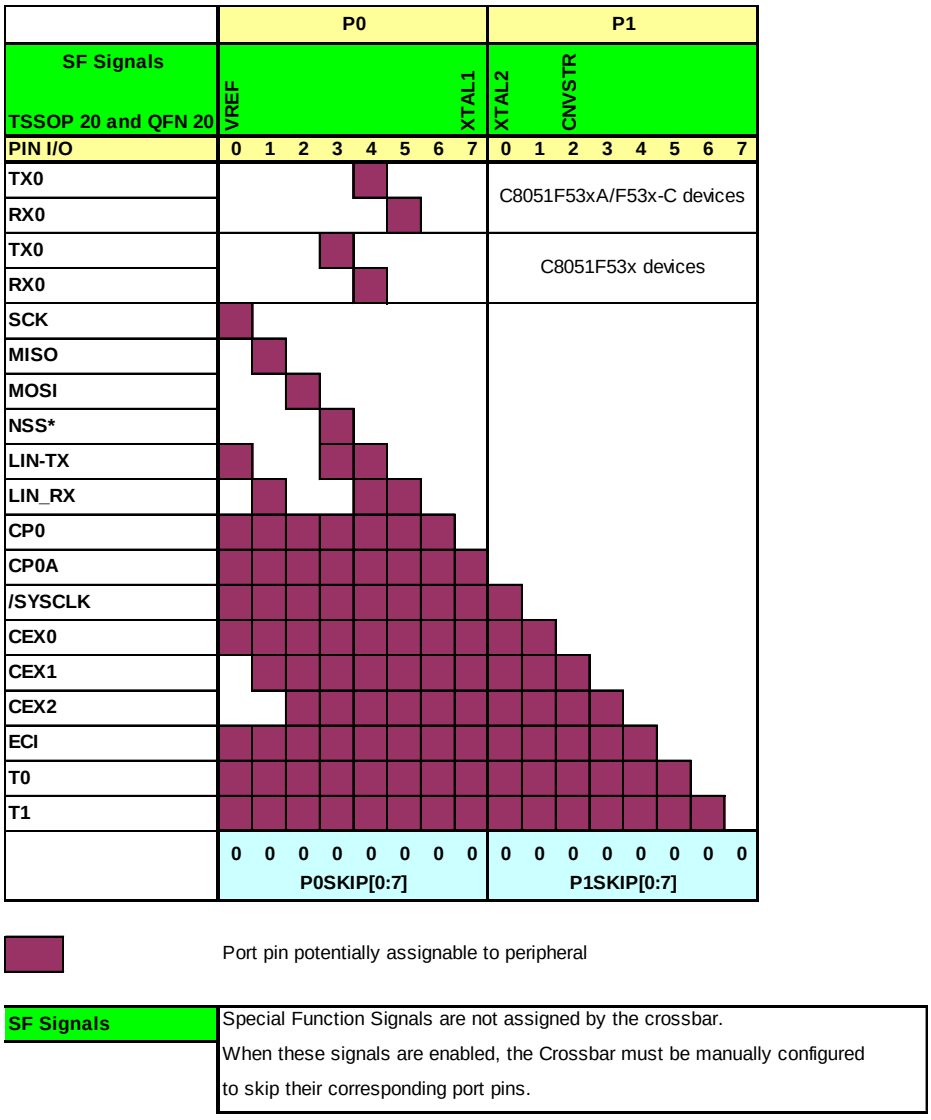
8.3.3. Suspend Mode

The C8051F52x/F52xA/F53x/F53xA devices feature a low-power Suspend mode, which stops the internal oscillator until a wakening event occurs. See Section Section “14.1.1. Internal Oscillator Suspend Mode” on page 136 for more information.

Note: When entering Suspend mode, firmware must set the ZTCEN bit in REF0CN (SFR Definition 5.1).

13.1. Priority Crossbar Decoder

The Priority Crossbar Decoder (Figure 13.3) assigns a priority to each I/O function, starting at the top with UART0. When a digital resource is selected, the least-significant unassigned Port pin is assigned to that resource (excluding UART0, which will be assigned to pins P0.4 and P0.5). If a Port pin is assigned, the Crossbar skips that pin when assigning the next selected resource. Additionally, the Crossbar will skip Port pins whose associated bits in the PnSKIP registers are set. The PnSKIP registers allow software to skip Port pins that are to be used for analog input, dedicated functions, or GPIO.



Note: 4-Wire SPI Only.

Figure 13.3. Crossbar Priority Decoder with No Pins Skipped (TSSOP 20 and QFN 20)

Important Note on Crossbar Configuration: If a Port pin is claimed by a peripheral without use of the Crossbar, its corresponding PnSKIP bit should be set. This applies to P1.0 and/or P0.7 (F53x/F53xA) or P0.2 and/or P0.3 (F52x/F52xA) for the external oscillator, P0.0 for V_{REF}, P1.2 (F53x/F53xA) or P0.5

SFR Definition 14.1. OSCICN: Internal Oscillator Control

R/W	R/W	R/W	R	R	R/W	R/W	R/W	Reset Value
IOSCEN1	IOSCEN0	SUSPEND	IFRDY	—	IFCN2	IFCN1	IFCN0	11000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xB2

Bits7–6: **IOSCEN[1:0]**: Internal Oscillator Enable Bits.
00: Oscillator Disabled.
01: Reserved.
10: Reserved.
11: Oscillator Enabled in Normal Mode and Disabled in Suspend Mode.

Bit5: **SUSPEND**: Internal Oscillator Suspend Enable Bit.
Setting this bit to logic 1 places the internal oscillator in SUSPEND mode. The internal oscillator resumes operation when one of the SUSPEND mode awakening events occur.

Bit4: **IFRDY**: Internal Oscillator Frequency Ready Flag.
0: Internal Oscillator is not running at programmed frequency.
1: Internal Oscillator is running at programmed frequency.

Bit3: **UNUSED**. Read = 0b, Write = don't care.

Bits2–0: **IFCN2–0**: Internal Oscillator Frequency Control Bits.
000: SYSCLK derived from Internal Oscillator divided by 128 (default).
001: SYSCLK derived from Internal Oscillator divided by 64.
010: SYSCLK derived from Internal Oscillator divided by 32.
011: SYSCLK derived from Internal Oscillator divided by 16.
100: SYSCLK derived from Internal Oscillator divided by 8.
101: SYSCLK derived from Internal Oscillator divided by 4.
110: SYSCLK derived from Internal Oscillator divided by 2.
111: SYSCLK derived from Internal Oscillator divided by 1.

15.3. Multiprocessor Communications

9-Bit UART mode supports multiprocessor communication between a master processor and one or more slave processors by special use of the ninth data bit. When a master processor wants to transmit to one or more slaves, it first sends an address byte to select the target(s). An address byte differs from a data byte in that its ninth bit is logic 1; in a data byte, the ninth bit is always set to logic 0.

Setting the MCE0 bit (SCON0.5) of a slave processor configures its UART such that when a stop bit is received, the UART will generate an interrupt only if the ninth bit is logic 1 (RB80 = 1) signifying an address byte has been received. In the UART interrupt handler, software will compare the received address with the slave's own assigned 8-bit address. If the addresses match, the slave will clear its MCE0 bit to enable interrupts on the reception of the following data byte(s). Slaves that weren't addressed leave their MCE0 bits set and do not generate interrupts on the reception of the following data bytes, thereby ignoring the data. Once the entire message is received, the addressed slave resets its MCE0 bit to ignore all transmissions until it receives the next address byte.

Multiple addresses can be assigned to a single slave and/or a single address can be assigned to multiple slaves, thereby enabling "broadcast" transmissions to more than one slave simultaneously. The master processor can be configured to receive all transmissions or a protocol can be implemented such that the master/slave role is temporarily reversed to enable half-duplex transmission between the original master and slave(s).

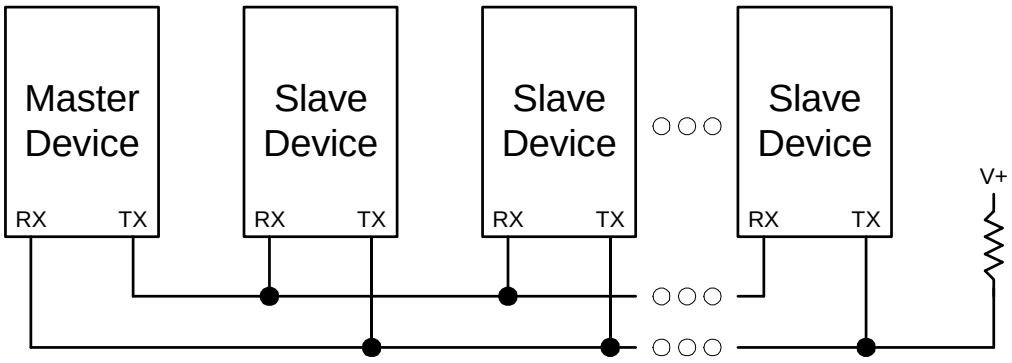


Figure 15.6. UART Multi-Processor Mode Interconnect Diagram

The shift register contents are locked after the slave detects the first edge of SCK. Writes to SPI0DAT that occur after the first SCK edge will be held in the TX latch until the end of the current transfer.

When configured as a slave, SPI0 can be configured for 4-wire or 3-wire operation. The default, 4-wire slave mode, is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 1. In 4-wire mode, the NSS signal is routed to a port pin and configured as a digital input. SPI0 is enabled when NSS is logic 0, and disabled when NSS is logic 1. The bit counter is reset on a falling edge of NSS. Note that the NSS signal must be driven low at least 2 system clocks before the first active edge of SCK for each byte transfer. Figure 16.4 shows a connection diagram between two slave devices in 4-wire slave mode and a master device.

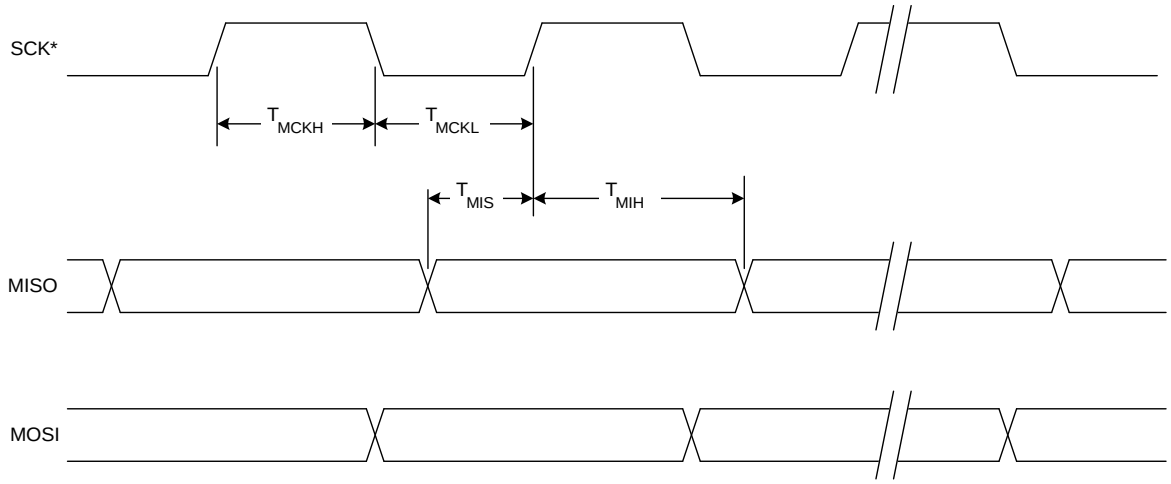
3-wire slave mode is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 0. NSS is not used in this mode, and is not mapped to an external port pin through the crossbar. Since there is not a way of uniquely addressing the device in 3-wire slave mode, SPI0 must be the only slave device present on the bus. It is important to note that in 3-wire slave mode there is no external means of resetting the bit counter that determines when a full byte has been received. The bit counter can only be reset by disabling and re-enabling SPI0 with the SPIEN bit. Figure 16.3 shows a connection diagram between a slave device in 3-wire slave mode and a master device.

16.4. SPI0 Interrupt Sources

When SPI0 interrupts are enabled, the following four flags will generate an interrupt when they are set to logic 1:

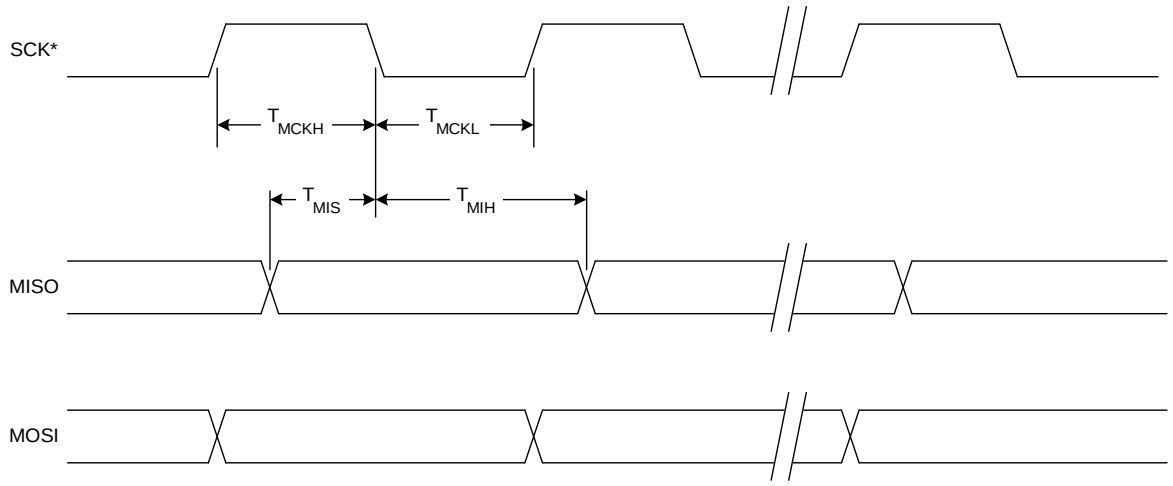
Note that all of the following interrupt bits must be cleared by software.

1. The SPI Interrupt Flag, SPIF (SPI0CN.7) is set to logic 1 at the end of each byte transfer. This flag can occur in all SPI0 modes.
2. The Write Collision Flag, WCOL (SPI0CN.6) is set to logic 1 if a write to SPI0DAT is attempted when the transmit buffer has not been emptied to the SPI shift register. When this occurs, the write to SPI0DAT will be ignored, and the transmit buffer will not be written.This flag can occur in all SPI0 modes.
3. The Mode Fault Flag MODF (SPI0CN.5) is set to logic 1 when SPI0 is configured as a master in multi-master mode and the NSS pin is pulled low. When a Mode Fault occurs, the MSTEN and SPIEN bits in SPI0CN are set to logic 0 to disable SPI0 and allow another master device to access the bus.
4. The Receive Overrun Flag RXOVRN (SPI0CN.4) is set to logic 1 when configured as a slave, and a transfer is completed while the receive buffer still holds an unread byte from a previous transfer. The new byte is not transferred to the receive buffer, allowing the previously received data byte to be read. The data byte which caused the overrun is lost.



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 16.6. SPI Master Timing (CKPHA = 0)



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 16.7. SPI Master Timing (CKPHA = 1)

SFR Definition 17.12. LIN0CTRL: LIN0 Control Register

W	W	W	R/W	R/W	R/W	R/W	R/W	Reset Value
STOP	SLEEP	TXRX	DTACK	RSTINT	RSTERR	WUPREQ	STREQ	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Address: 0x08 (indirect)

Bit7: **STOP**: Stop Communication Processing Bit (**slave mode only**).
This bit is to be set by the application to block the processing of the LIN Communications until the next SYNCH BREAK signal. It is used when the application is handling a data request interrupt and cannot use the frame content with the received identifier (always reads 0).

Bit6: **SLEEP**: Sleep Mode Warning.
This bit is to be set by the application to warn the peripheral that a Sleep Mode Frame was received and that the Bus is in sleep mode or if a Bus Idle timeout interrupt is requested. The application must reset it when a Wake-Up interrupt is requested.

Bit5: **TXRX**: Transmit/Receive Selection Bit.
This bit determines if the current frame is a transmit frame or a receive frame.
0: Current frame is a receive operation.
1: Current frame is a transmit operation.

Bit4: **DTACK**: Data acknowledge bit (**slave mode only**).
Set to 1 after handling a data request interrupt to acknowledge the transfer. The bit will automatically be cleared to 0 by the LIN controller.

Bit3: **RSTINT**: Interrupt Reset bit.
This bit always reads as 0.
0: No effect.
1: Reset the LININT bit (LIN0ST.3).

Bit2: **RSTERR**: Error Reset Bit.
This bit always reads as 0.
0: No effect.
1: Reset the error bits in LIN0ST and LIN0ERR.

Bit1: **WUPREQ**: Wake-Up Request Bit.
Set to 1 to terminate sleep mode by sending a wakeup signal. The bit will automatically be cleared to 0 by the LIN controller.

Bit0: **STREQ**: Start Request Bit (**master mode only**).
1: Start a LIN transmission. This should be set only after loading the identifier, data length and data buffer if necessary.
The bit is reset to 0 upon transmission completion or error detection.

SFR Definition 18.1. TCON: Timer Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable
							SFR Address:	0x88

Bit7: **TF1**: Timer 1 Overflow Flag.
Set by hardware when Timer 1 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 1 interrupt service routine.
0: No Timer 1 overflow detected.
1: Timer 1 has overflowed.

Bit6: **TR1**: Timer 1 Run Control.
0: Timer 1 disabled.
1: Timer 1 enabled.

Bit5: **TF0**: Timer 0 Overflow Flag.
Set by hardware when Timer 0 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 0 interrupt service routine.
0: No Timer 0 overflow detected.
1: Timer 0 has overflowed.

Bit4: **TR0**: Timer 0 Run Control.
0: Timer 0 disabled.
1: Timer 0 enabled.

Bit3: **IE1**: External Interrupt 1.
This flag is set by hardware when an edge/level of type defined by IT1 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 1 service routine if IT1 = 1. When IT1 = 0, this flag is set to 1 when $\overline{INT0}$ is active as defined by bit IN1PL in register IT01CF (see SFR Definition 10.5. "IT01CF: INT0/INT1 Configuration" on page 105).

Bit2: **IT1**: Interrupt 1 Type Select.
This bit selects whether the configured $\overline{INT0}$ interrupt will be edge or level sensitive. $\overline{INT0}$ is configured active low or high by the IN1PL bit in the IT01CF register (see SFR Definition 10.5. "IT01CF: INT0/INT1 Configuration" on page 105).
0: $\overline{INT0}$ is level triggered.
1: $\overline{INT0}$ is edge triggered.

Bit1: **IE0**: External Interrupt 0.
This flag is set by hardware when an edge/level of type defined by IT0 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 0 service routine if IT0 = 1. When IT0 = 0, this flag is set to 1 when $\overline{INT0}$ is active as defined by bit IN0PL in register IT01CF (see SFR Definition 10.5. "IT01CF: INT0/INT1 Configuration" on page 105).

Bit0: **IT0**: Interrupt 0 Type Select.
This bit selects whether the configured $\overline{INT0}$ interrupt will be edge or level sensitive. $\overline{INT0}$ is configured active low or high by the IN0PL bit in register IT01CF (see SFR Definition 10.5. "IT01CF: INT0/INT1 Configuration" on page 105).
0: $\overline{INT0}$ is level triggered.
1: $\overline{INT0}$ is edge triggered.

19.3.1. Watchdog Timer Operation

While the WDT is enabled:

- PCA counter is forced on.
- Writes to PCA0L and PCA0H are not allowed.
- PCA clock source bits (CPS2-CPS0) are frozen.
- PCA Idle control bit (CIDL) is frozen.
- Module 2 is forced into software timer mode.
- Writes to the Module 2 mode register (PCA0CPM2) are disabled.

While the WDT is enabled, writes to the CR bit will not change the PCA counter state; the counter will run until the WDT is disabled. The PCA counter run control (CR) will read zero if the WDT is enabled but user software has not enabled the PCA counter. If a match occurs between PCA0CPH2 and PCA0H while the WDT is enabled, a reset will be generated. To prevent a WDT reset, the WDT may be updated with a write of any value to PCA0CPH2. Upon a PCA0CPH2 write, PCA0H plus the offset held in PCA0CPL2 is loaded into PCA0CPH2 (See Figure 19.10).

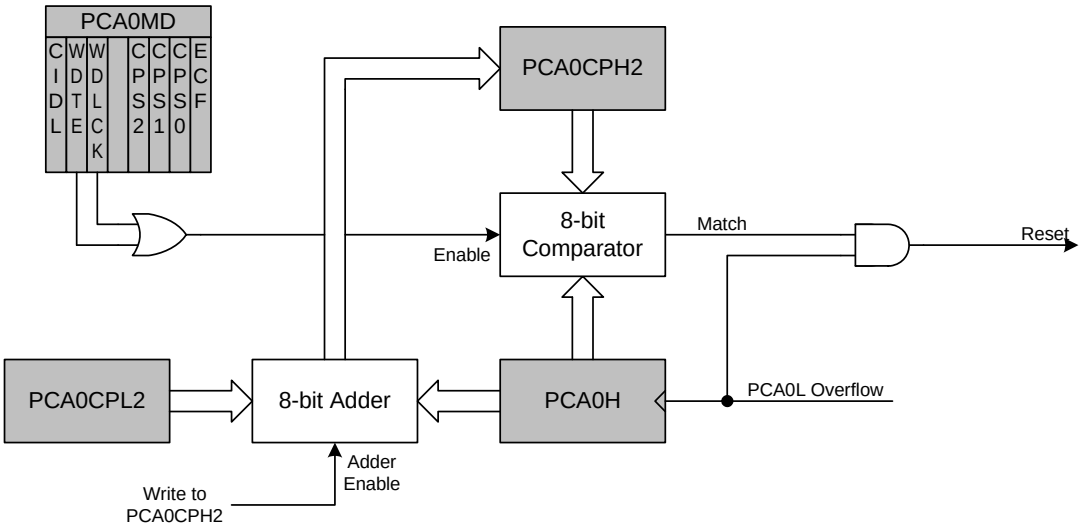


Figure 19.10. PCA Module 2 with Watchdog Timer Enabled

Note that the 8-bit offset held in PCA0CPH2 is compared to the upper byte of the 16-bit PCA counter. This offset value is the number of PCA0L overflows before a reset. Up to 256 PCA clocks may pass before the first PCA0L overflow occurs, depending on the value of the PCA0L when the update is performed. The total offset is then given (in PCA clocks) by Equation 19.4, where PCA0L is the value of the PCA0L register at the time of the update.

$$Offset = (256 \times PCA0CPL2) + (256 - PCA0L)$$

Equation 19.4. Watchdog Timer Offset in PCA Clocks

The WDT reset is generated when PCA0L overflows while there is a match between PCA0CPH2 and PCA0H. Software may force a WDT reset by writing a 1 to the CCF2 flag (PCA0CN.2) while the WDT is enabled.

C2 Register Definition 21.3. REVID: C2 Revision ID

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Reset Value
								Varies

This read-only register returns the 8-bit revision ID.
For example, 0x00 = Revision A.

C2 Register Definition 21.4. FPCTL: C2 Flash Programming Control

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Reset Value
								00000000

Bits7–0 **FPCTL**: Flash Programming Control Register.
This register is used to enable Flash programming via the C2 interface. To enable C2 Flash programming, the following codes must be written in order: 0x02, 0x01. Note that once C2 Flash programming is enabled, a system reset must be issued to resume normal operation.

C2 Register Definition 21.5. FPDAT: C2 Flash Programming Data

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Reset Value
								00000000

Bits7–0: **FPDAT**: C2 Flash Programming Data Register.
This register is used to pass Flash commands, addresses, and data during C2 Flash accesses. Valid commands are listed below.

Code	Command
0x06	Flash Block Read
0x07	Flash Block Write
0x08	Flash Page Erase
0x03	Device Erase