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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f533a-it

Table 2.9. Flash Electrical Characteristics

V_{DD} = 1.8 to 2.75 V; –40 to +125 ºC unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Flash Size	’F520/0A/1/1A and ’F530/0A/1/1A ’F523/3A/4/4A and ’F533/3A/4/4A ’F526/6A/7/7A and ’F536/6A/7/7A	7680 4096 2048	—	—	bytes
Endurance[2]	$V_{DD} \geq V_{RST\text{-}HIGH}$[1]	20 k	150 k	—	Erase/Write
Erase Cycle Time		27	32	38	ms
Write Cycle Time		57	65	74	µs
V_{DD}	Write/Erase Operations	$V_{RST\text{-}HIGH}$[1]	—	—	V

Notes:

1. See Table 2.8 on page 32 for the $V_{RST\text{-}HIGH}$ specification.
2. For –I (industrial Grade) parts, flash should be programmed (erase/write) at a minimum temperature of 0 °C for reliable flash operation across the entire temperature range of –40 to +125 °C. This minimum programming temperature does not apply to –A (Automotive Grade) parts.

Table 2.10. Port I/O DC Electrical Characteristics

V_{REGIN} = 2.7 to 5.25 V, –40 to +125 °C unless otherwise specified

Parameters	Conditions	Min	Typ	Max	Units
Output High Voltage	I_{OH} = –3 mA, Port I/O push-pull I_{OH} = –10 µA, Port I/O push-pull I_{OH} = –10 mA, Port I/O push-pull	V_{REGIN} – 0.4 V_{REGIN} – 0.02 —	— — V_{REGIN} – 0.7	— — —	V
Output Low Voltage	**V_{REGIN} = 2.7 V:** I_{OL} = 70 µA I_{OL} = 8.5 mA **V_{REGIN} = 5.25 V:** I_{OL} = 70 µA I_{OL} = 8.5 mA	 — — — —	 — — — —	 45 550 40 400	mV
Input High Voltage		V_{REGIN} x 0.7	—	—	V
Input Low Voltage		—	—	V_{REGIN} x 0.3	V
Input Leakage Current	Weak Pullup Off **C8051F52xA/53xA:** Weak Pullup On, V_{IN} = 0 V; V_{REGIN} = 1.8 V **C8051F52x/52xA/53x/53xA:** Weak Pullup On, V_{IN} = 0 V; V_{REGIN} = 2.7 V Weak Pullup On, V_{IN} = 0 V; V_{REGIN} = 5.25 V	— — — —	— 5 20 65	±2 15 50 115	µA

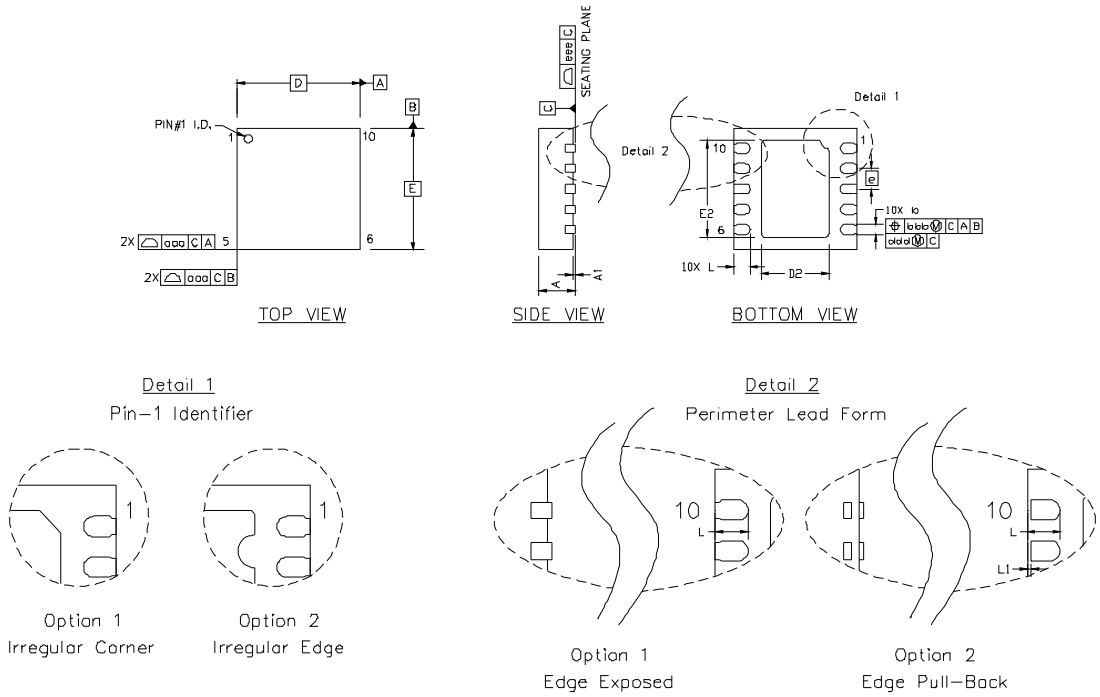


Figure 3.2. DFN-10 Package Diagram

Table 3.2. DFN-10 Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		3.00 BSC.	
D2	1.50	1.65	1.80
e		0.50 BSC.	
E		3.00 BSC.	
E2	2.23	2.38	2.53
L	0.30	0.40	0.50
L1	0.00	—	0.15
aaa	—	—	0.15
bbb	—	—	0.15
ddd	—	—	0.05
eee	—	—	0.08

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VEED except for custom features D2, E2, and L, which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

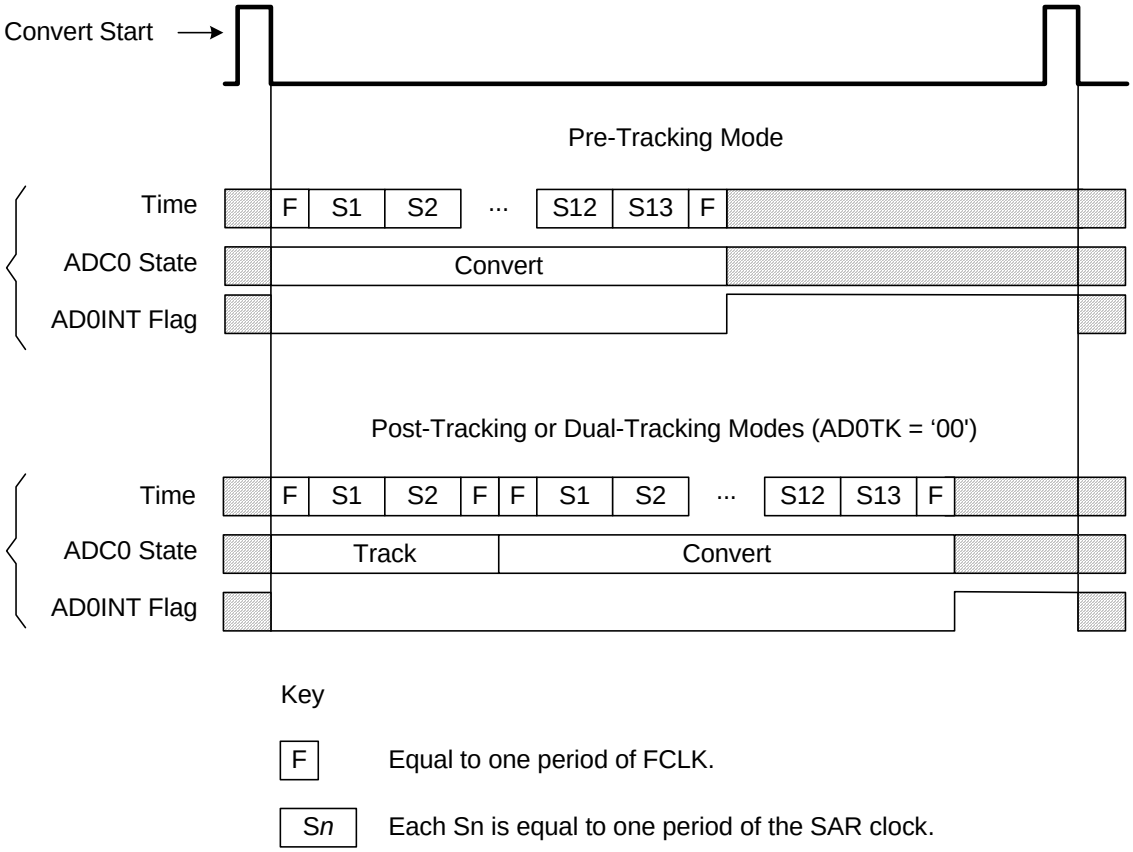


Figure 4.4. 12-Bit ADC Tracking Mode Example

4.3.6. Settling Time Requirements

A minimum tracking time is required before an accurate conversion can be performed. This tracking time is determined by the AMUX0 resistance, the ADC0 sampling capacitance, any external source resistance, and the accuracy required for the conversion.

Figure 4.6 shows the equivalent ADC0 input circuit. The required ADC0 settling time for a given settling accuracy (SA) may be approximated by Equation 4.1. When measuring the Temperature Sensor output, use the settling time specified in Table 2.3 on page 28. See Table 2.3 on page 28 for ADC0 minimum settling time requirements.

$$t = \ln\left(\frac{2^n}{SA}\right) \times R_{TOTAL} C_{SAMPLE}$$

Equation 4.1. ADC0 Settling Time Requirements

Where:
SA is the settling accuracy, given as a fraction of an LSB (for example, 0.25 to settle within 1/4 LSB)
t is the required settling time in seconds
R_{TOTAL} is the sum of the AMUX0 resistance and any external source resistance.
n is the ADC resolution in bits (12).

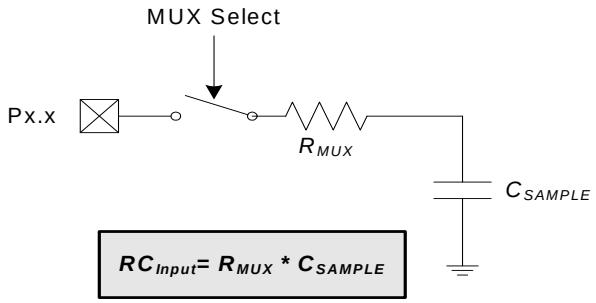


Figure 4.6. ADC0 Equivalent Input Circuits

4.4. Selectable Gain

ADC0 on the C8051F52x/52xA/53x/53xA family of devices implements a selectable gain adjustment option. By writing a value to the gain adjust address range, the user can select gain values between 0 and 1.016.

For example, three analog sources to be measured have full-scale outputs of 5.0 V, 4.0 V, and 3.0 V, respectively. Each ADC measurement would ideally use the full dynamic range of the ADC with an internal voltage reference of 1.5 V or 2.2 V (set to 2.2 V for this example). When selecting signal one (5.0 V full-scale), a gain value of 0.44 (5 V full scale * 0.44 = 2.2 V full scale) provides a full-scale signal of 2.2 V when the input signal is 5.0 V. Likewise, a gain value of 0.55 (4 V full scale * 0.55 = 2.2 V full scale) for the second source and 0.73 (3 V full scale * 0.73 = 2.2 V full scale) for the third source provide full-scale ADC0 measurements when the input signal is full-scale.

Additionally, some sensors or other input sources have small part-to-part variations that must be accounted for to achieve accurate results. In this case, the programmable gain value could be used as a calibration value to eliminate these part-to-part variations.

SFR Definition 4.6. ADC0H: ADC0 Data Word MSB

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xBE

Bits7–0: ADC0 Data Word High-Order Bits.
For AD0LJST = 0 and AD0RPT as follows:
00: Bits 3–0 are the upper 4 bits of the 12-bit result. Bits 7–4 are 0000b.
01: Bits 4–0 are the upper 5 bits of the 14-bit result. Bits 7–5 are 000b.
10: Bits 5–0 are the upper 6 bits of the 15-bit result. Bits 7–6 are 00b.
11: Bits 7–0 are the upper 8 bits of the 16-bit result.
For AD0LJST = 1 (AD0RPT must be '00'): Bits 7–0 are the most-significant bits of the ADC0 12-bit result.

SFR Definition 4.7. ADC0L: ADC0 Data Word LSB

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xBD

Bits7–0: ADC0 Data Word Low-Order Bits.
For AD0LJST = 0: Bits 7–0 are the lower 8 bits of the ADC0 Accumulated Result.
For AD0LJST = 1 (AD0RPT must be '00'): Bits 7–4 are the lower 4 bits of the 12-bit result. Bits 3–0 are 0000b.

5. Voltage Reference

The Voltage reference MUX on C8051F52x/F52xA/F53x/F53xA devices is configurable to use an externally connected voltage reference, the internal reference voltage generator, or the V_{DD} power supply voltage (see Figure 5.1). The REFSL bit in the Reference Control register (REF0CN) selects the reference source. For an external source or the internal reference applied to the V_{REF} pin, REFSL should be set to 0. To use V_{DD} as the reference source, REFSL should be set to 1.

The BIASE bit enables the internal voltage bias generator, which is used by the ADC, Temperature Sensor, and internal oscillators. This bit is forced to logic 1 when any of the aforementioned peripherals are enabled. The bias generator may be enabled manually by writing a 1 to the BIASE bit in register REF0CN; see SFR Definition 5.1 for REF0CN register details. The electrical specifications for the voltage reference circuit are given in Table 2.5 on page 29.

The internal voltage reference circuit consists of a temperature stable bandgap voltage reference generator and a gain-of-two output buffer amplifier. The output voltage is selectable between 1.5 V and 2.2 V. The internal voltage reference can be driven out on the V_{REF} pin by setting the REFBE bit in register REF0CN to a 1 (see Figure 5.1). The load seen by the V_{REF} pin must draw less than 200 µA to GND. When using the internal voltage reference, bypass capacitors of 0.1 µF and 4.7 µF are recommended from the V_{REF} pin to GND. If the internal reference is not used, the REFBE bit should be cleared to 0. Electrical specifications for the internal voltage reference are given in Table 2.5 on page 29.

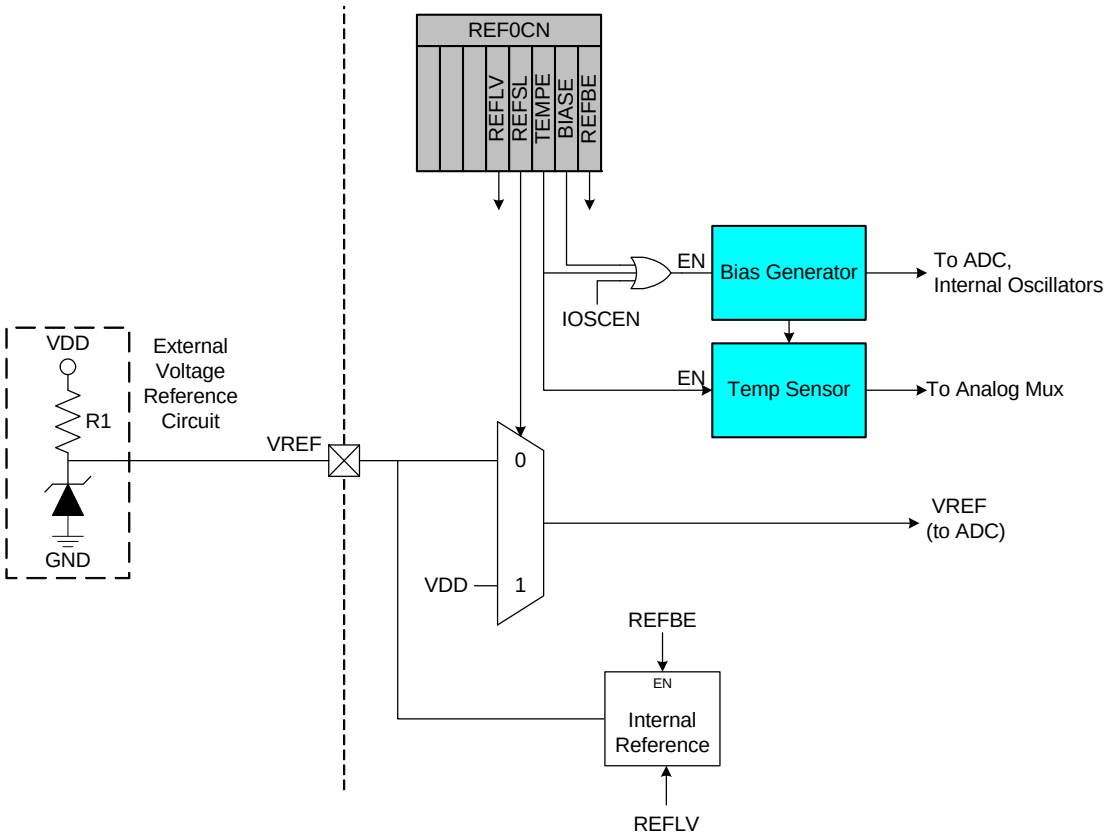


Figure 5.1. Voltage Reference Functional Block Diagram

6. Voltage Regulator (REG0)

C8051F52x/F52xA/F53x/F53xAdevices include an on-chip low dropout voltage regulator (REG0). The input to REG0 at the V_{REGIN} pin can be as high as 5.25 V. The output can be selected by software to 2.1 V or 2.6 V. When enabled, the output of REG0 appears on the V_{DD} pin, powers the microcontroller core, and can be used to power external devices. On reset, REG0 is enabled and can be disabled by software.

The input (V_{REGIN}) and output (V_{DD}) of the voltage regulator should both be bypassed with a large capacitor (4.7 µF + 0.1 µF) to ground. These capacitors are required for regulator stability, and will eliminate power spikes and provide any immediate power required by the microcontroller. The settling time associated with the voltage regulator is shown in Table 2.6 on page 30.

Important Note: The bypass capacitors are required for the stability of the voltage regulator.

The voltage regulator can also generate an interrupt (if enabled by EREG0, EIE1.6) that is triggered whenever the V_{REGIN} input voltage drops below the dropout threshold (see Table 2.6 on page 30). This dropout interrupt has no pending flag. The recommended procedure to use the interrupt is as follows:

1. Wait enough time to ensure the V_{REGIN} input voltage is stable.
2. Enable the dropout interrupt (EREG0, EIE1.6) and select the proper priority (PREG0, EIP1.6).
3. If triggered, disable the interrupt in the Interrupt Service Routine (clear EREG0, EIE1.6) and execute all necessary procedures to put the system in “safe mode,” leaving the interrupt disabled.
4. The main application, now running in safe mode, should regularly check the DROPOUT bit (REG0CN.0). Once it is cleared by the regulator hardware, the application can re-enable the interrupt (EREG0, EIE1.6) and return to normal mode operation.

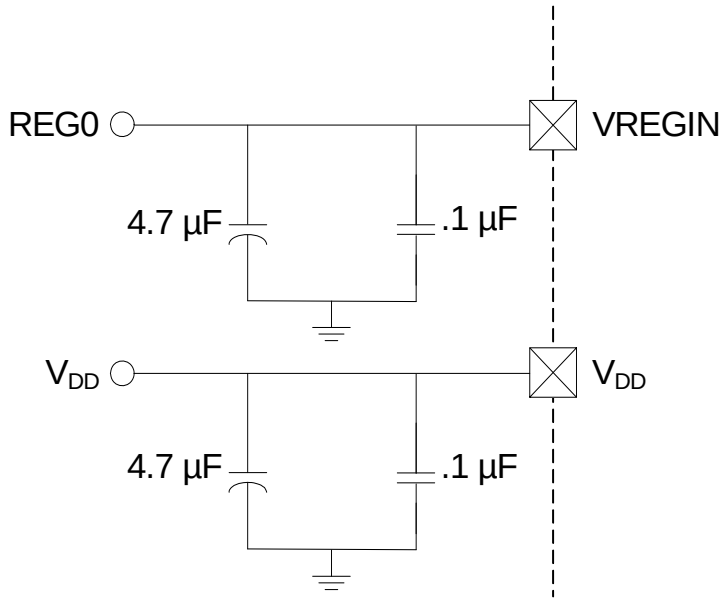


Figure 6.1. External Capacitors for Voltage Regulator Input/Output

less than 100 nA. See Section “13.1. Priority Crossbar Decoder” on page 122 for details on configuring Comparator outputs via the digital Crossbar. Comparator inputs can be externally driven from –0.25 V to (V_{REGIN}) + 0.25 V without damage or upset. The complete Comparator electrical specifications are given in Table 2.7 on page 31.

The Comparator response time may be configured in software via the CPTnMD register (see SFR Definition 7.3). Selecting a longer response time reduces the Comparator supply current. See Table 2.7 on page 31 for complete timing and current consumption specifications.

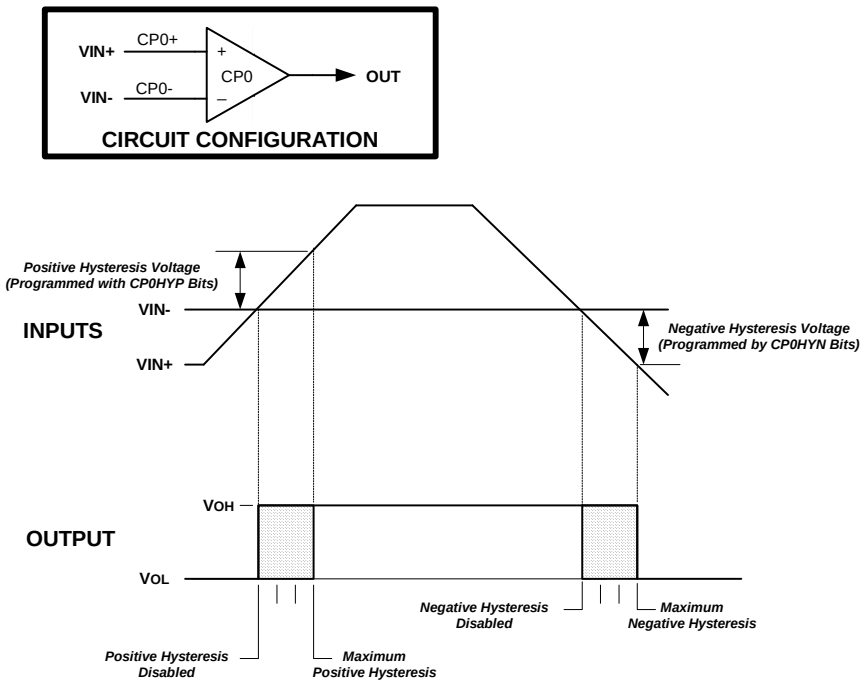


Figure 7.2. Comparator Hysteresis Plot

The Comparator hysteresis is software-programmable via its Comparator Control register CPT0CN. The user can program both the amount of hysteresis voltage (referred to the input voltage) and the positive and negative-going symmetry of this hysteresis around the threshold voltage.

The Comparator hysteresis is programmed using Bits3–0 in the Comparator Control Register CPT0CN (shown in SFR Definition 7.1). The amount of negative hysteresis voltage is determined by the settings of the CP0HYN bits. As shown in Table 2.7 on page 31, settings of 20, 10 or 5 mV of negative hysteresis can be programmed, or negative hysteresis can be disabled. In a similar way, the amount of positive hysteresis is determined by the setting the CP0HYP bits.

Comparator interrupts can be generated on both rising-edge and falling-edge output transitions. (For Interrupt enable and priority control, see Section “10. Interrupt Handler” on page 98). The CP0FIF flag is set to logic 1 upon a Comparator falling-edge detect, and the CP0RIF flag is set to logic 1 upon the Comparator rising-edge detect. Once set, these bits remain set until cleared by software. The output state of the Comparator can be obtained at any time by reading the CP0OUT bit. The Comparator is enabled by setting the CP0EN bit to logic 1 and is disabled by clearing this bit to logic 0. When the Comparator is enabled, the internal oscillator is awakened from SUSPEND mode if the Comparator output is logic 0.

Table 8.1. CIP-51 Instruction Set Summary (Continued)

Mnemonic	Description	Bytes	Clock Cycles
ORL direct, #data	OR immediate to direct byte	3	3
XRL A, Rn	Exclusive-OR Register to A	1	1
XRL A, direct	Exclusive-OR direct byte to A	2	2
XRL A, @Ri	Exclusive-OR indirect RAM to A	1	2
XRL A, #data	Exclusive-OR immediate to A	2	2
XRL direct, A	Exclusive-OR A to direct byte	2	2
XRL direct, #data	Exclusive-OR immediate to direct byte	3	3
CLR A	Clear A	1	1
CPL A	Complement A	1	2
RL A	Rotate A left	1	1
RLC A	Rotate A left through Carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through Carry	1	1
SWAP A	Swap nibbles of A	1	1
Data Transfer			
MOV A, Rn	Move Register to A	1	1
MOV A, direct	Move direct byte to A	2	2
MOV A, @Ri	Move indirect RAM to A	1	2
MOV A, #data	Move immediate to A	2	2
MOV Rn, A	Move A to Register	1	1
MOV Rn, direct	Move direct byte to Register	2	2
MOV Rn, #data	Move immediate to Register	2	2
MOV direct, A	Move A to direct byte	2	2
MOV direct, Rn	Move Register to direct byte	2	2
MOV direct, direct	Move direct byte to direct byte	3	3
MOV direct, @Ri	Move indirect RAM to direct byte	2	2
MOV direct, #data	Move immediate to direct byte	3	3
MOV @Ri, A	Move A to indirect RAM	1	2
MOV @Ri, direct	Move direct byte to indirect RAM	2	2
MOV @Ri, #data	Move immediate to indirect RAM	2	2
MOV DPTR, #data16	Load DPTR with 16-bit constant	3	3
MOVC A, @A+DPTR	Move code byte relative DPTR to A	1	3
MOVC A, @A+PC	Move code byte relative PC to A	1	3
MOVX A, @Ri	Move external data (8-bit address) to A	1	3
MOVX @Ri, A	Move A to external data (8-bit address)	1	3
MOVX A, @DPTR	Move external data (16-bit address) to A	1	3
MOVX @DPTR, A	Move A to external data (16-bit address)	1	3
PUSH direct	Push direct byte onto stack	2	2
POP direct	Pop direct byte from stack	2	2
XCH A, Rn	Exchange Register with A	1	1
XCH A, direct	Exchange direct byte with A	2	2
XCH A, @Ri	Exchange indirect RAM with A	1	2
XCHD A, @Ri	Exchange low nibble of indirect RAM with A	1	2

SFR Definition 8.5. ACC: Accumulator

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0xE0

Bits7–0: **ACC**: Accumulator.
This register is the accumulator for arithmetic operations.

SFR Definition 8.6. B: B Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0xF0

Bits7–0: **B**: B Register.
This register serves as a second accumulator for certain arithmetic operations.

8.3. Power Management Modes

The CIP-51 core has two software programmable power management modes: Idle and Stop. Idle mode halts the CPU while leaving the peripherals and internal clocks active. In Stop mode, the CPU is halted, all interrupts and timers (except the Missing Clock Detector) are inactive, and the internal oscillator is stopped (analog peripherals remain in their selected states; the external oscillator is not affected). Since clocks are running in Idle mode, power consumption is dependent upon the system clock frequency and the number of peripherals left in active mode before entering Idle. Stop mode consumes the least power. SFR Definition 8.7 describes the Power Control Register (PCON) used to control the CIP-51's power management modes.

Although the CIP-51 has Idle and Stop modes built in (as with any standard 8051 architecture), power management of the entire MCU is better accomplished by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers or serial buses, draw little power when they are not in use. Turning off the oscillators lowers power consumption considerably; however a reset is required to restart the MCU.

The C8051F52x/F52xA/F53x/F53xA devices feature a low-power SUSPEND mode, which stops the internal oscillator until a wakening event occurs. See Section “14.1.1. Internal Oscillator Suspend Mode” on page 136 for more information.

8.3.1. Idle Mode

Setting the Idle Mode Select bit (PCON.0) causes the CIP-51 to halt the CPU and enter Idle mode as soon as the instruction that sets the bit completes execution. All internal registers and memory maintain their original data. All analog and digital peripherals can remain active during Idle mode.

Idle mode is terminated when an enabled interrupt is asserted or a reset occurs. The assertion of an enabled interrupt will cause the Idle Mode Selection bit (PCON.0) to be cleared and the CPU to resume operation. The pending interrupt will be serviced and the next instruction to be executed after the return from interrupt (RETI) will be the instruction immediately following the one that set the Idle Mode Select bit. If Idle mode is terminated by an internal or external reset, the CIP-51 performs a normal reset sequence and begins program execution at address 0x0000.

If enabled, the Watchdog Timer (WDT) will eventually cause an internal watchdog reset and thereby terminate the Idle mode. This feature protects the system from an unintended permanent shutdown in the event of an inadvertent write to the PCON register. If this behavior is not desired, the WDT may be disabled by software prior to entering the Idle mode if the WDT was initially configured to allow this operation. This provides the opportunity for additional power savings, allowing the system to remain in the Idle mode indefinitely, waiting for an external stimulus to wake up the system.

8.3.2. Stop Mode

Setting the Stop Mode Select bit (PCON.1) causes the CIP-51 to enter Stop mode as soon as the instruction that sets the bit completes execution. In Stop mode the internal oscillator, CPU, and all digital peripherals are stopped; the state of the external oscillator circuit is not affected. Each analog peripheral (including the external oscillator circuit) may be shut down individually prior to entering Stop Mode. Stop mode can only be terminated by an internal or external reset. On reset, the CIP-51 performs the normal reset sequence and begins program execution at address 0x0000.

If enabled, the Missing Clock Detector will cause an internal reset and thereby terminate the Stop mode. The Missing Clock Detector should be disabled if the CPU is to be put to in STOP mode for longer than the MCD timeout period of 100 µs.

8.3.3. Suspend Mode

The C8051F52x/F52xA/F53x/F53xA devices feature a low-power Suspend mode, which stops the internal oscillator until a wakening event occurs. See Section Section “14.1.1. Internal Oscillator Suspend Mode” on page 136 for more information.

Note: When entering Suspend mode, firmware must set the ZTCEN bit in REF0CN (SFR Definition 5.1).

SFR Definition 10.3. EIE1: Extended Interrupt Enable 1

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
EMAT	EREG0	ELIN	ECPR	ECPF	EPCA0	EADC0	EWADC0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xE6

Bit7: **EMAT**: Enable Port Match Interrupt.
This bit sets the masking of the Port Match interrupt.
0: Disable the Port Match interrupt.
1: Enable the Port Match interrupt.

Bit6: **EREG0**: Enable Voltage Regulator Interrupt.
This bit sets the masking of the Voltage Regulator Dropout interrupt.
0: Disable the Voltage Regulator Dropout interrupt.
1: Enable the Voltage Regulator Dropout interrupt.

Bit5: **ELIN**: Enable LIN Interrupt.
This bit sets the masking of the LIN interrupt.
0: Disable LIN interrupts.
1: Enable LIN interrupt requests.

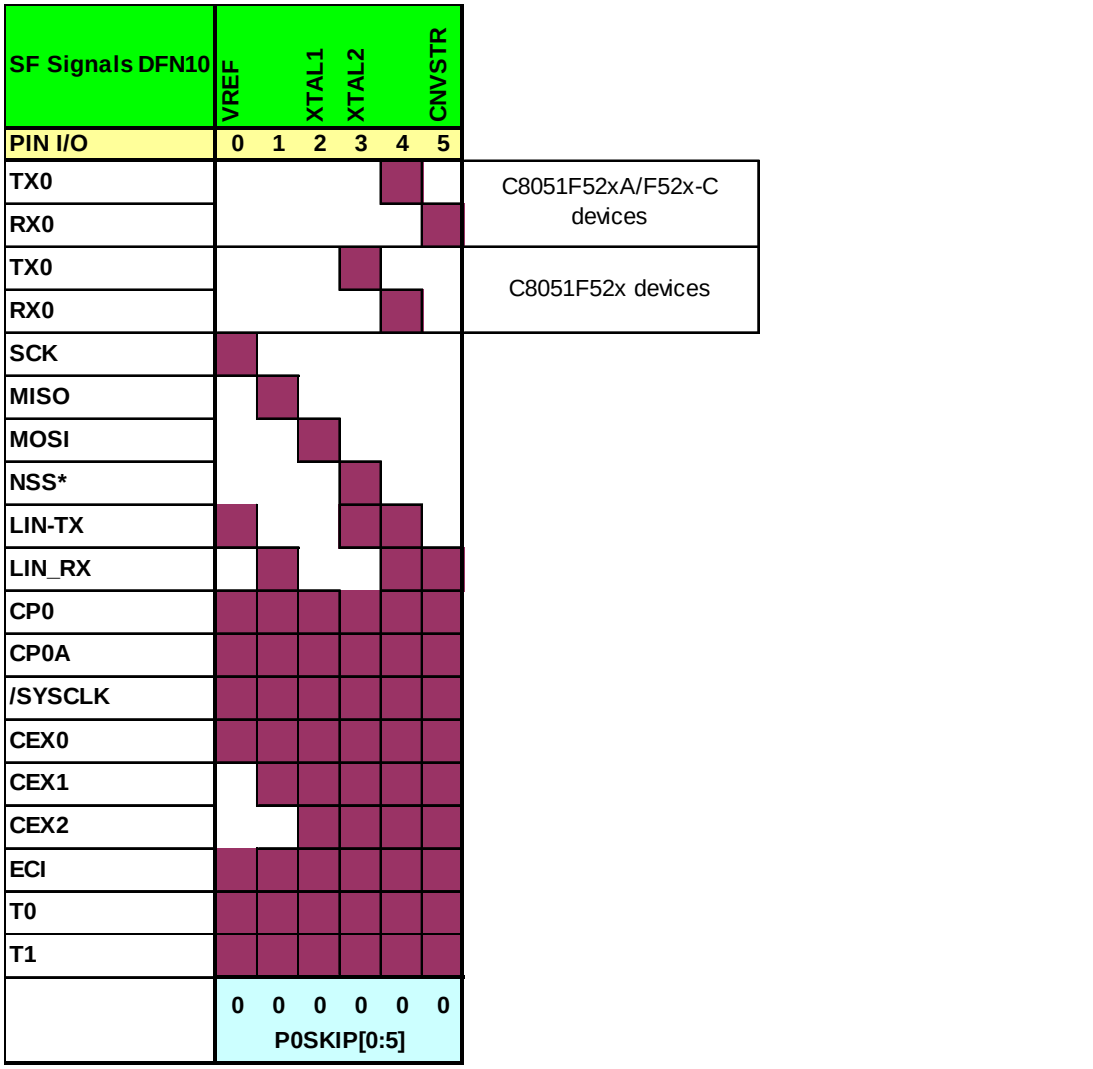
Bit4: **ECPR**: Enable Comparator 0 Rising Edge Interrupt
This bit sets the masking of the CP0 Rising Edge interrupt.
0: Disable CP0 Rising Edge Interrupt.
1: Enable CP0 Rising Edge Interrupt.

Bit3: **ECPF**: Enable Comparator 0 Falling Edge Interrupt
This bit sets the masking of the CP0 Falling Edge interrupt.
0: Disable CP0 Falling Edge Interrupt.
1: Enable CP0 Falling Edge Interrupt.

Bit2: **EPCA0**: Enable Programmable Counter Array (PCA0) Interrupt.
This bit sets the masking of the PCA0 interrupts.
0: Disable all PCA0 interrupts.
1: Enable interrupt requests generated by PCA0.

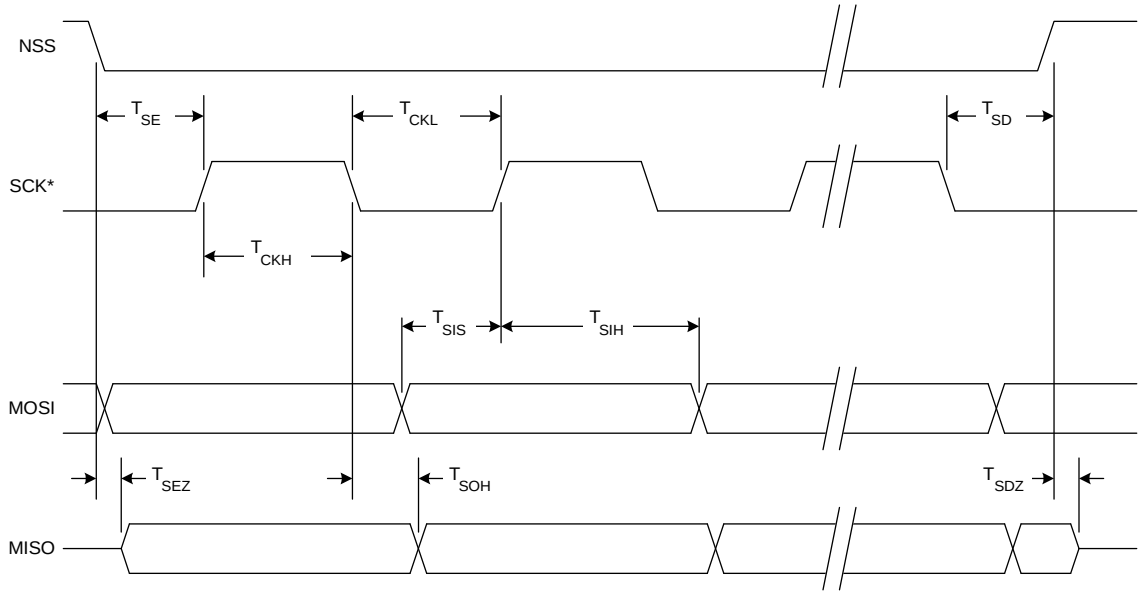
Bit1: **EADC0**: Enable ADC0 Conversion Complete Interrupt.
This bit sets the masking of the ADC0 Conversion Complete interrupt.
0: Disable ADC0 Conversion Complete interrupt.
1: Enable interrupt requests generated by the AD0INT flag.

Bit0: **EWADC0**: Enable ADC0 Window Comparison Interrupt.
This bit sets the masking of the ADC0 Window Comparison interrupt.
0: Disable ADC0 Window Comparison interrupt.
1: Enable interrupt requests generated by the AD0WINT flag.



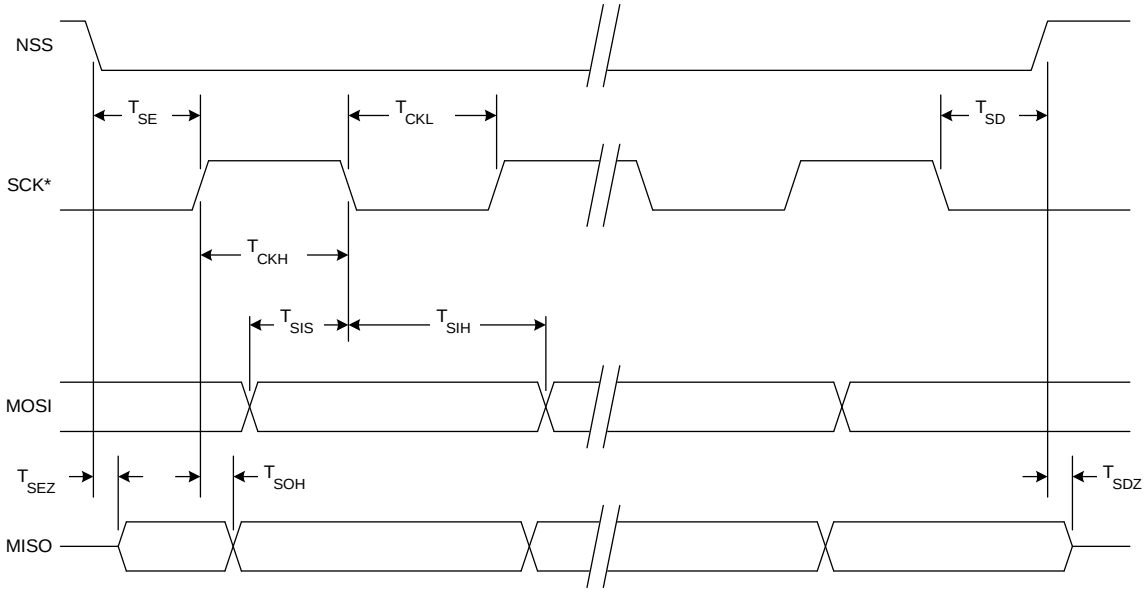
Note: 4-Wire SPI Only.

Figure 13.5. Crossbar Priority Decoder with No Pins Skipped (DFN 10)



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 16.8. SPI Slave Timing (CKPHA = 0)



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 16.9. SPI Slave Timing (CKPHA = 1)

SFR Definition 17.17. LIN0MUL: LIN0 Multiplier Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
PRESCL[1:0]		LINMUL[4:0]					DIV9	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Address: 0x0D (indirect)

Bit7–6: **PRESCL1–0**: LIN Baud Rate Prescaler Bits.
These bits are the baud rate prescaler bits.

Bit5–1: **LINMUL4–0**: LIN Baud Rate Multiplier Bits.
These bits are the baud rate multiplier bits. These bits are not used in slave mode.

Bit0: **DIV9**: LIN Baud Rate Divider Most Significant Bit.
The most significant bit of the baud rate divider. The 8 least significant bits are in LIN0DIV.
The valid range for the divider is 200 to 511.

SFR Definition 17.18. LIN0ID: LIN0 ID Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
		ID[5:0]						00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Address: 0x0E (indirect)

Bit7–6: **UNUSED**. Read = 00b. Write = don't care.

Bit5–0: **ID5–0**: LIN Identifier Bits.
These bits form the data identifier.

If the LINSIZE bits (LIN0SIZE[3:0]) are 1111b, bits ID[5:4] are used to determine the data size and are interpreted as follows:
00: 2 bytes
01: 2 bytes
10: 4 bytes
11: 8 bytes

clocked by the system clock. When T0M is cleared, Timer 0 is clocked by the source selected by the Clock Scale bits in CKCON (see SFR Definition 18.3).

Setting the TR0 bit (TCON.4) enables the timer when either GATE0 (TMOD.3) is logic 0 or the input signal INT0 is active as defined by bit IN0PL in register IT01CF (see SFR Definition 10.5. IT01CF: INT0/INT1 Configuration). Setting GATE0 to 1 allows the timer to be controlled by the external input signal INT0 (see Section “10.4. Interrupt Register Descriptions” on page 100), facilitating pulse width measurements.

TR0	GATE0	INT0	Counter/Timer
0	X	X	Disabled
1	0	X	Enabled
1	1	0	Disabled
1	1	1	Enabled
X = Don't Care			

Setting TR0 does not force the timer to reset. The timer registers should be loaded with the desired initial value before the timer is enabled.

TL1 and TH1 form the 13-bit register for Timer 1 in the same manner as described above for TL0 and TH0. Timer 1 is configured and controlled using the relevant TCON and TMOD bits just as with Timer 0. The input signal INT0 is used with Timer 1; the INT0 polarity is defined by bit IN1PL in register IT01CF (see SFR Definition 10.5. IT01CF: INT0/INT1 Configuration).

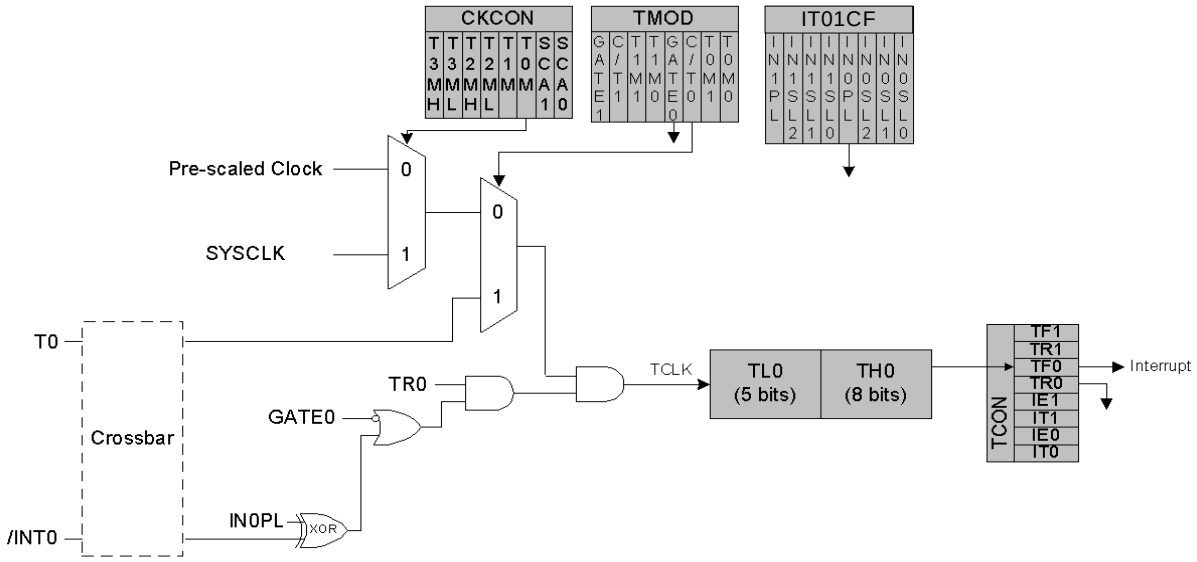


Figure 18.1. T0 Mode 0 Block Diagram

19.2.2. Software Timer (Compare) Mode

In Software Timer mode, the PCA counter/timer value is compared to the module's 16-bit capture/compare register (PCA0CPHn and PCA0CPLn). When a match occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1 and an interrupt request is generated if CCF interrupts are enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Setting the ECOMn and MATn bits in the PCA0CPMn register enables Software Timer mode.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

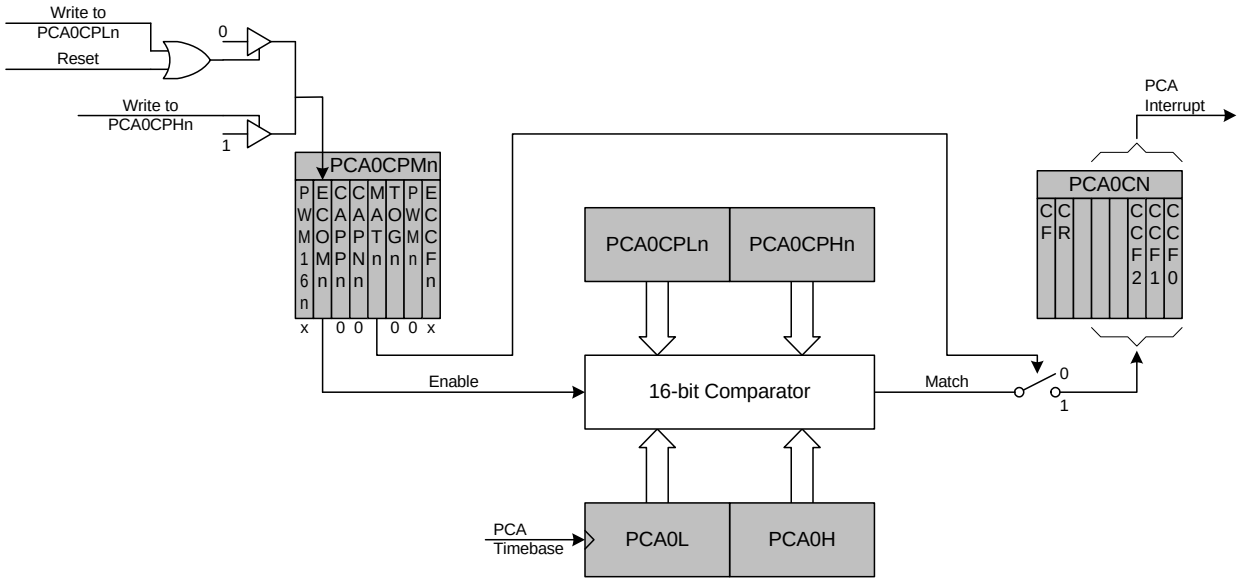


Figure 19.5. PCA Software Timer Mode Diagram

19.2.3. High Speed Output Mode

In High Speed Output mode, a module's associated CEXn pin is toggled each time a match occurs between the PCA Counter and the module's 16-bit capture/compare register (PCA0CPHn and PCA0CPLn) Setting the TOGn, MATn, and ECOMn bits in the PCA0CPMn register enables the High-Speed Output mode.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

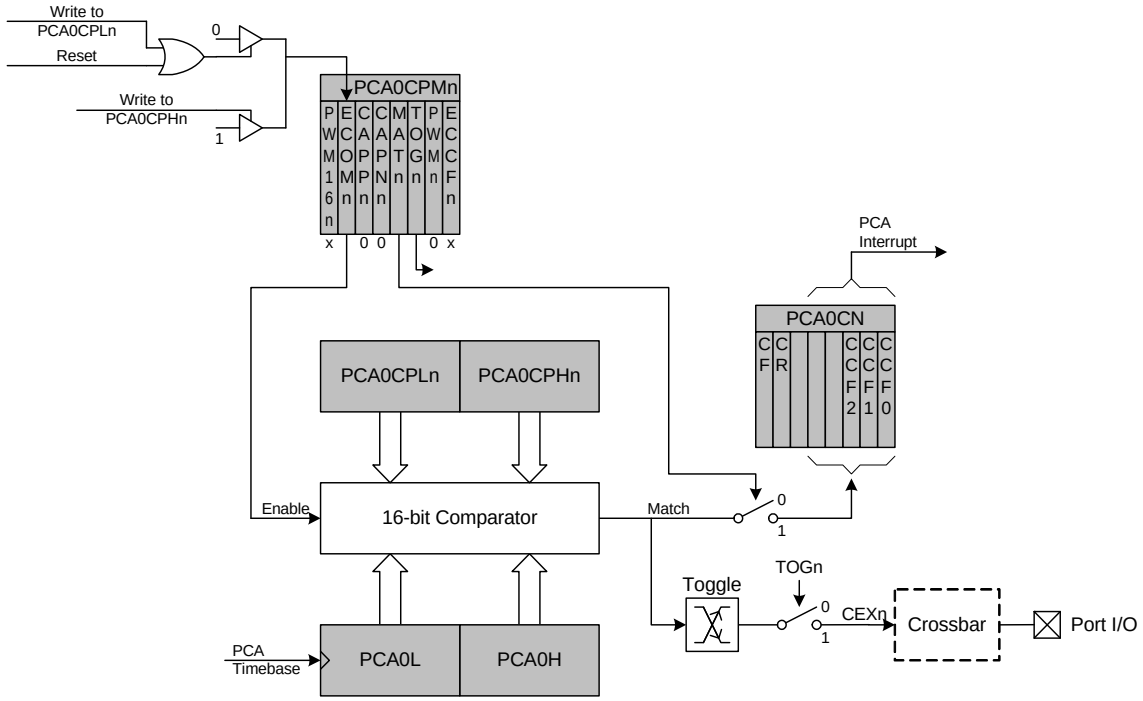


Figure 19.6. PCA High-Speed Output Mode Diagram

Note: The initial state of the Toggle output is logic 1 and is initialized to this state when the module enters High Speed Output Mode.

SFR Definition 19.2. PCA0MD: PCA Mode

R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	Reset Value
CIDL	WDTE	WDLCK	-	CPS2	CPS1	CPS0	ECF	01000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xD9

Bit7: **CIDL**: PCA Counter/Timer Idle Control.
Specifies PCA behavior when CPU is in Idle Mode.
0: PCA continues to function normally while the system controller is in Idle Mode.
1: PCA operation is suspended while the system controller is in Idle Mode.

Bit6: **WDTE**: Watchdog Timer Enable
If this bit is set, PCA Module 2 is used as the watchdog timer.
0: Watchdog Timer disabled.
1: PCA Module 2 enabled as Watchdog Timer.

Bit5: **WDLCK**: Watchdog Timer Lock
This bit locks/unlocks the Watchdog Timer Enable. When WDLCK is set, the Watchdog Timer may not be disabled until the next system reset.
0: Watchdog Timer Enable unlocked.
1: Watchdog Timer Enable locked.

Bit4: **UNUSED**. Read = 0b, Write = don't care.

Bits3–1: **CPS2–CPS0**: PCA Counter/Timer Pulse Select.
These bits select the timebase source for the PCA counter.

CPS2	CPS1	CPS0	Timebase
0	0	0	System clock divided by 12
0	0	1	System clock divided by 4
0	1	0	Timer 0 overflow
0	1	1	High-to-low transitions on ECI (max rate = system clock divided by 4)
1	0	0	System clock
1	0	1	External clock divided by 8*
1	1	0	Reserved
1	1	1	Reserved

Note: External clock divided by 8 is synchronized with the system clock.

Bit0: **ECF**: PCA Counter/Timer Overflow Interrupt Enable.
This bit sets the masking of the PCA Counter/Timer Overflow (CF) interrupt.
0: Disable the CF interrupt.
1: Enable a PCA Counter/Timer Overflow interrupt request when CF (PCA0CN.7) is set.

Note: When the WDTE bit is set to 1, the PCA0MD register cannot be modified. To change the contents of the PCA0MD register, the Watchdog Timer must first be disabled.

Revision 1.2 to 1.3

- Updated “System Overview” on page 13 with a voltage range specification for the internal oscillator.
- Updated Table 2.11 on page 34 with new conditions for the internal oscillator accuracy. The internal oscillator accuracy is dependent on the operating voltage range.
- Updated Section 2 to remove the internal oscillator curve across temperature diagram.
- Updated Figure “4.5 12-Bit ADC Burst Mode Example with Repeat Count Set to 4” on page 58 with new timing diagram when using CNVSTR pin.
- Updated SFR Definition 5.1 (REF0CN) with oscillator suspend requirement for ZTCEN.
- Updated SFR Definition 6.1 (REG0CN) with a new definition for Bit 6. The bit 6 reset value is 1b and must be written to 1b.
- Updated Section “8.3.3. Suspend Mode” on page 90 with note regarding ZTCEN.
- Updated Section “17. LIN (C8051F520/0A/3/3A/6/6A and C8051F530/0A/3/3A/6/6A)” on page 164 with a voltage range specification for the internal oscillator.

Revision 1.3 to 1.4

- Added ‘AEC-Q100’ qualification information on page 1.
- Changed page headers throughout the document from ‘C8051F52x/F52xA/F53x/F53xA’ to ‘C8051F52x/53x’.
- Updated supply voltage to "2.0 to 5.25 V" on page 1 and in Section 1 on page 13.
- Corrected reference to development kit (C8051F530DK) in Section “1.2.4. On-Chip Debug Circuitry” on page 18.
- Updated minimum Supply Input Voltage (V_{REGIN}) for C8051F52x-C/F53x-C devices in Table 2.2 on page 26 and Table 2.6 on page 30.
- Updated digital supply current (I_{DD} and Idle I_{DD}) typical values for condition ‘Clock = 25 MHz’ in Table 2.2 on page 26.
- Updated I_{DD} Frequency Sensitivity and Idle I_{DD} Frequency Sensitivity values in Table 2.2 on page 26; removed Figure 2.1 and Figure 2.2 that used to provide the same frequency sensitivity slopes. Also removed IDD Supply Sensitivity and Idle IDD Supply Sensitivity typical values.
- Added Digital Supply Current (Stop or Suspend Mode) values at multiple temperatures Table 2.2 on page 26.
- Added a note in Table 2.3, “ADC0 Electrical Characteristics,” on page 28 with reference to Section “4.4. Selectable Gain” on page 60; also added note to indicate that additional tracking time may be necessary if VDD is less than the minimum specified VDD.
- Split off temperature sensor specifications from Table 2.3 into a separate table Table 2.4; Updated temperature sensor gain and added supply current values.
- Added temperature condition for Bias Current specification in Table 2.6 on page 30.
- Updated Comparator Input Offset Voltage values in Table 2.7 on page 31.
- Updated VDD Monitor (VDDMON0) Low Threshold ($V_{RST-LOW}$) minimum value for C8051F52xA/F52x-C/F53xA/F53x-C devices in Table 2.8 on page 32.
- Updated VDD Monitor (VDDMON0) supply current values in Table 2.8 on page 32.
- Added specifications for the new level-sensitive VDD monitor (VDDMON1) to Table 2.8, “Reset Electrical Characteristics,” on page 32 and also added notes to clarify the applicable V_{RST} theshold level.
- Added note in Table 2.9, “Flash Electrical Characteristics,” on page 33 to describe the minimum flash programming temperature for –I (Industrial Grade) devices; Also added the same note and references to it in Section “12.1. Programming The Flash Memory” on page 113, Section “12.3. Non-volatile Data Storage” on page 117, and in SFR Definition 12.1 (PSCTL).