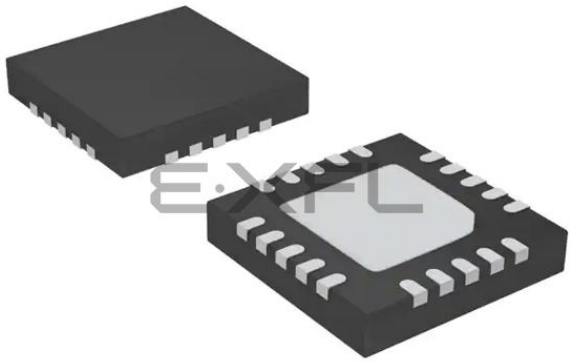

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.25V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f534-c-im

List of Registers

Table 1.2. Product Selection Guide (Not Recommended for New Designs)

Ordering Part Number	Flash Memory (kB)	Port I/Os	LIN	Package	Ordering Part Number	Flash Memory (kB)	Port I/Os	LIN	Package
C8051F520-IM C8051F520A-IM	8	6	✓	DFN-10	C8051F534-IM C8051F534A-IM	4	16	—	QFN-20
C8051F521-IM C8051F521A-IM	8	6	—	DFN-10	C8051F536-IM C8051F536A-IM	2	16	✓	QFN-20
C8051F523-IM C8051F523A-IM	4	6	✓	DFN-10	C8051F537-IM C8051F537A-IM	2	16	—	QFN-20
C8051F524-IM C8051F524A-IM	4	6	—	DFN-10	C8051F530-IT C8051F530A-IT	8	16	✓	TSSOP-20
C8051F526-IM C8051F526A-IM	2	6	✓	DFN-10	C8051F531-IT C8051F531A-IT	8	16	—	TSSOP-20
C8051F527-IM C8051F527A-IM	2	6	—	DFN-10	C8051F533-IT C8051F533A-IT	4	16	✓	TSSOP-20
C8051F530-IM C8051F530A-IM	8	16	✓	QFN-20	C8051F534-IT C8051F534A-IT	4	16	—	TSSOP-20
C8051F531-IM C8051F531A-IM	8	16	—	QFN-20	C8051F536-IT C8051F536A-IT	2	16	✓	TSSOP-20
C8051F533-IM C8051F533A-IM	4	16	✓	QFN-20	C8051F537-IT C8051F537A-IT	2	16	—	TSSOP-20

The part numbers in Table 1.2 are not recommended for new designs. Instead, select the corresponding part number from Table 1.1 (silicon revision C) for your design. In Table 1.2, the part numbers in the format similar to C8051F520-IM are silicon revision A devices. The part numbers in the format similar to C8051F520A-IM are silicon revision B devices.

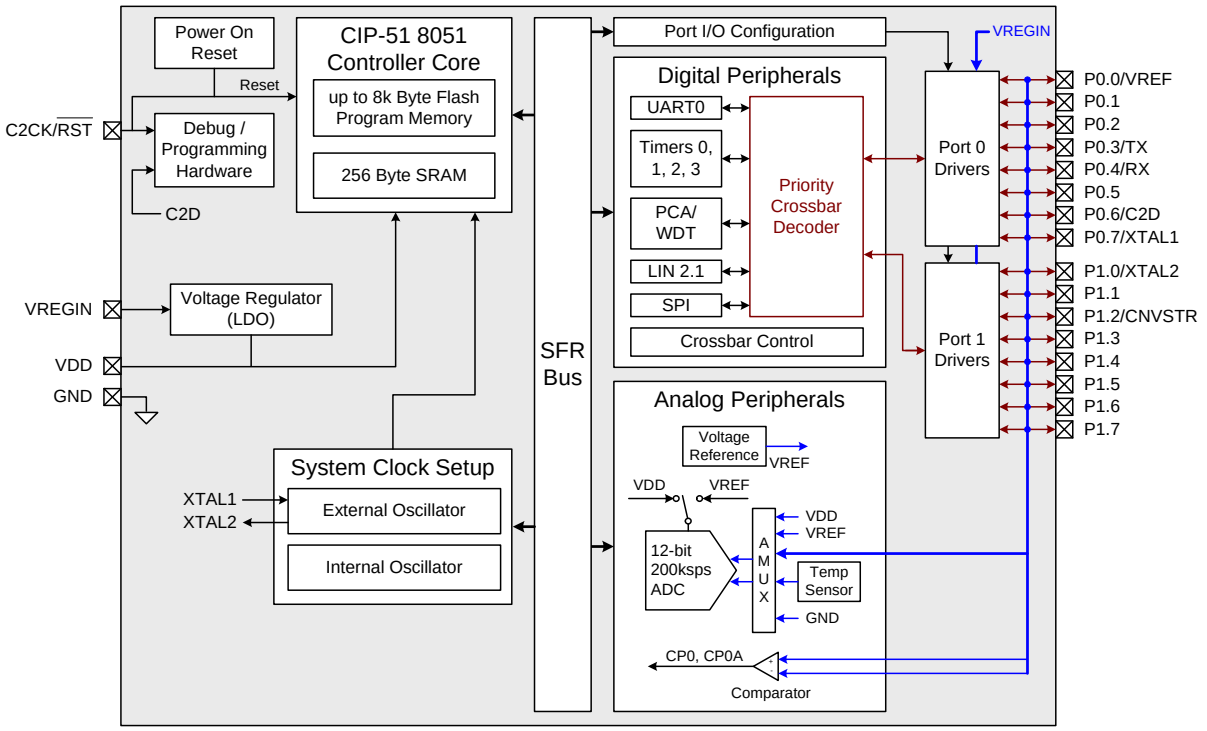


Figure 1.3. C8051F53x Block Diagram (Silicon Revision A)

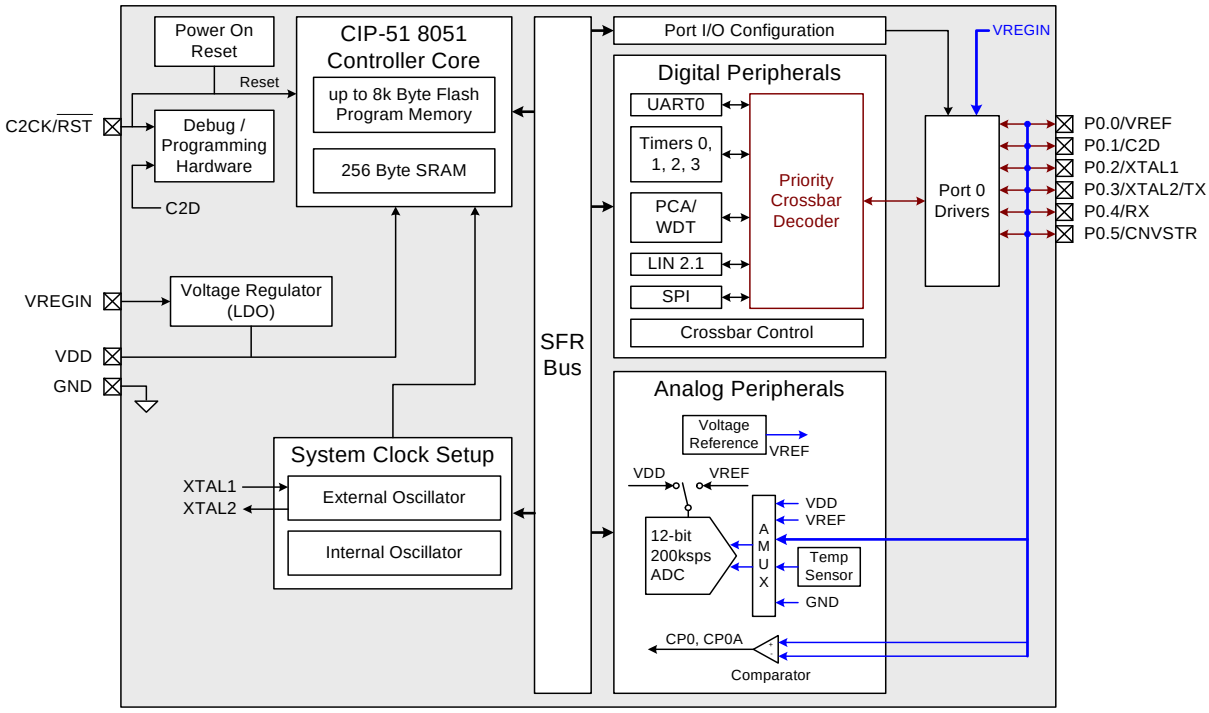


Figure 1.4. C8051F52x Block Diagram (Silicon Revision A)

1.3. On-Chip Memory

The CIP-51 has a standard 8051 program and data address configuration. It includes 256 bytes of data RAM, with the upper 128 bytes dual-mapped. Indirect addressing accesses the upper 128 bytes of general purpose RAM, and direct addressing accesses the 128 byte SFR address space. The lower 128 bytes of RAM are accessible via direct and indirect addressing. The first 32 bytes are addressable as four banks of general purpose registers, and the next 16 bytes can be byte addressable or bit addressable.

Program memory consists of 7680 bytes (’F520/0A/1/1A and ’F530/0A/1/1A), 4 kB (’F523/3A/4/4A and C8051F53x/53xA), or 2 kB (’F526/6A/7/7A and ’F536/6A/7/7A) of Flash. This memory is byte writable and erased in 512-byte sectors, and requires no special off-chip programming voltage.

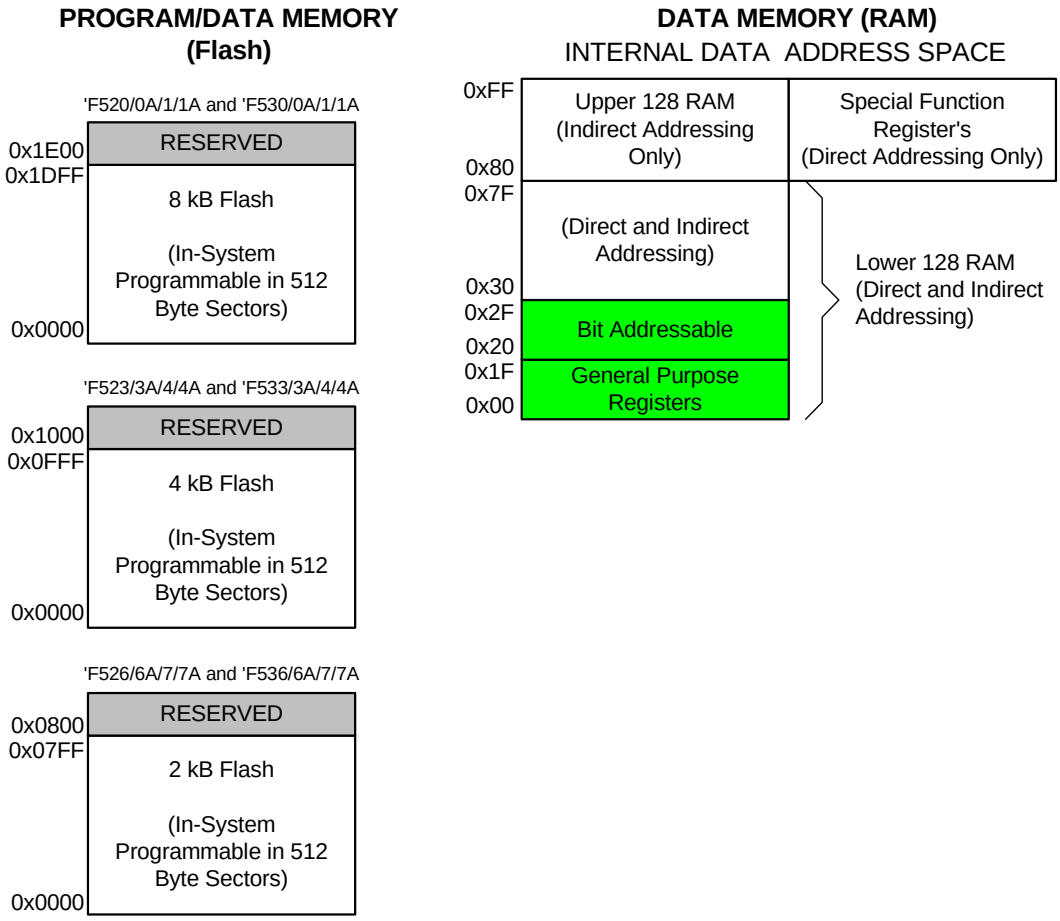


Figure 1.6. Memory Map

2. Electrical Characteristics

2.1. Absolute Maximum Ratings

Table 2.1. Absolute Maximum Ratings

Parameter	Conditions	Min	Typ	Max	Units
Ambient temperature under Bias		–55	—	135	°C
Storage Temperature		–65	—	150	°C
Voltage on V_{REGIN} with Respect to GND		–0.3	—	5.5	V
Voltage on V_{DD} with Respect to GND		–0.3	—	2.8	V
Voltage on XTAL1 with Respect to GND		–0.3	—	V_{REGIN} + 0.3	V
Voltage on XTAL2 with Respect to GND		–0.3	—	V_{REGIN} + 0.3	V
Voltage on any Port I/O Pin or $\overline{RST}$ with Respect to GND		–0.3	—	V_{REGIN} + 0.3	V
Maximum Output Current Sunk by any Port Pin		—	—	100	mA
Maximum Output Current Sourced by any Port Pin		—	—	100	mA
Maximum Total Current through V_{REGIN}, and GND		—	—	500	mA

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 2.4. Temperature Sensor Electrical Characteristics

V_{DD} = 2.1 V, V_{REF} = 1.5 V (REFSL=0), –40 to +125 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Linearity[1]		—	0.1	—	°C
Gain[1]		—	3.33	—	mV/°C
Gain Error[2]		—	±100	—	µV/°C
Offset[1]	Temp = 0 °C	—	890	—	mV
Offset Error[2]	Temp = 0 °C	—	±15	—	mV
Tracking Time		12	—	—	µs
Power Supply Current		—	17	—	µA

Notes:
1. Includes ADC offset, gain, and linearity variations.
2. Represents one standard deviation from the mean.

Table 2.5. Voltage Reference Electrical Characteristics

V_{DD} = 2.1 V; –40 to +125 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Internal Reference (REFBE = 1)					
Output Voltage	I_{DD} ≈ 1 mA; No load on VREF pin and all other GPIO pins. 25 °C ambient (REFLV = 0) 25 °C ambient (REFLV = 1), V_{DD} = 2.6 V	 1.45 2.15	 1.5 2.2	 1.55 2.25	 V
V_{REF} Short-Circuit Current		—	2.5	—	mA
V_{REF} Temperature Coefficient		—	33	—	ppm/°C
Load Regulation	Load = 0 to 200 µA to GND	—	10	—	ppm/µA
V_{REF} Turn-on Time 1	4.7 µF, 0.1 µF bypass	—	21	—	ms
V_{REF} Turn-on Time 2	0.1 µF bypass	—	230	—	µs
Power Supply Rejection		—	2.1	—	mV/V
External Reference (REFBE = 0)					
Input Voltage Range		0	—	V_{DD}	V
Input Current	Sample Rate = 200 ksps; V_{REF} = 1.5 V	—	2.4	—	µA
Bias Generators					
ADC Bias Generator	BIASE = 1	—	22	—	µA
Power Consumption (Internal)		—	35	—	µA

4.3.6. Settling Time Requirements

A minimum tracking time is required before an accurate conversion can be performed. This tracking time is determined by the AMUX0 resistance, the ADC0 sampling capacitance, any external source resistance, and the accuracy required for the conversion.

Figure 4.6 shows the equivalent ADC0 input circuit. The required ADC0 settling time for a given settling accuracy (SA) may be approximated by Equation 4.1. When measuring the Temperature Sensor output, use the settling time specified in Table 2.3 on page 28. See Table 2.3 on page 28 for ADC0 minimum settling time requirements.

$$t = \ln\left(\frac{2^n}{SA}\right) \times R_{TOTAL} C_{SAMPLE}$$

Equation 4.1. ADC0 Settling Time Requirements

Where:
SA is the settling accuracy, given as a fraction of an LSB (for example, 0.25 to settle within 1/4 LSB)
t is the required settling time in seconds
R_{TOTAL} is the sum of the AMUX0 resistance and any external source resistance.
n is the ADC resolution in bits (12).

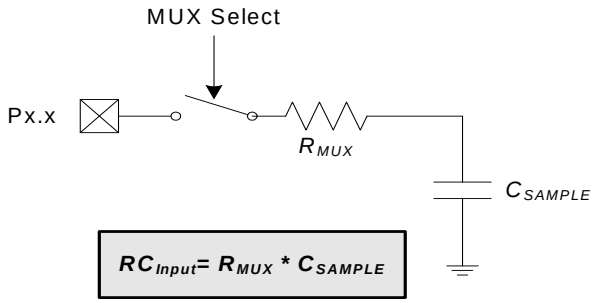


Figure 4.6. ADC0 Equivalent Input Circuits

4.4. Selectable Gain

ADC0 on the C8051F52x/52xA/53x/53xA family of devices implements a selectable gain adjustment option. By writing a value to the gain adjust address range, the user can select gain values between 0 and 1.016.

For example, three analog sources to be measured have full-scale outputs of 5.0 V, 4.0 V, and 3.0 V, respectively. Each ADC measurement would ideally use the full dynamic range of the ADC with an internal voltage reference of 1.5 V or 2.2 V (set to 2.2 V for this example). When selecting signal one (5.0 V full-scale), a gain value of 0.44 (5 V full scale * 0.44 = 2.2 V full scale) provides a full-scale signal of 2.2 V when the input signal is 5.0 V. Likewise, a gain value of 0.55 (4 V full scale * 0.55 = 2.2 V full scale) for the second source and 0.73 (3 V full scale * 0.73 = 2.2 V full scale) for the third source provide full-scale ADC0 measurements when the input signal is full-scale.

Additionally, some sensors or other input sources have small part-to-part variations that must be accounted for to achieve accurate results. In this case, the programmable gain value could be used as a calibration value to eliminate these part-to-part variations.

Table 9.2. Special Function Registers

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Description	Page
ACC	0xE0	Accumulator	89
ADC0CF	0xBC	ADC0 Configuration	65
ADC0CN	0xE8	ADC0 Control	67
ADC0H	0xBE	ADC0	66
ADC0L	0xBD	ADC0	66
ADC0GTH	0xC4	ADC0 Greater-Than Data High Byte	69
ADC0GTL	0xC3	ADC0 Greater-Than Data Low Byte	69
ADC0LTH	0xC6	ADC0 Less-Than Data High Byte	70
ADC0LTL	0xC5	ADC0 Less-Than Data Low Byte	70
ADC0MX	0xBB	ADC0 Channel Select	64
ADC0TK	0xBA	ADC0 Tracking Mode Select	68
B	0xF0	B Register	89
CKCON	0x8E	Clock Control	188
CLKSEL	0xA9	Clock Select	143
CPT0CN	0x9B	Comparator0 Control	78
CPT0MD	0x9D	Comparator0 Mode Selection	80
CPT0MX	0x9F	Comparator0 MUX Selection	79
DPH	0x83	Data Pointer High	87
DPL	0x82	Data Pointer Low	87
EIE1	0xE6	Extended Interrupt Enable 1	102
EIP1	0xF6	Extended Interrupt Priority 1	103
FLKEY	0xB7	Flash Lock and Key	119
IE	0xA8	Interrupt Enable	100
IP	0xB8	Interrupt Priority	101
IT01CF	0xE4	INT0/INT1 Configuration	105
LINADDR	0x92	LIN indirect address pointer	172
LINCF	0x95	LIN master-slave and automatic baud rate selection	173
LINDATA	0x93	LIN indirect data buffer	172
OSCICL	0xB3	Internal Oscillator Calibration	138

Table 9.2. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Description	Page
OSCICN	0xB2	Internal Oscillator Control	137
OSCXCN	0xB1	External Oscillator Control	142
P0	0x80	Port 0 Latch	129
P0MASK	0xC7	Port 0 Mask	131
P0MAT	0xD7	Port 0 Match	131
P0MDIN	0xF1	Port 0 Input Mode Configuration	129
P0MDOUT	0xA4	Port 0 Output Mode Configuration	130
P0SKIP	0xD4	Port 0 Skip	130
P1	0x90	Port 1 Latch	132
P1MASK	0xBF	Port 1 Mask	134
P1MAT	0xCF	Port 1 Match	134
P1MDIN	0xF2	Port 1 Input Mode Configuration	132
P1MDOUT	0xA5	Port 1 Output Mode Configuration	133
P1SKIP	0xD5	Port 1 Skip	133
PCA0CN	0xD8	PCA Control	206
PCA0CPH0	0xFC	PCA Capture 0 High	209
PCA0CPH1	0xEA	PCA Capture 1 High	209
PCA0CPH2	0xEC	PCA Capture 2 High	209
PCA0CPL0	0xFB	PCA Capture 0 Low	209
PCA0CPL1	0xE9	PCA Capture 1 Low	209
PCA0CPL2	0xEB	PCA Capture 2 Low	209
PCA0CPM0	0xDA	PCA Module 0 Mode	208
PCA0CPM1	0xDB	PCA Module 1 Mode	208
PCA0CPM2	0xDC	PCA Module 2 Mode	208
PCA0H	0xFA	PCA Counter High	209
PCA0L	0xF9	PCA Counter Low	209
PCA0MD	0xD9	PCA Mode	207
PCON	0x87	Power Control	91
PSCTL	0x8F	Program Store R/W Control	119
PSW	0xD0	Program Status Word	88

11.1. Power-On Reset

During power-up, the device is held in a reset state and the $\overline{RST}$ pin is driven low until V_{DD} settles above V_{RST}. V_{DD} ramp time is defined as how fast V_{DD} ramps from 0 V to V_{RST}. An additional delay ($T_{PORDelay}$) occurs before the device is released from reset. The V_{RST} threshold and $T_{PORDelay}$ are specified in Table 2.8, “Reset Electrical Characteristics,” on page 32. Figure 11.2 plots the power-on and V_{DD} monitor reset timing.

Note: Please refer to Section “20.4. VDD Monitors and VDD Ramp Time” on page 211 for definition of V_{RST} and V_{DD} ramp time in older silicon revisions A and B.

On exit from a power-on reset, the PORSF flag (RSTSRC.1) is set by hardware to logic 1. When PORSF is set, all of the other reset flags in the RSTSRC Register are indeterminate (PORSF is cleared by all other resets). Since all resets cause program execution to begin at the same location (0x0000), software can read the PORSF flag to determine if a power-up was the cause of reset. The contents of internal data memory should be assumed to be undefined after a power-on reset. Both the V_{DD} monitors (VDDMON0 and VDDMON1) are enabled following a power-on reset.

Note: Please refer to Section “11.2.1. VDD Monitor Thresholds and Minimum VDD” on page 108 for recommendations related to minimum V_{DD}.

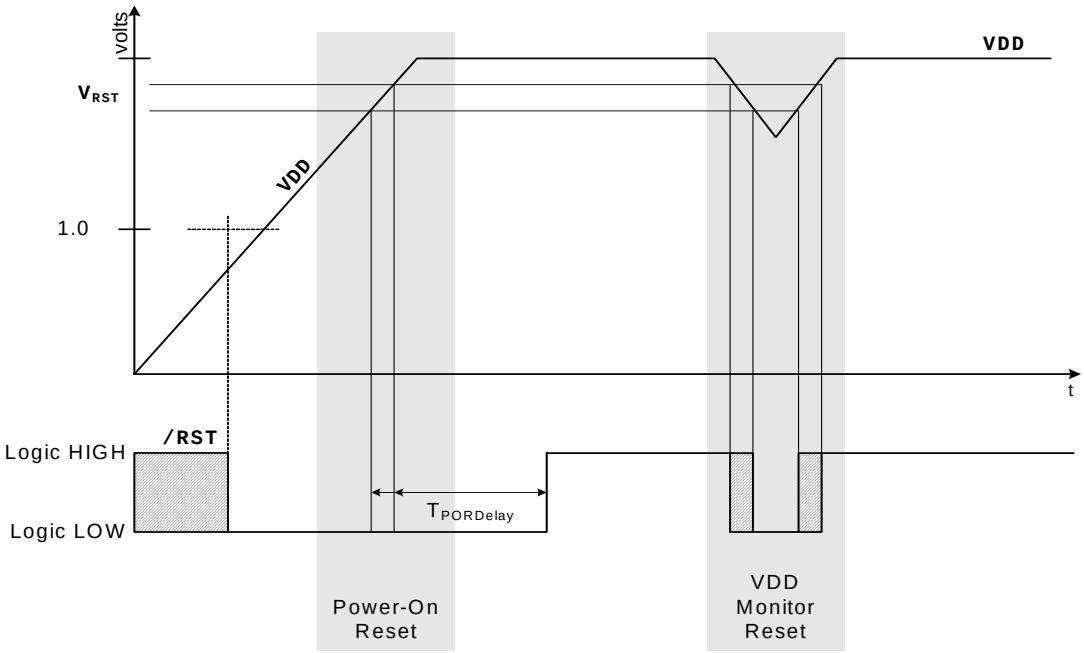


Figure 11.2. Power-On and V_{DD} Monitor Reset Timing

ramp or during a brownout condition even when V_{DD} is below the specified minimum of 2.0 V. There are two possible ways to handle this transitional period as described below:

If using the on-chip regulator (REG0) at the 2.6 V setting (default), it is recommended that user software set the VDDMON0 threshold to its high setting ($V_{RST-HIGH}$) as soon as possible after reset by setting the VDMLVL bit to 1 in SFR Definition 11.1 (VDDMON). In this typical configuration, no external hardware or additional software routines are necessary to monitor the V_{DD} level.

Note: Please refer to Section “20.5. VDD Monitor (VDDMON0) High Threshold Setting” on page 212 for important notes related to the VDD Monitor high threshold setting in older silicon revisions A and B.

If using the on-chip regulator (REG0) at the 2.1 V setting or if directly driving V_{DD} with REG0 disabled, the user system (software/hardware) should monitor V_{DD} at power-on and also during device operation. The two key parameters that can be affected when V_{DD} < 2.0 V are: internal oscillator frequency (Table 2.11 on page 34) and minimum ADC tracking time (Table 2.3 on page 28).

SFR Definition 11.1. VDDMON: V_{DD} Monitor Control

R/W	R	R/W	R	R	R	R	R	Reset Value
VDMEN	VDDSTAT	VDMLVL	VDM1EN	Reserved	Reserved	Reserved	Reserved	1v010000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xFF

Bit7: **VDMEN**: V_{DD} Monitor Enable (VDDMON0).
This bit turns the V_{DD} monitor circuit on/off. The V_{DD} Monitor cannot generate system resets until it is also selected as a reset source in register RSTSRC (SFR Definition 11.2). The V_{DD} Monitor can be allowed to stabilize before it is selected as a reset source. **Selecting the V_{DD} monitor as a reset source before it has stabilized may generate a system reset.** See Table 2.8 on page 32 for the minimum V_{DD} Monitor turn-on time.
0: V_{DD} Monitor Disabled.
1: V_{DD} Monitor Enabled (default).

Bit6: **VDDSTAT**: V_{DD} Status.
This bit indicates the current power supply status (V_{DD} Monitor output).
0: V_{DD} is at or below the V_{DD} Monitor (VDDMON0) Threshold.
1: V_{DD} is above the V_{DD} Monitor (VDDMON0) Threshold.

Bit5: **VDMLVL**: V_{DD} Level Select.
0: V_{DD} Monitor (VDDMON0) Threshold is set to $V_{RST-LOW}$ (default).
1: V_{DD} Monitor (VDDMON0) Threshold is set to $V_{RST-HIGH}$. This setting is **required** for any system that includes code that writes to and/or erases Flash.

Bit4: **VDM1EN***: Level-sensitive V_{DD} Monitor Enable (VDDMON1).
This bit turns the V_{DD} monitor circuit on/off. If turned on, it is also selected as a reset source, and can generate a system reset.
0: Level-sensitive VDD Monitor Disabled.
1: Level-sensitive VDD Monitor Enabled (default).

Bits3–0: **RESERVED**. Read = Variable. Write = don’t care.

***Note:** Available only on the C8051F52x-C/F53x-C devices

SFR Definition 12.1. PSCTL: Program Store R/W Control

R	R	R	R	R	R	R/W	R/W	Reset Value
—	—	—	—	—	—	PSEE	PSWE	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x8F

Bits7–2: **UNUSED**: Read = 000000b, Write = don't care.

Bit1: **PSEE**: Program Store Erase Enable
Setting this bit (in combination with PSWE) allows an entire page of Flash program memory to be erased. If this bit is logic 1 and Flash writes are enabled (PSWE is logic 1), a write to Flash memory using the MOVX instruction will erase the entire page that contains the location addressed by the MOVX instruction. The value of the data byte written does not matter.
0: Flash program memory erasure disabled.
1: Flash program memory erasure enabled.

Bit0: **PSWE**: Program Store Write Enable
Setting this bit allows writing a byte of data to the Flash program memory using the MOVX write instruction. The Flash location should be erased before writing data.
0: Writes to Flash program memory disabled.
1: Writes to Flash program memory enabled; the MOVX write instruction targets Flash memory.

Note: See Section "12.1. Programming The Flash Memory" on page 113 for minimum V_{DD} and temperature requirements for flash erase and write operations.

SFR Definition 12.2. FLKEY: Flash Lock and Key

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xB7

Bits7–0: **FLKEY**: Flash Lock and Key Register
Write:
This register provides a lock and key function for Flash erasures and writes. Flash writes and erases are enabled by writing 0xA5 followed by 0xF1 to the FLKEY register. Flash writes and erases are automatically disabled after the next write or erase is complete. If any writes to FLKEY are performed incorrectly, or if a Flash write or erase operation is attempted while these operations are disabled, the Flash will be permanently locked from writes or erasures until the next device reset. If an application never writes to Flash, it can intentionally lock the Flash by writing a non-0xA5 value to FLKEY from software.
Read:
When read, bits 1–0 indicate the current Flash lock state.
00: Flash is write/erase locked.
01: The first key code has been written (0xA5).
10: Flash is unlocked (writes/erases allowed).
11: Flash writes/erases disabled until the next reset.

13. Port Input/Output

Digital and analog resources are available through up to 16 I/O pins. Port pins are organized as two or one byte-wide Ports. Each of the Port pins can be defined as general-purpose I/O (GPIO) or analog input/output; Port pins P0.0 - P2.7 can be assigned to one of the internal digital resources as shown in Figure 13.3. The designer has complete control over which functions are assigned, limited only by the number of physical I/O pins. This resource assignment flexibility is achieved through the use of a Priority Crossbar Decoder. Note that the state of a Port I/O pin can always be read in the corresponding Port latch, regardless of the Crossbar settings.

The Crossbar assigns the selected internal digital resources to the I/O pins based on the peripheral priority order of the Priority Decoder (Figure 13.3 and Figure 13.4). The registers XBR0 and XBR1, defined in SFR Definition 13.1 and SFR Definition 13.2, are used to select internal digital functions.

Port I/O pins are 5.25 V tolerant over the operating range of V_{REGIN}. Figure 13.2 shows the Port cell circuit. The Port I/O cells are configured as either push-pull or open-drain in the Port Output Mode registers (PnMDOUT, where n = 0,1). Complete Electrical Specifications for Port I/O are given in Table 2.10 on page 33.

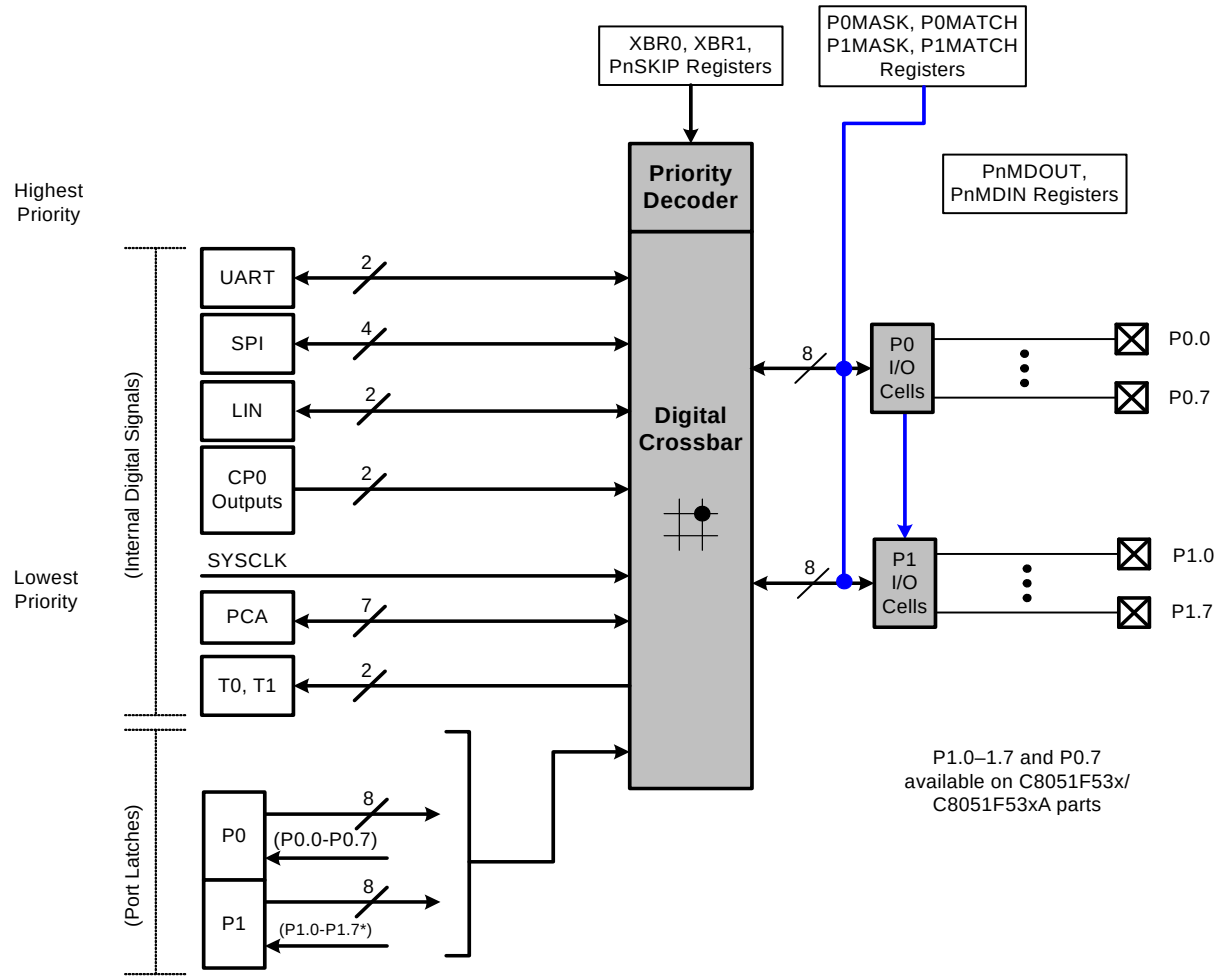
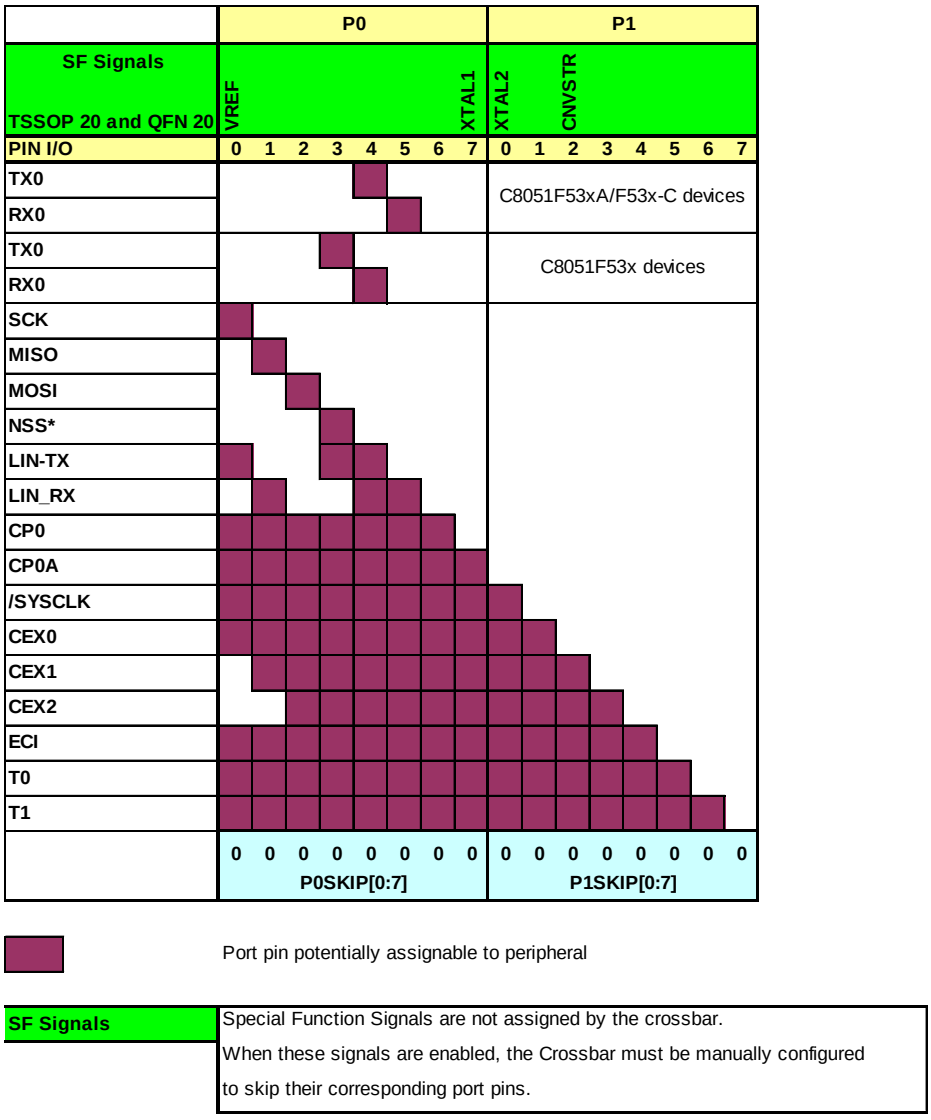


Figure 13.1. Port I/O Functional Block Diagram

13.1. Priority Crossbar Decoder

The Priority Crossbar Decoder (Figure 13.3) assigns a priority to each I/O function, starting at the top with UART0. When a digital resource is selected, the least-significant unassigned Port pin is assigned to that resource (excluding UART0, which will be assigned to pins P0.4 and P0.5). If a Port pin is assigned, the Crossbar skips that pin when assigning the next selected resource. Additionally, the Crossbar will skip Port pins whose associated bits in the PnSKIP registers are set. The PnSKIP registers allow software to skip Port pins that are to be used for analog input, dedicated functions, or GPIO.



Note: 4-Wire SPI Only.

Figure 13.3. Crossbar Priority Decoder with No Pins Skipped (TSSOP 20 and QFN 20)

Important Note on Crossbar Configuration: If a Port pin is claimed by a peripheral without use of the Crossbar, its corresponding PnSKIP bit should be set. This applies to P1.0 and/or P0.7 (F53x/F53xA) or P0.2 and/or P0.3 (F52x/F52xA) for the external oscillator, P0.0 for V_{REF}, P1.2 (F53x/F53xA) or P0.5

SFR Definition 14.1. OSCICN: Internal Oscillator Control

R/W	R/W	R/W	R	R	R/W	R/W	R/W	Reset Value
IOSCEN1	IOSCEN0	SUSPEND	IFRDY	—	IFCN2	IFCN1	IFCN0	11000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xB2

Bits7–6: **IOSCEN[1:0]**: Internal Oscillator Enable Bits.
00: Oscillator Disabled.
01: Reserved.
10: Reserved.
11: Oscillator Enabled in Normal Mode and Disabled in Suspend Mode.

Bit5: **SUSPEND**: Internal Oscillator Suspend Enable Bit.
Setting this bit to logic 1 places the internal oscillator in SUSPEND mode. The internal oscillator resumes operation when one of the SUSPEND mode awakening events occur.

Bit4: **IFRDY**: Internal Oscillator Frequency Ready Flag.
0: Internal Oscillator is not running at programmed frequency.
1: Internal Oscillator is running at programmed frequency.

Bit3: **UNUSED**. Read = 0b, Write = don't care.

Bits2–0: **IFCN2–0**: Internal Oscillator Frequency Control Bits.
000: SYSCLK derived from Internal Oscillator divided by 128 (default).
001: SYSCLK derived from Internal Oscillator divided by 64.
010: SYSCLK derived from Internal Oscillator divided by 32.
011: SYSCLK derived from Internal Oscillator divided by 16.
100: SYSCLK derived from Internal Oscillator divided by 8.
101: SYSCLK derived from Internal Oscillator divided by 4.
110: SYSCLK derived from Internal Oscillator divided by 2.
111: SYSCLK derived from Internal Oscillator divided by 1.

15.2.2. 9-Bit UART

9-bit UART mode uses a total of eleven bits per data byte: a start bit, 8 data bits (LSB first), a programmable ninth data bit, and a stop bit. The state of the ninth transmit data bit is determined by the value in TB80 (SCON0.3), which is assigned by user software. It can be assigned the value of the parity flag (bit P in register PSW) for error detection, or used in multiprocessor communications. On receive, the ninth data bit goes into RB80 (SCON0.2) and the stop bit is ignored.

Data transmission begins when an instruction writes a data byte to the SBUF0 register. The TI0 Transmit Interrupt Flag (SCON0.1) is set at the end of the transmission (the beginning of the stop-bit time). Data reception can begin any time after the REN0 Receive Enable bit (SCON0.4) is set to 1. After the stop bit is received, the data byte will be loaded into the SBUF0 receive register if the following conditions are met: (1) RI0 must be logic 0, and (2) if MCE0 is logic 1, the 9th bit must be logic 1 (when MCE0 is logic 0, the state of the ninth data bit is unimportant). If these conditions are met, the eight bits of data are stored in SBUF0, the ninth bit is stored in RB80, and the RI0 flag is set to 1. If the above conditions are not met, SBUF0 and RB80 will not be loaded and the RI0 flag will not be set to 1. A UART0 interrupt will occur if enabled when either TI0 or RI0 is set to 1.

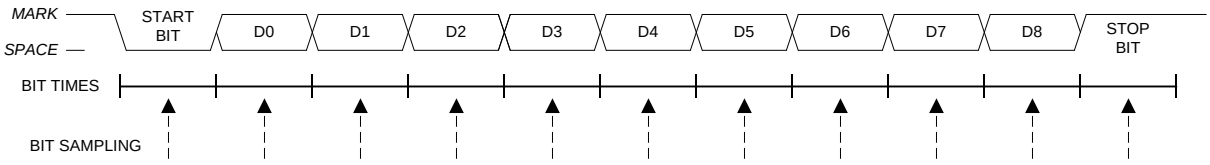


Figure 15.5. 9-Bit UART Timing Diagram

16.1. Signal Descriptions

The four signals used by SPI0 (MOSI, MISO, SCK, NSS) are described below.

16.1.1. Master Out, Slave In (MOSI)

The master-out, slave-in (MOSI) signal is an output from a master device and an input to slave devices. It is used to serially transfer data from the master to the slave. This signal is an output when SPI0 is operating as a master and an input when SPI0 is operating as a slave. Data is transferred most-significant bit first. When configured as a master, MOSI is driven by the MSB of the shift register in both 3- and 4-wire mode.

16.1.2. Master In, Slave Out (MISO)

The master-in, slave-out (MISO) signal is an output from a slave device and an input to the master device. It is used to serially transfer data from the slave to the master. This signal is an input when SPI0 is operating as a master and an output when SPI0 is operating as a slave. Data is transferred most-significant bit first. The MISO pin is placed in a high-impedance state when the SPI module is disabled and when the SPI operates in 4-wire mode as a slave that is not selected. When acting as a slave in 3-wire mode, MISO is always driven by the MSB of the shift register.

16.1.3. Serial Clock (SCK)

The serial clock (SCK) signal is an output from the master device and an input to slave devices. It is used to synchronize the transfer of data between the master and slave on the MOSI and MISO lines. SPI0 generates this signal when operating as a master. The SCK signal is ignored by a SPI slave when the slave is not selected (NSS = 1) in 4-wire slave mode.

16.1.4. Slave Select (NSS)

The function of the slave-select (NSS) signal is dependent on the setting of the NSSMD1 and NSSMD0 bits in the SPI0CN register. There are three possible modes that can be selected with these bits:

1. NSSMD[1:0] = 00: 3-Wire Master or 3-Wire Slave Mode: SPI0 operates in 3-wire mode, and NSS is disabled. When operating as a slave device, SPI0 is always selected in 3-wire mode. Since no select signal is present, SPI0 must be the only slave on the bus in 3-wire mode. This is intended for point-to-point communication between a master and one slave.
2. NSSMD[1:0] = 01: 4-Wire Slave or Multi-Master Mode: SPI0 operates in 4-wire mode, and NSS is enabled as an input. When operating as a slave, NSS selects the SPI0 device. When operating as a master, a 1-to-0 transition of the NSS signal disables the master function of SPI0 so that multiple master devices can be used on the same SPI bus.
3. NSSMD[1:0] = 1x: 4-Wire Master Mode: SPI0 operates in 4-wire mode, and NSS is enabled as an output. The setting of NSSMD0 determines what logic level the NSS pin will output. This configuration should only be used when operating SPI0 as a master device.

See Figure 16.2, Figure 16.3, and Figure 16.4 for typical connection diagrams of the various operational modes. **Note that the setting of NSSMD bits affects the pinout of the device.** When in 3-wire master or 3-wire slave mode, the NSS pin will not be mapped by the crossbar. In all other modes, the NSS signal will be mapped to a pin on the device. See Section “13. Port Input/Output” on page 120 for general purpose port I/O and crossbar information.

19.2.2. Software Timer (Compare) Mode

In Software Timer mode, the PCA counter/timer value is compared to the module's 16-bit capture/compare register (PCA0CPHn and PCA0CPLn). When a match occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1 and an interrupt request is generated if CCF interrupts are enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Setting the ECOMn and MATn bits in the PCA0CPMn register enables Software Timer mode.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

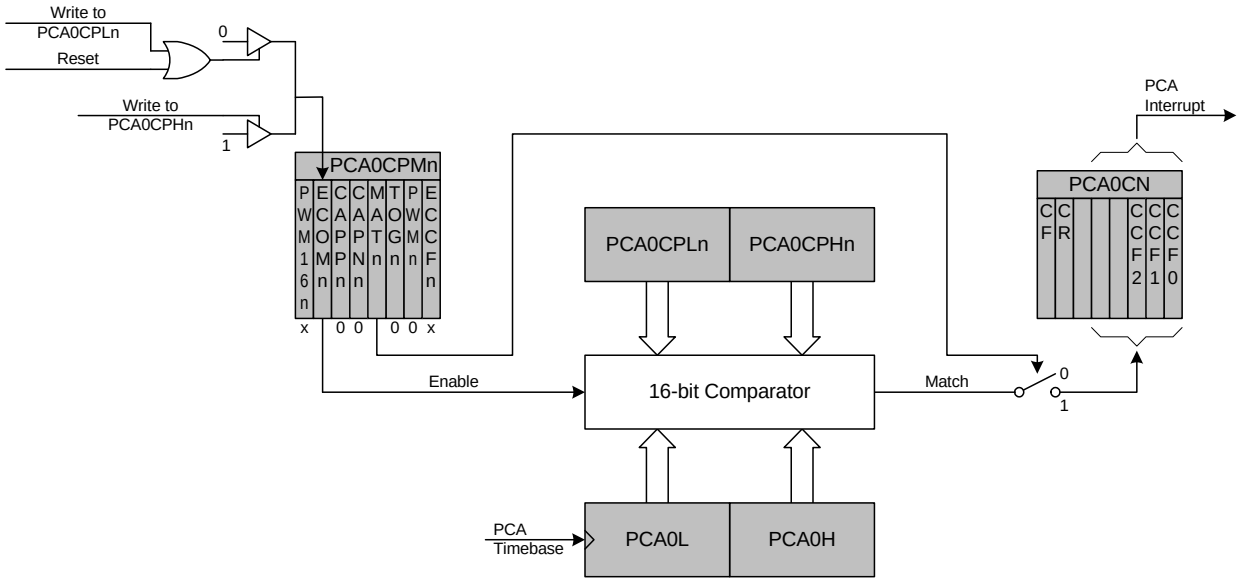


Figure 19.5. PCA Software Timer Mode Diagram

20.8. UART Pins

The location of the pins used by the serial UART interface differs between the silicon revisions of C8051F52x/52xA/F53x/F53xA devices.

On Revision A devices, the TX and RX pins used by the UART interface are mapped to the P0.3 (TX) and P0.4 (RX) pins. Beginning with Revision B devices, the TX and RX pins used by the UART interface are mapped to the P0.4 (TX) and P0.5 (RX) pins.

Important Note: On Revision B and newer devices, the UART pins must be skipped if the UART is enabled in order for peripherals to appear on port pins beyond the UART on the crossbar. For example, with the SPI and UART enabled on the crossbar with the SPI on P1.0-P1.3, the UART pins must be skipped using P0SKIP for the SPI pins to appear correctly.

20.9. LIN

The LIN peripheral behavior differs between the silicon revisions of C8051F52x/52xA/F53x/F53xA devices. The differences are:

20.9.1. Stop Bit Check

On Revision A devices, the stop bits of the fields in the LIN frame are not checked and no error is generated if the stop bits could not be sent or received correctly. On Revision B and Revision C devices, the stop bits are checked, and an error will be generated if the stop bit was not sent or received correctly.

20.9.2. Synch Break and Synch Field Length Check

On Revision A devices, the check of sync field length versus sync break length is incorrect. On Revision B and Revision C devices, the sync break length must be larger than 10 bit times (of the measured bit time) to enable the synchronization.

Revision 1.2 to 1.3

- Updated “System Overview” on page 13 with a voltage range specification for the internal oscillator.
- Updated Table 2.11 on page 34 with new conditions for the internal oscillator accuracy. The internal oscillator accuracy is dependent on the operating voltage range.
- Updated Section 2 to remove the internal oscillator curve across temperature diagram.
- Updated Figure “4.5 12-Bit ADC Burst Mode Example with Repeat Count Set to 4” on page 58 with new timing diagram when using CNVSTR pin.
- Updated SFR Definition 5.1 (REF0CN) with oscillator suspend requirement for ZTCEN.
- Updated SFR Definition 6.1 (REG0CN) with a new definition for Bit 6. The bit 6 reset value is 1b and must be written to 1b.
- Updated Section “8.3.3. Suspend Mode” on page 90 with note regarding ZTCEN.
- Updated Section “17. LIN (C8051F520/0A/3/3A/6/6A and C8051F530/0A/3/3A/6/6A)” on page 164 with a voltage range specification for the internal oscillator.

Revision 1.3 to 1.4

- Added ‘AEC-Q100’ qualification information on page 1.
- Changed page headers throughout the document from ‘C8051F52x/F52xA/F53x/F53xA’ to ‘C8051F52x/53x’.
- Updated supply voltage to "2.0 to 5.25 V" on page 1 and in Section 1 on page 13.
- Corrected reference to development kit (C8051F530DK) in Section “1.2.4. On-Chip Debug Circuitry” on page 18.
- Updated minimum Supply Input Voltage (V_{REGIN}) for C8051F52x-C/F53x-C devices in Table 2.2 on page 26 and Table 2.6 on page 30.
- Updated digital supply current (I_{DD} and Idle I_{DD}) typical values for condition ‘Clock = 25 MHz’ in Table 2.2 on page 26.
- Updated I_{DD} Frequency Sensitivity and Idle I_{DD} Frequency Sensitivity values in Table 2.2 on page 26; removed Figure 2.1 and Figure 2.2 that used to provide the same frequency sensitivity slopes. Also removed IDD Supply Sensitivity and Idle IDD Supply Sensitivity typical values.
- Added Digital Supply Current (Stop or Suspend Mode) values at multiple temperatures Table 2.2 on page 26.
- Added a note in Table 2.3, “ADC0 Electrical Characteristics,” on page 28 with reference to Section “4.4. Selectable Gain” on page 60; also added note to indicate that additional tracking time may be necessary if VDD is less than the minimum specified VDD.
- Split off temperature sensor specifications from Table 2.3 into a separate table Table 2.4; Updated temperature sensor gain and added supply current values.
- Added temperature condition for Bias Current specification in Table 2.6 on page 30.
- Updated Comparator Input Offset Voltage values in Table 2.7 on page 31.
- Updated VDD Monitor (VDDMON0) Low Threshold ($V_{RST-LOW}$) minimum value for C8051F52xA/F52x-C/F53xA/F53x-C devices in Table 2.8 on page 32.
- Updated VDD Monitor (VDDMON0) supply current values in Table 2.8 on page 32.
- Added specifications for the new level-sensitive VDD monitor (VDDMON1) to Table 2.8, “Reset Electrical Characteristics,” on page 32 and also added notes to clarify the applicable V_{RST} theshold level.
- Added note in Table 2.9, “Flash Electrical Characteristics,” on page 33 to describe the minimum flash programming temperature for –I (Industrial Grade) devices; Also added the same note and references to it in Section “12.1. Programming The Flash Memory” on page 113, Section “12.3. Non-volatile Data Storage” on page 117, and in SFR Definition 12.1 (PSCTL).