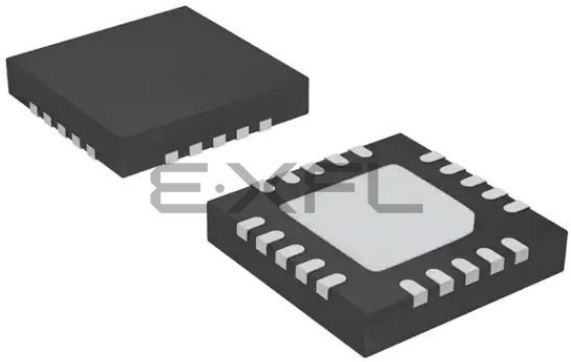

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f534a-im

Table 2.11. Internal Oscillator Electrical Characteristics

V_{DD} = 1.8 to 2.75 V, –40 to +125 °C unless otherwise specified; Using factory-calibrated settings.

Parameter	Conditions	Min	Typ	Max	Units
Oscillator Frequency[1]	IFCN = 111b VDD ≥ VREGMIN[2]	24.5 – 0.5%	24.5[3]	24.5 + 0.5%	MHz
	IFCN = 111b VDD < VREGMIN[2]	24.5 – 1.0%	24.5[3]	24.5 + 1.0%	
Oscillator Supply Current (from V_{DD})	Oscillator On OSCICN[7:6] = 11b	—	800	1100	µA
	Oscillator Suspend OSCICN[7:6] = 00b ZTCEN = 1				
	T = 25 °C	—	67	—	µA
	T = 85 °C	—	77	—	µA
	T = 125 °C	—	117	300	µA
	Oscillator Suspend OSCICN[7:6] = 00b ZTCEN = 0				
	T = 25 °C	—	2	—	µA
	T = 85 °C	—	3	—	µA
	T = 125 °C	—	50	—	µA
Wake-Up Time From Suspend	OSCICN[7:6] = 00b ZTCEN = 0[4]	—	—	1	µs
	OSCICN[7:6] = 00b ZTCEN = 1	—	5	—	Instruction Cycles
Power Supply Sensitivity	Constant Temperature	—	0.10	—	%/V
Temperature Sensitivity[5]	Constant Supply				
	TC_1	—	5.0	—	ppm/°C
	TC_2	—	–0.65	—	ppm/°C^2

Notes:

1. See Section “11.2.1. VDD Monitor Thresholds and Minimum VDD” on page 108 for minimum V_{DD} requirements.
2. VREGMIN is the minimum output of the voltage regulator for its low setting (REG0CN: REG0MD = 0b). See Table 2.6, “Voltage Regulator Electrical Specifications,” on page 30.
3. This is the average frequency across the operating temperature range.
4. See “20.7. Internal Oscillator Suspend Mode” on page 212 for ZTCEN setting in older silicon revisions.
5. Use temperature coefficients TC_1 and TC_2 to calculate the new internal oscillator frequency using the following equation:

$$f(T) = f0 \times (1 + TC_1 \times (T - T0) + TC_2 \times (T - T0)^2)$$

where f0 is the internal oscillator frequency at 25 °C and T0 is 25 °C.

4.3.4. Burst Mode

Burst Mode is a power saving feature that allows ADC0 to remain in a very low power state between conversions. When Burst Mode is enabled, ADC0 wakes from a very low power state, accumulates 1, 4, 8, or 16 samples using an internal Burst Mode Oscillator, then re-enters a very low power state. Since the Burst Mode clock is independent of the system clock, ADC0 can perform multiple conversions then enter a very low power state within a single system clock cycle, even if the system clock is slow (e.g. 32.768 kHz), or suspended.

Burst Mode is enabled by setting BURSTEN to logic 1. When in Burst Mode, AD0EN controls the ADC0 idle power state (i.e., the state ADC0 enters when not tracking or performing conversions). If AD0EN is set to logic 0, ADC0 is powered down after each burst. If AD0EN is set to logic 1, ADC0 remains enabled after each burst. On each convert start signal, ADC0 is awakened from its Idle Power State. If ADC0 is powered down, it will automatically power up and wait the programmable Power-Up Time controlled by the AD0PWR bits. Otherwise, ADC0 will start tracking and converting immediately. Figure 4.5 shows an example of Burst Mode Operation with a slow system clock and a repeat count of 4.

Important Note: When Burst Mode is enabled, only Post-Tracking and Dual-Tracking modes can be used.

When Burst Mode is enabled, a single convert start will initiate a number of conversions equal to the repeat count. When Burst Mode is disabled, a convert start is required to initiate each conversion. In both modes, the ADC0 End of Conversion Interrupt Flag (AD0INT) will be set after “repeat count” conversions have been accumulated. Similarly, the Window Comparator will not compare the result to the greater-than and less-than registers until “repeat count” conversions have been accumulated.

Note: When using Burst Mode, care must be taken to issue a convert start signal no faster than once every four SYSCLK periods. This includes external convert start signals.

SFR Definition 4.4. ADC0MX: ADC0 Channel Select

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	AD0MX					00011111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xBB

Bits7–5: **UNUSED**. Read = 000b; Write = don't care.
Bits4–0: **AD0MX4–0**: AMUX0 Positive Input Selection

AD0MX4–0	ADC0 Input Channel
00000	P0.0
00001	P0.1
00010	P0.2
00011	P0.3
00100	P0.4
00101	P0.5
00110	P0.6*
00111	P0.7*
01000	P1.0*
01001	P1.1*
01010	P1.2*
01011	P1.3*
01100	P1.4*
01101	P1.5*
01110	P1.6*
01111	P1.7*
11000	Temp Sensor
11001	V_{DD}
11010 - 11111	GND

Note: Only applies to C8051F53x/C8051F53xA parts.

SFR Definition 4.8. ADC0CN: ADC0 Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
AD0EN	BURSTEN	AD0INT	AD0BUSY	AD0WINT	AD0LJST	AD0CM1	AD0CM0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
							(bit addressable)	0xE8

Bit7: **AD0EN**: ADC0 Enable Bit.
0: ADC0 Disabled. ADC0 is in low-power shutdown.
1: ADC0 Enabled. ADC0 is active and ready for data conversions.

Bit6: **BURSTEN**: ADC0 Burst Mode Enable Bit.
0: ADC0 Burst Mode Disabled.
1: ADC0 Burst Mode Enabled.

Bit5: **AD0INT**: ADC0 Conversion Complete Interrupt Flag.
0: ADC0 has not completed a data conversion since the last time AD0INT was cleared.
1: ADC0 has completed a data conversion.

Bit4: **AD0BUSY**: ADC0 Busy Bit.
Read:
0: ADC0 conversion is complete or a conversion is not currently in progress. AD0INT is set to logic 1 on the falling edge of AD0BUSY.
1: ADC0 conversion is in progress.
Write:
0: No Effect.
1: Initiates ADC0 Conversion if AD0CM1–0 = 00b

Bit3: **AD0WINT**: ADC0 Window Compare Interrupt Flag.
This bit must be cleared by software.
0: ADC0 Window Comparison Data match has not occurred since this flag was last cleared.
1: ADC0 Window Comparison Data match has occurred.

Bit2: **AD0LJST**: ADC0 Left Justify Select
0: Data in ADC0H:ADC0L registers is right justified.
1: Data in ADC0H:ADC0L registers is left justified. This option should not be used with a repeat count greater than 1 (when AD0RPT1–0 is 01b, 10b, or 11b).

Bits1–0: **AD0CM1–0**: ADC0 Start of Conversion Mode Select.
00: ADC0 conversion initiated on every write of 1 to AD0BUSY.
01: ADC0 conversion initiated on overflow of Timer 1.
10: ADC0 conversion initiated on rising edge of external CNVSTR.
11: ADC0 conversion initiated on overflow of Timer 2.

Important Note About the V_{REF} Pin: Port pin P0.0 is used as the external V_{REF} input and as an output for the internal V_{REF}. When using either an external voltage reference or the internal reference circuitry, P0.0 should be configured as an analog pin, and skipped by the Digital Crossbar. To configure P0.0 as an analog pin, clear Bit 0 in register P0MDIN to 0. To configure the Crossbar to skip P0.0, set Bit 0 in register P0SKIP to 1. Refer to Section "13. Port Input/Output" on page 120 for complete Port I/O configuration details.

The TEMPE bit in register REF0CN enables/disables the temperature sensor. While disabled, the temperature sensor defaults to a high impedance state and any ADC0 measurements performed on the sensor result in meaningless data.

SFR Definition 5.1. REF0CN: Reference Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
Reserved	Reserved	ZTCEN	REFLV	REFSL	TEMPE	BIASE	REFBE	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xD1

Bits7–6: **RESERVED**. Read = 00b. Must write 00b.

Bit5: **ZTCEN**: Zero-TempCo Bias Enable Bit*****.
0: ZeroTC Bias Generator automatically enabled when needed.
1: ZeroTC Bias Generator forced on.

Bit4: **REFLV**: Voltage Reference Output Level Select.
This bit selects the output voltage level for the internal voltage reference.
0: Internal voltage reference set to 1.5 V.
1: Internal voltage reference set to 2.2 V.

Bit3: **REFSL**: Voltage Reference Select.
This bit selects the source for the internal voltage reference.
0: V_{REF} pin used as voltage reference.
1: V_{DD} used as voltage reference.

Bit2: **TEMPE**: Temperature Sensor Enable Bit.
0: Internal Temperature Sensor off.
1: Internal Temperature Sensor on.

Bit1: **BIASE**: Internal Analog Bias Generator Enable Bit.
0: Internal Analog Bias Generator automatically enabled when needed.
1: Internal Analog Bias Generator on.

Bit0: **REFBE**: Internal Reference Buffer Enable Bit.
0: Internal Reference Buffer disabled.
1: Internal Reference Buffer enabled. Internal voltage reference driven on the V_{REF} pin.

*****Note: See Section "20.7. Internal Oscillator Suspend Mode" on page 212 for a note related to the ZTCEN bit in older silicon revisions.

SFR Definition 6.1. REG0CN: Regulator Control

R/W	R/W	R	R/W	R	R	R	R	Reset Value
REGDIS	Reserved	—	REG0MD	—	—	—	DROPOUT	01010000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xC9

Bit7: **REGDIS**: Voltage Regulator Disable Bit.
This bit disables/enables the Voltage Regulator.
0: Voltage Regulator Enabled.
1: Voltage Regulator Disabled.
Bit6: **RESERVED**. Read = 1b. Must write 1b.
Bit5: **UNUSED**. Read = 0b. Write = don't care.
Bit4: **REG0MD**: Voltage Regulator Mode Select Bit.
This bit selects the Voltage Regulator output voltage.
0: Voltage Regulator output is 2.1 V.
1: Voltage Regulator output is 2.6 V (default).
Bits3–1: **UNUSED**. Read = 000b. Write = don't care.
Bit0: **DROPOUT**: Voltage Regulator Dropout Indicator Bit.
0: Voltage Regulator is not in dropout.
1: Voltage Regulator is in or near dropout.

SFR Definition 8.4. PSW: Program Status Word

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	Reset Value
CY	AC	F0	RS1	RS0	OV	F1	PARITY	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0xD0

Bit7: **CY**: Carry Flag.
This bit is set when the last arithmetic operation resulted in a carry (addition) or a borrow (subtraction). It is cleared to 0 by all other arithmetic operations.

Bit6: **AC**: Auxiliary Carry Flag
This bit is set when the last arithmetic operation resulted in a carry into (addition) or a borrow from (subtraction) the high order nibble. It is cleared to 0 by all other arithmetic operations.

Bit5: **F0**: User Flag 0.
This is a bit-addressable, general purpose flag for use under software control.

Bits4–3: **RS1–RS0**: Register Bank Select.
These bits select which register bank is used during register accesses.

RS1	RS0	Register Bank	Address
0	0	0	0x00–0x07
0	1	1	0x08–0x0F
1	0	2	0x10–0x17
1	1	3	0x18–0x1F

Bit2: **OV**: Overflow Flag.
This bit is set to 1 under the following circumstances:
- An ADD, ADDC, or SUBB instruction causes a sign-change overflow.
- A MUL instruction results in an overflow (result is greater than 255).
- A DIV instruction causes a divide-by-zero condition.

The OV bit is cleared to 0 by the ADD, ADDC, SUBB, MUL, and DIV instructions in all other cases.

Bit1: **F1**: User Flag 1.
This is a bit-addressable, general purpose flag for use under software control.

Bit0: **PARITY**: Parity Flag.
This bit is set to 1 if the sum of the eight bits in the accumulator is odd and cleared if the sum is even.

11.1. Power-On Reset

During power-up, the device is held in a reset state and the $\overline{RST}$ pin is driven low until V_{DD} settles above V_{RST}. V_{DD} ramp time is defined as how fast V_{DD} ramps from 0 V to V_{RST}. An additional delay ($T_{PORDelay}$) occurs before the device is released from reset. The V_{RST} threshold and $T_{PORDelay}$ are specified in Table 2.8, “Reset Electrical Characteristics,” on page 32. Figure 11.2 plots the power-on and V_{DD} monitor reset timing.

Note: Please refer to Section “20.4. VDD Monitors and VDD Ramp Time” on page 211 for definition of V_{RST} and V_{DD} ramp time in older silicon revisions A and B.

On exit from a power-on reset, the PORSF flag (RSTSRC.1) is set by hardware to logic 1. When PORSF is set, all of the other reset flags in the RSTSRC Register are indeterminate (PORSF is cleared by all other resets). Since all resets cause program execution to begin at the same location (0x0000), software can read the PORSF flag to determine if a power-up was the cause of reset. The contents of internal data memory should be assumed to be undefined after a power-on reset. Both the V_{DD} monitors (VDDMON0 and VDDMON1) are enabled following a power-on reset.

Note: Please refer to Section “11.2.1. VDD Monitor Thresholds and Minimum VDD” on page 108 for recommendations related to minimum V_{DD}.

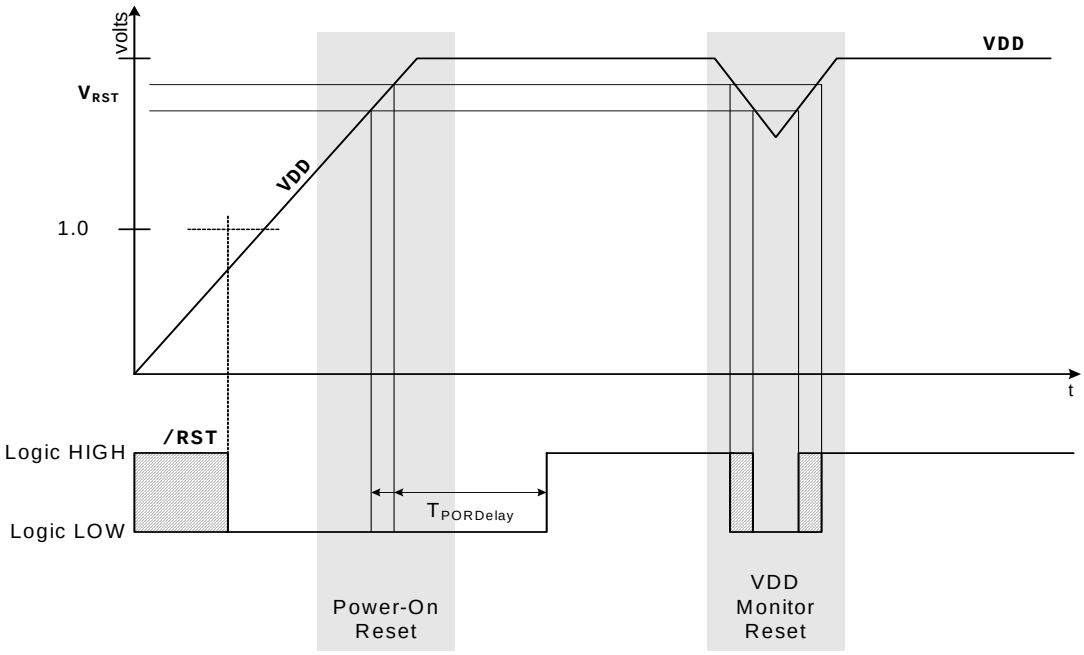


Figure 11.2. Power-On and V_{DD} Monitor Reset Timing

12.3. Non-volatile Data Storage

The Flash memory can be used for non-volatile data storage as well as program code. This allows data such as calibration coefficients to be calculated and stored at run time. Data is written using the MOVX write instruction and read using the MOVC instruction. Note: MOVX read instructions always target XRAM.

Note: See Section “12.1. Programming The Flash Memory” on page 113 for minimum V_{DD} and temperature requirements for flash erase and write operations.

12.4. Security Options

The CIP-51 provides security options to protect the Flash memory from inadvertent modification by software as well as to prevent the viewing of proprietary program code and constants. The Program Store Write Enable (bit PSWE in register PSCTL) and the Program Store Erase Enable (bit PSEE in register PSCTL) bits protect the Flash memory from accidental modification by software. PSWE must be explicitly set to 1 before software can modify the Flash memory; both PSWE and PSEE must be set to 1 before software can erase Flash memory. Additional security features prevent proprietary program code and data constants from being read or altered across the C2 interface.

A Security Lock Byte located at the last byte of Flash user space offers protection of the Flash program memory from access (reads, writes, or erases) by unprotected code or the C2 interface. The Flash security mechanism allows the user to lock *n* 512-byte Flash pages, starting at page 0 (addresses 0x0000 to 0x01FF), where *n* is the 1’s complement number represented by the Security Lock Byte. **Note that the page containing the Flash Security Lock Byte is unlocked when no other Flash pages are locked (all bits of the Lock Byte are 1) and locked when any other Flash pages are locked (any bit of the Lock Byte is 0).** See example below.

Security Lock Byte:	11111101b
1’s Complement:	00000010b
Flash pages locked:	3 (First two Flash pages + Lock Byte Page)
Addresses locked:	0x0000 to 0x03FF (first two Flash pages) 0x1C00 to 0x1DFF in ’F520/0A/1/1A and ’F530/0A/1/1A 0x0C00 to 0x0FFF in ’F523/3A/4/4A and ’F533/3A/4/4A and 0x0600 to 0x07FF in ’F526/6A/7/7A and ’F536/6A/7/7A

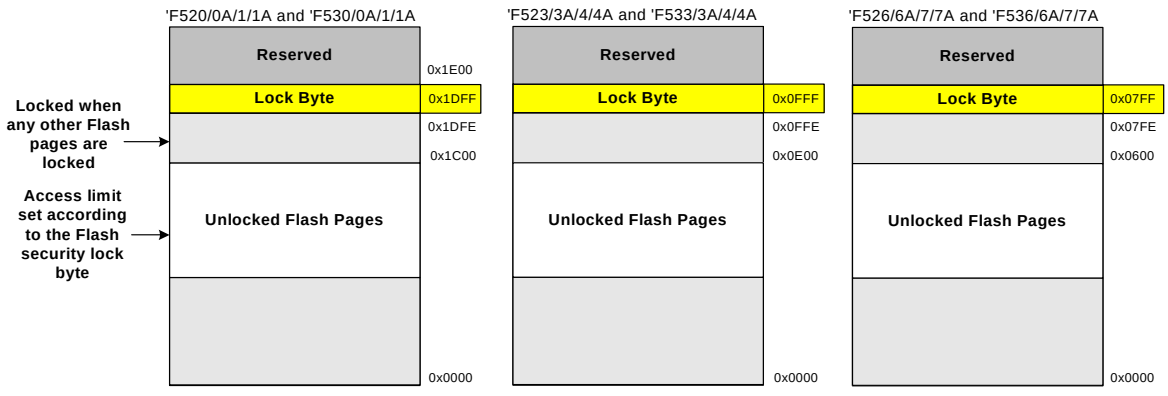


Figure 12.1. Flash Program Memory Map

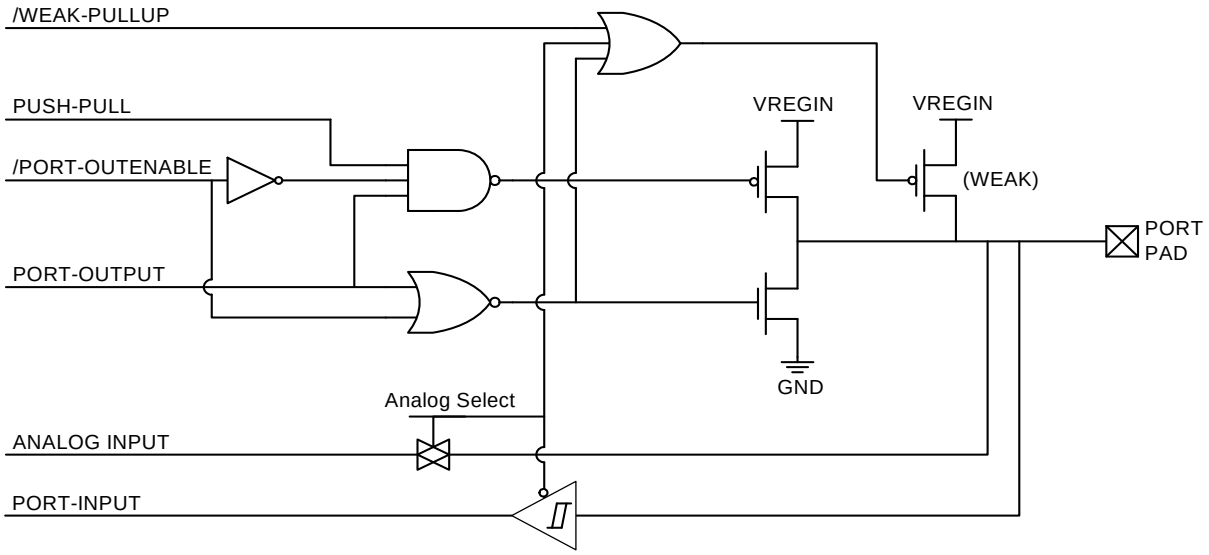


Figure 13.2. Port I/O Cell Block Diagram

SFR Definition 13.2. XBR1: Port I/O Crossbar Register 1

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
WEAKPUD	XBARE	T1E	T0E	ECIE	Reserved	PCA0ME		00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xE2

Bit7: **WEAKPUD**: Port I/O Weak Pullup Disable.
0: Weak Pullups enabled (except for Ports whose I/O are configured as analog input).
1: Weak Pullups disabled.
Bit6: **XBARE**: Crossbar Enable.
0: Crossbar disabled.
1: Crossbar enabled.
Bit5: **T1E**: T1 Enable
0: T1 unavailable at Port pin.
1: T1 routed to Port pin.
Bit4: **T0E**: T0 Enable
0: T0 unavailable at Port pin.
1: T0 routed to Port pin.
Bit3: **ECIE**: PCA0 External Counter Input Enable
0: ECI unavailable at Port pin.
1: ECI routed to Port pin.
Bit2: **Reserved**. Must Write 0b.
Bits1–0: **PCA0ME**: PCA Module I/O Enable Bits.
00: All PCA I/O unavailable at Port pins.
01: CEX0 routed to Port pin.
10: CEX0, CEX1 routed to Port pins.
11: CEX0, CEX1, CEX2 routed to Port pins.

13.3. General Purpose Port I/O

Port pins that remain unassigned by the Crossbar and are not used by analog peripherals can be used for general purpose I/O. Ports P0–P1 are accessed through corresponding special function registers (SFRs) that are both byte addressable and bit addressable. When writing to a Port, the value written to the SFR is latched to maintain the output data value at each pin. When reading, the logic levels of the Port's input pins are returned regardless of the XBRn settings (i.e., even when the pin is assigned to another signal by the Crossbar, the Port register can always read its corresponding Port I/O pin). The exception to this is the execution of the read-modify-write instructions that target a Port Latch register as the destination. The read-modify-write instructions when operating on a Port SFR are the following: ANL, ORL, XRL, JBC, CPL, INC, DEC, DJNZ and MOV, CLR or SETB, when the destination is an individual bit in a Port SFR. For these instructions, the value of the latch register (not the pin) is read, modified, and written back to the SFR.

SFR Definition 13.13. P0SKIP: Port0 Skip

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xD4

Bits7–0: **P1SKIP[7:0]**: Port1 Crossbar Skip Enable Bits.
These bits select Port pins to be skipped by the Crossbar Decoder. Port pins used as analog inputs (for ADC or Comparator) or used as special functions (V_{REF} input, external oscillator circuit, CNVSTR input) should be skipped by the Crossbar.
0: Corresponding P1.n pin is not skipped by the Crossbar.
1: Corresponding P1.n pin is skipped by the Crossbar.

SFR Definition 13.14. P1MAT: Port1 Match

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xCF

Bits7–0: **P1MAT[7:0]**: Port1 Match Value.
These bits control the value that unmasked P0 Port pins are compared against. A Port Match event is generated if (P1 & P1MASK) does not equal (P1MAT & P1MASK).

SFR Definition 13.15. P1MASK: Port1 Mask

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xBF

Bits7–0: **P1MASK[7:0]**: Port1 Mask Value.
These bits select which Port pins will be compared to the value stored in P1MAT.
0: Corresponding P1.n pin is ignored and cannot cause a Port Match event.
1: Corresponding P1.n pin is compared to the corresponding bit in P1MAT.

15.3. Multiprocessor Communications

9-Bit UART mode supports multiprocessor communication between a master processor and one or more slave processors by special use of the ninth data bit. When a master processor wants to transmit to one or more slaves, it first sends an address byte to select the target(s). An address byte differs from a data byte in that its ninth bit is logic 1; in a data byte, the ninth bit is always set to logic 0.

Setting the MCE0 bit (SCON0.5) of a slave processor configures its UART such that when a stop bit is received, the UART will generate an interrupt only if the ninth bit is logic 1 (RB80 = 1) signifying an address byte has been received. In the UART interrupt handler, software will compare the received address with the slave's own assigned 8-bit address. If the addresses match, the slave will clear its MCE0 bit to enable interrupts on the reception of the following data byte(s). Slaves that weren't addressed leave their MCE0 bits set and do not generate interrupts on the reception of the following data bytes, thereby ignoring the data. Once the entire message is received, the addressed slave resets its MCE0 bit to ignore all transmissions until it receives the next address byte.

Multiple addresses can be assigned to a single slave and/or a single address can be assigned to multiple slaves, thereby enabling "broadcast" transmissions to more than one slave simultaneously. The master processor can be configured to receive all transmissions or a protocol can be implemented such that the master/slave role is temporarily reversed to enable half-duplex transmission between the original master and slave(s).

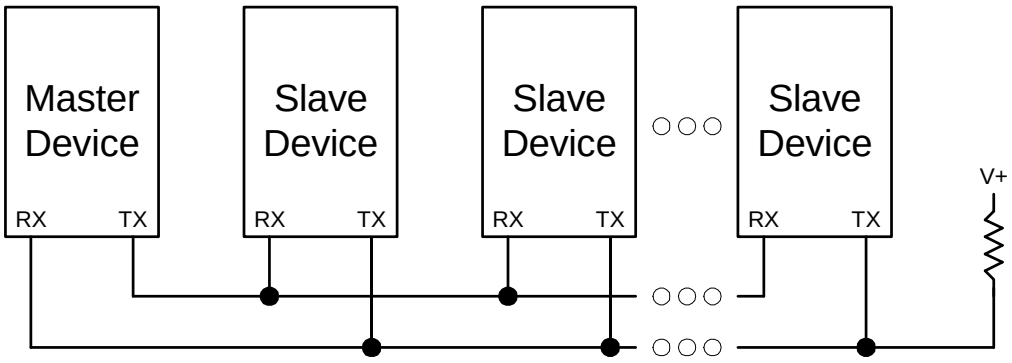


Figure 15.6. UART Multi-Processor Mode Interconnect Diagram

16. Enhanced Serial Peripheral Interface (SPI0)

The Serial Peripheral Interface (SPI0) provides access to a flexible, full-duplex synchronous serial bus. SPI0 can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select SPI0 in slave mode, or to disable Master Mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a chip-select output in master mode, or disabled for 3-wire operation. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

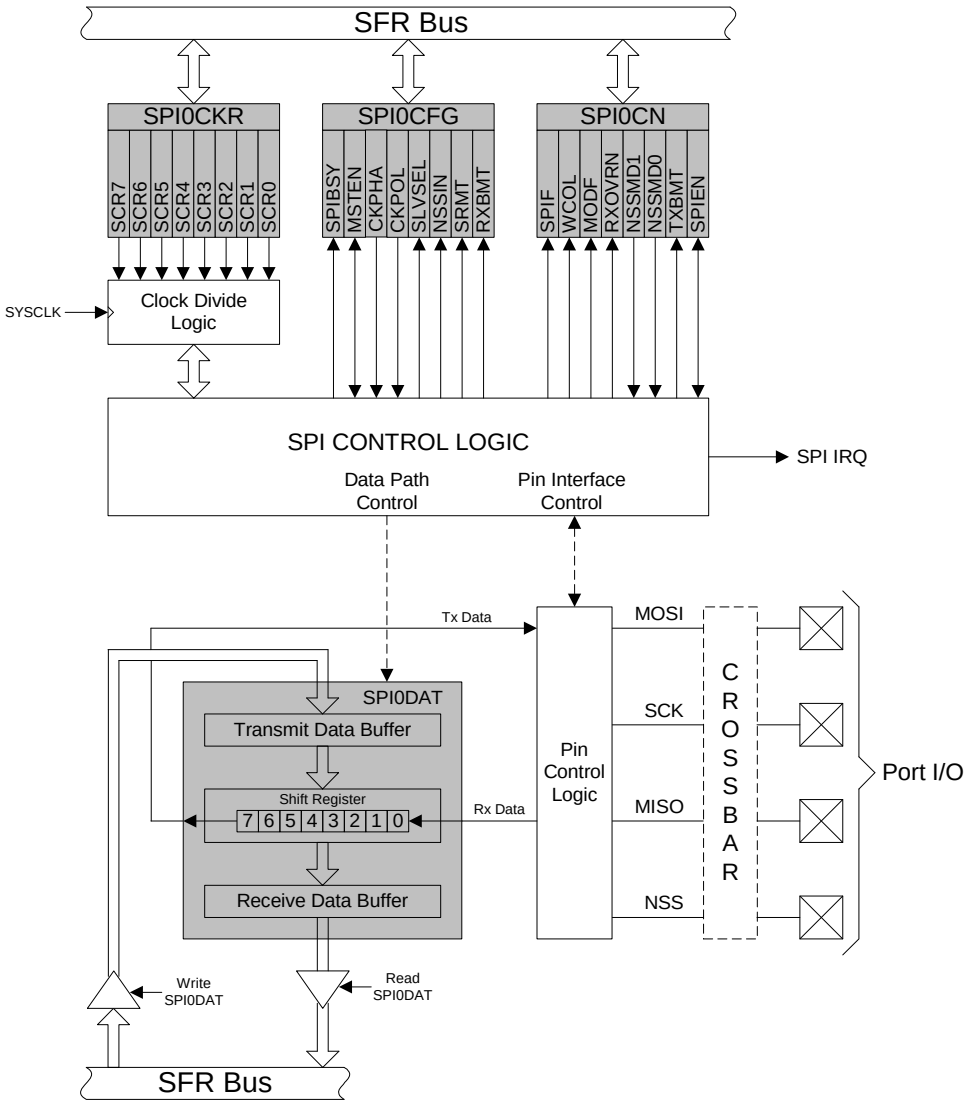


Figure 16.1. SPI Block Diagram

16.5. Serial Clock Timing

Four combinations of serial clock phase and polarity can be selected using the clock control bits in the SPI0 Configuration Register (SPI0CFG). The CKPHA bit (SPI0CFG.5) selects one of two clock phases (edge used to latch the data). The CKPOL bit (SPI0CFG.4) selects between a rising edge or a falling edge. Both master and slave devices must be configured to use the same clock phase and polarity. SPI0 should be disabled (by clearing the SPIEN bit, SPI0CN.0) when changing the clock phase or polarity. The clock and data line relationships are shown in Figure 16.5.

The SPI0 Clock Rate Register (SPI0CKR) as shown in SFR Definition 16.3 controls the master mode serial clock frequency. This register is ignored when operating in slave mode. When the SPI is configured as a master, the maximum data transfer rate (bits/sec) is one-half the system clock frequency or 12.5 MHz, whichever is slower. When the SPI is configured as a slave, the maximum data transfer rate (bits/sec) for full-duplex operation is 1/10 the system clock frequency, provided that the master issues SCK, NSS (in 4-wire slave mode), and the serial input data synchronously with the slave's system clock. If the master issues SCK, NSS, and the serial input data asynchronously, the maximum data transfer rate (bits/sec) must be less than 1/10 the system clock frequency. In the special case where the master only wants to transmit data to the slave and does not need to receive data from the slave (i.e. half-duplex operation), the SPI slave can receive data at a maximum data transfer rate (bits/sec) of 1/4 the system clock frequency. This is provided that the master issues SCK, NSS, and the serial input data synchronously with the slave's system clock.

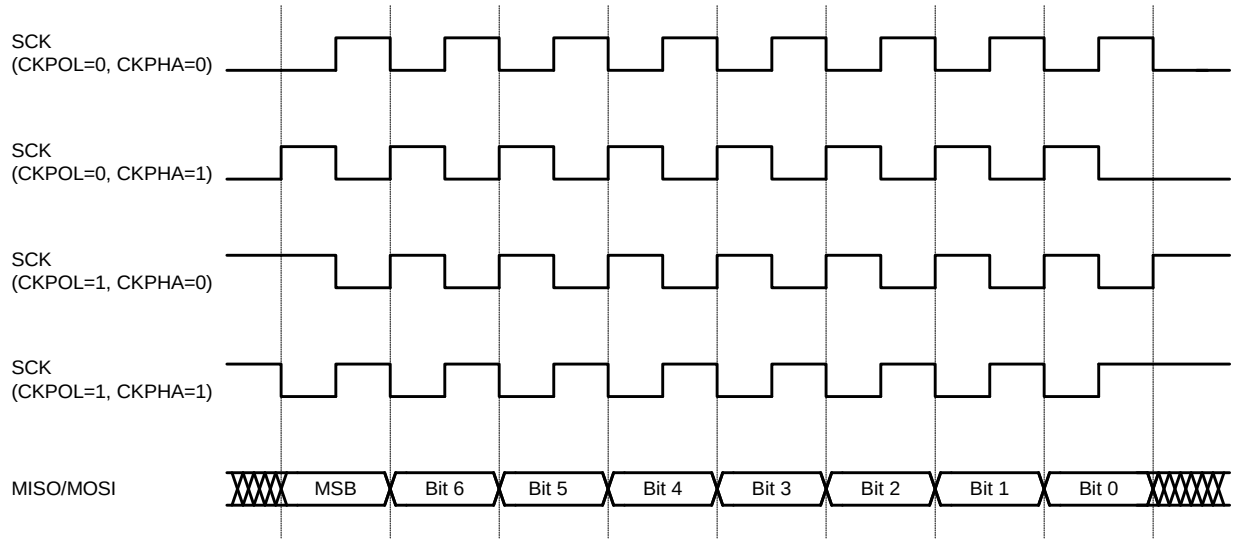
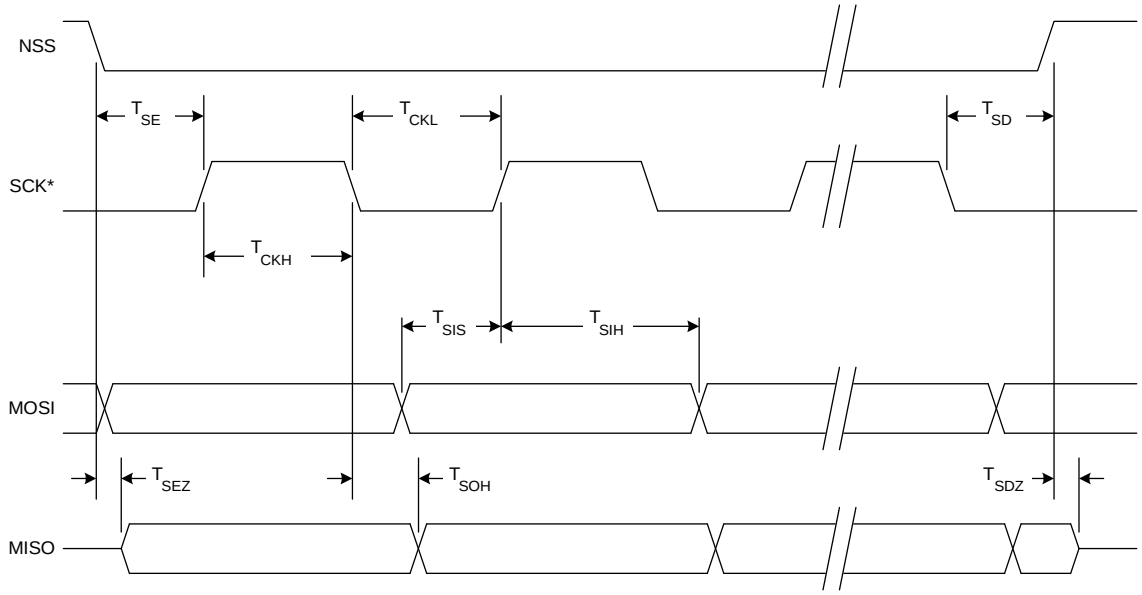


Figure 16.5. Data/Clock Timing Relationship

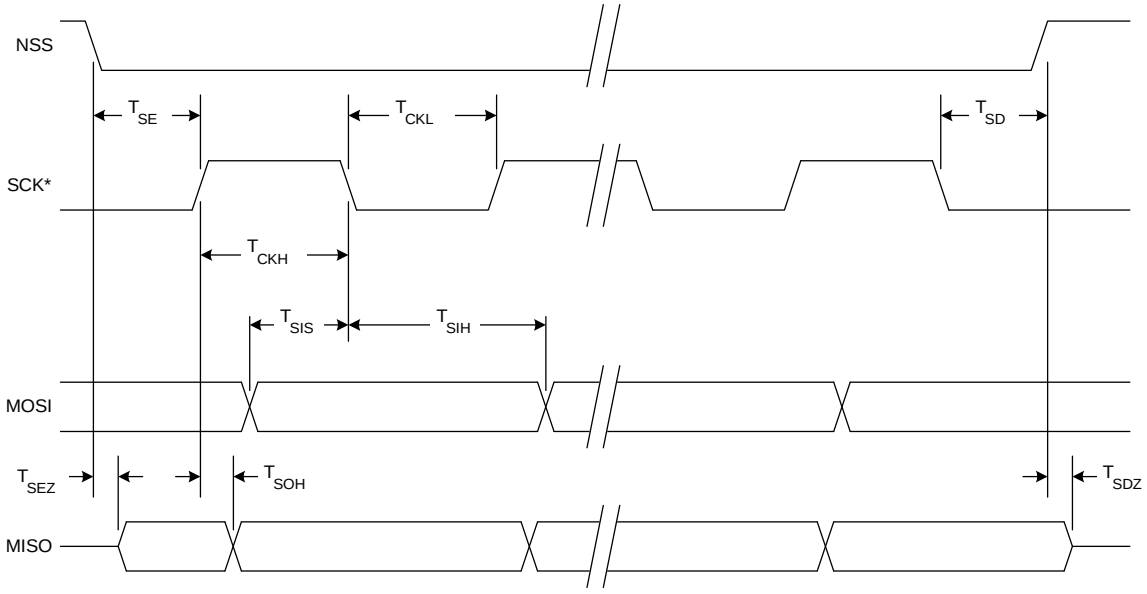
16.6. SPI Special Function Registers

SPI0 is accessed and controlled through four special function registers in the system controller: SPI0CN Control Register, SPI0DAT Data Register, SPI0CFG Configuration Register, and SPI0CKR Clock Rate Register. The four special function registers related to the operation of the SPI0 Bus are described in the following figures.



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 16.8. SPI Slave Timing (CKPHA = 0)



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 16.9. SPI Slave Timing (CKPHA = 1)

17.7. LIN Registers

The following Special Function Registers (SFRs) are available:

17.7.1. LIN Direct Access SFR Registers Definition

SFR Definition 17.1. LINADDR: Indirect Address Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x92

Bit7–0: **LINADDR7-0**: LIN Indirect Address Register Bits.
This register hold an 8-bit address used to indirectly access the LIN0 core registers. Table 17.4 lists the LIN0 core registers and their indirect addresses. Reads and writes to LINDATA will target the register indicated by the LINADDR bits.

SFR Definition 17.2. LINDATA: LIN Data Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x93

Bit7–0: **LINDATA7-0**: LIN Indirect Data Register Bits.
When this register is read, it will read the contents of the LIN0 core register pointed to by LINADDR.
When this register is written, it will write the value to the LIN0 core register pointed to by LINADDR.

SFR Definition 17.17. LIN0MUL: LIN0 Multiplier Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
PRESCL[1:0]		LINMUL[4:0]					DIV9	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Address: 0x0D (indirect)

Bit7–6: **PRESCL1–0**: LIN Baud Rate Prescaler Bits.
These bits are the baud rate prescaler bits.

Bit5–1: **LINMUL4–0**: LIN Baud Rate Multiplier Bits.
These bits are the baud rate multiplier bits. These bits are not used in slave mode.

Bit0: **DIV9**: LIN Baud Rate Divider Most Significant Bit.
The most significant bit of the baud rate divider. The 8 least significant bits are in LIN0DIV.
The valid range for the divider is 200 to 511.

SFR Definition 17.18. LIN0ID: LIN0 ID Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
		ID[5:0]						00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Address: 0x0E (indirect)

Bit7–6: **UNUSED**. Read = 00b. Write = don't care.

Bit5–0: **ID5–0**: LIN Identifier Bits.
These bits form the data identifier.

If the LINSIZE bits (LIN0SIZE[3:0]) are 1111b, bits ID[5:4] are used to determine the data size and are interpreted as follows:
00: 2 bytes
01: 2 bytes
10: 4 bytes
11: 8 bytes

clocked by the system clock. When T0M is cleared, Timer 0 is clocked by the source selected by the Clock Scale bits in CKCON (see SFR Definition 18.3).

Setting the TR0 bit (TCON.4) enables the timer when either GATE0 (TMOD.3) is logic 0 or the input signal INT0 is active as defined by bit IN0PL in register IT01CF (see SFR Definition 10.5. IT01CF: INT0/INT1 Configuration). Setting GATE0 to 1 allows the timer to be controlled by the external input signal INT0 (see Section “10.4. Interrupt Register Descriptions” on page 100), facilitating pulse width measurements.

TR0	GATE0	INT0	Counter/Timer
0	X	X	Disabled
1	0	X	Enabled
1	1	0	Disabled
1	1	1	Enabled
X = Don't Care			

Setting TR0 does not force the timer to reset. The timer registers should be loaded with the desired initial value before the timer is enabled.

TL1 and TH1 form the 13-bit register for Timer 1 in the same manner as described above for TL0 and TH0. Timer 1 is configured and controlled using the relevant TCON and TMOD bits just as with Timer 0. The input signal INT0 is used with Timer 1; the INT0 polarity is defined by bit IN1PL in register IT01CF (see SFR Definition 10.5. IT01CF: INT0/INT1 Configuration).

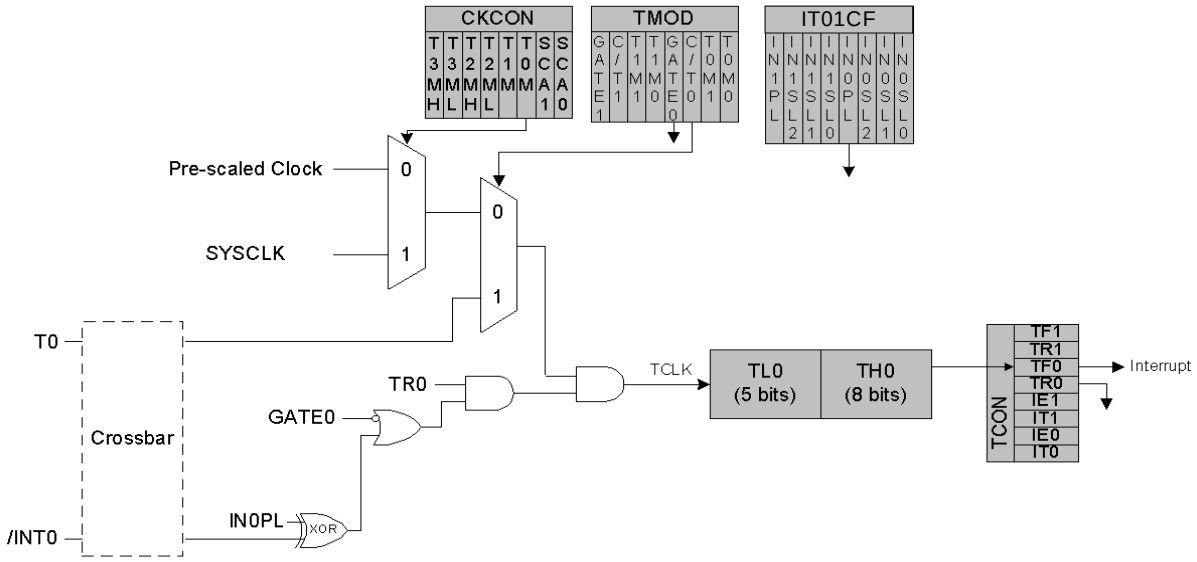


Figure 18.1. T0 Mode 0 Block Diagram

Revision 1.2 to 1.3

- Updated “System Overview” on page 13 with a voltage range specification for the internal oscillator.
- Updated Table 2.11 on page 34 with new conditions for the internal oscillator accuracy. The internal oscillator accuracy is dependent on the operating voltage range.
- Updated Section 2 to remove the internal oscillator curve across temperature diagram.
- Updated Figure “4.5 12-Bit ADC Burst Mode Example with Repeat Count Set to 4” on page 58 with new timing diagram when using CNVSTR pin.
- Updated SFR Definition 5.1 (REF0CN) with oscillator suspend requirement for ZTCEN.
- Updated SFR Definition 6.1 (REG0CN) with a new definition for Bit 6. The bit 6 reset value is 1b and must be written to 1b.
- Updated Section “8.3.3. Suspend Mode” on page 90 with note regarding ZTCEN.
- Updated Section “17. LIN (C8051F520/0A/3/3A/6/6A and C8051F530/0A/3/3A/6/6A)” on page 164 with a voltage range specification for the internal oscillator.

Revision 1.3 to 1.4

- Added ‘AEC-Q100’ qualification information on page 1.
- Changed page headers throughout the document from ‘C8051F52x/F52xA/F53x/F53xA’ to ‘C8051F52x/53x’.
- Updated supply voltage to "2.0 to 5.25 V" on page 1 and in Section 1 on page 13.
- Corrected reference to development kit (C8051F530DK) in Section “1.2.4. On-Chip Debug Circuitry” on page 18.
- Updated minimum Supply Input Voltage (V_{REGIN}) for C8051F52x-C/F53x-C devices in Table 2.2 on page 26 and Table 2.6 on page 30.
- Updated digital supply current (I_{DD} and Idle I_{DD}) typical values for condition ‘Clock = 25 MHz’ in Table 2.2 on page 26.
- Updated I_{DD} Frequency Sensitivity and Idle I_{DD} Frequency Sensitivity values in Table 2.2 on page 26; removed Figure 2.1 and Figure 2.2 that used to provide the same frequency sensitivity slopes. Also removed IDD Supply Sensitivity and Idle IDD Supply Sensitivity typical values.
- Added Digital Supply Current (Stop or Suspend Mode) values at multiple temperatures Table 2.2 on page 26.
- Added a note in Table 2.3, “ADC0 Electrical Characteristics,” on page 28 with reference to Section “4.4. Selectable Gain” on page 60; also added note to indicate that additional tracking time may be necessary if VDD is less than the minimum specified VDD.
- Split off temperature sensor specifications from Table 2.3 into a separate table Table 2.4; Updated temperature sensor gain and added supply current values.
- Added temperature condition for Bias Current specification in Table 2.6 on page 30.
- Updated Comparator Input Offset Voltage values in Table 2.7 on page 31.
- Updated VDD Monitor (VDDMON0) Low Threshold ($V_{RST-LOW}$) minimum value for C8051F52xA/F52x-C/F53xA/F53x-C devices in Table 2.8 on page 32.
- Updated VDD Monitor (VDDMON0) supply current values in Table 2.8 on page 32.
- Added specifications for the new level-sensitive VDD monitor (VDDMON1) to Table 2.8, “Reset Electrical Characteristics,” on page 32 and also added notes to clarify the applicable V_{RST} theshold level.
- Added note in Table 2.9, “Flash Electrical Characteristics,” on page 33 to describe the minimum flash programming temperature for –I (Industrial Grade) devices; Also added the same note and references to it in Section “12.1. Programming The Flash Memory” on page 113, Section “12.3. Non-volatile Data Storage” on page 117, and in SFR Definition 12.1 (PSCTL).