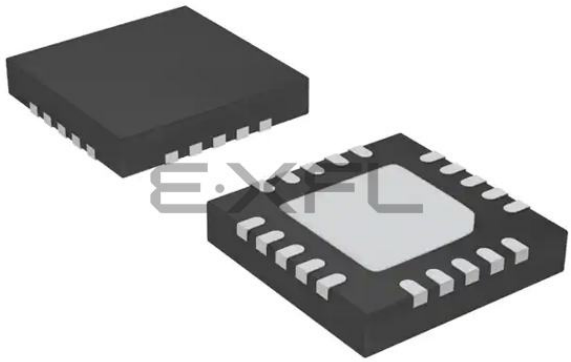

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f534a-imr

Table 1.2. Product Selection Guide (Not Recommended for New Designs)

Ordering Part Number	Flash Memory (kB)	Port I/Os	LIN	Package	Ordering Part Number	Flash Memory (kB)	Port I/Os	LIN	Package
C8051F520-IM C8051F520A-IM	8	6	✓	DFN-10	C8051F534-IM C8051F534A-IM	4	16	—	QFN-20
C8051F521-IM C8051F521A-IM	8	6	—	DFN-10	C8051F536-IM C8051F536A-IM	2	16	✓	QFN-20
C8051F523-IM C8051F523A-IM	4	6	✓	DFN-10	C8051F537-IM C8051F537A-IM	2	16	—	QFN-20
C8051F524-IM C8051F524A-IM	4	6	—	DFN-10	C8051F530-IT C8051F530A-IT	8	16	✓	TSSOP-20
C8051F526-IM C8051F526A-IM	2	6	✓	DFN-10	C8051F531-IT C8051F531A-IT	8	16	—	TSSOP-20
C8051F527-IM C8051F527A-IM	2	6	—	DFN-10	C8051F533-IT C8051F533A-IT	4	16	✓	TSSOP-20
C8051F530-IM C8051F530A-IM	8	16	✓	QFN-20	C8051F534-IT C8051F534A-IT	4	16	—	TSSOP-20
C8051F531-IM C8051F531A-IM	8	16	—	QFN-20	C8051F536-IT C8051F536A-IT	2	16	✓	TSSOP-20
C8051F533-IM C8051F533A-IM	4	16	✓	QFN-20	C8051F537-IT C8051F537A-IT	2	16	—	TSSOP-20

The part numbers in Table 1.2 are not recommended for new designs. Instead, select the corresponding part number from Table 1.1 (silicon revision C) for your design. In Table 1.2, the part numbers in the format similar to C8051F520-IM are silicon revision A devices. The part numbers in the format similar to C8051F520A-IM are silicon revision B devices.

1.9. Port Input/Output

C8051F52x/F52xA/F53x/F53xA devices include up to 16 I/O pins. Port pins are organized as two byte-wide ports. The port pins behave like typical 8051 ports with a few enhancements. Each port pin can be configured as a digital or analog I/O pin. Pins selected as digital I/O can be configured for push-pull or open-drain operation. The “weak pullups” that are fixed on typical 8051 devices may be globally disabled to save power.

The Digital Crossbar allows mapping of internal digital system resources to port I/O pins. On-chip counter/timers, serial buses, hardware interrupts, and other digital signals can be configured to appear on the port pins using the Crossbar control registers. This allows the user to select the exact mix of general-purpose port I/O, digital, and analog resources needed for the application.

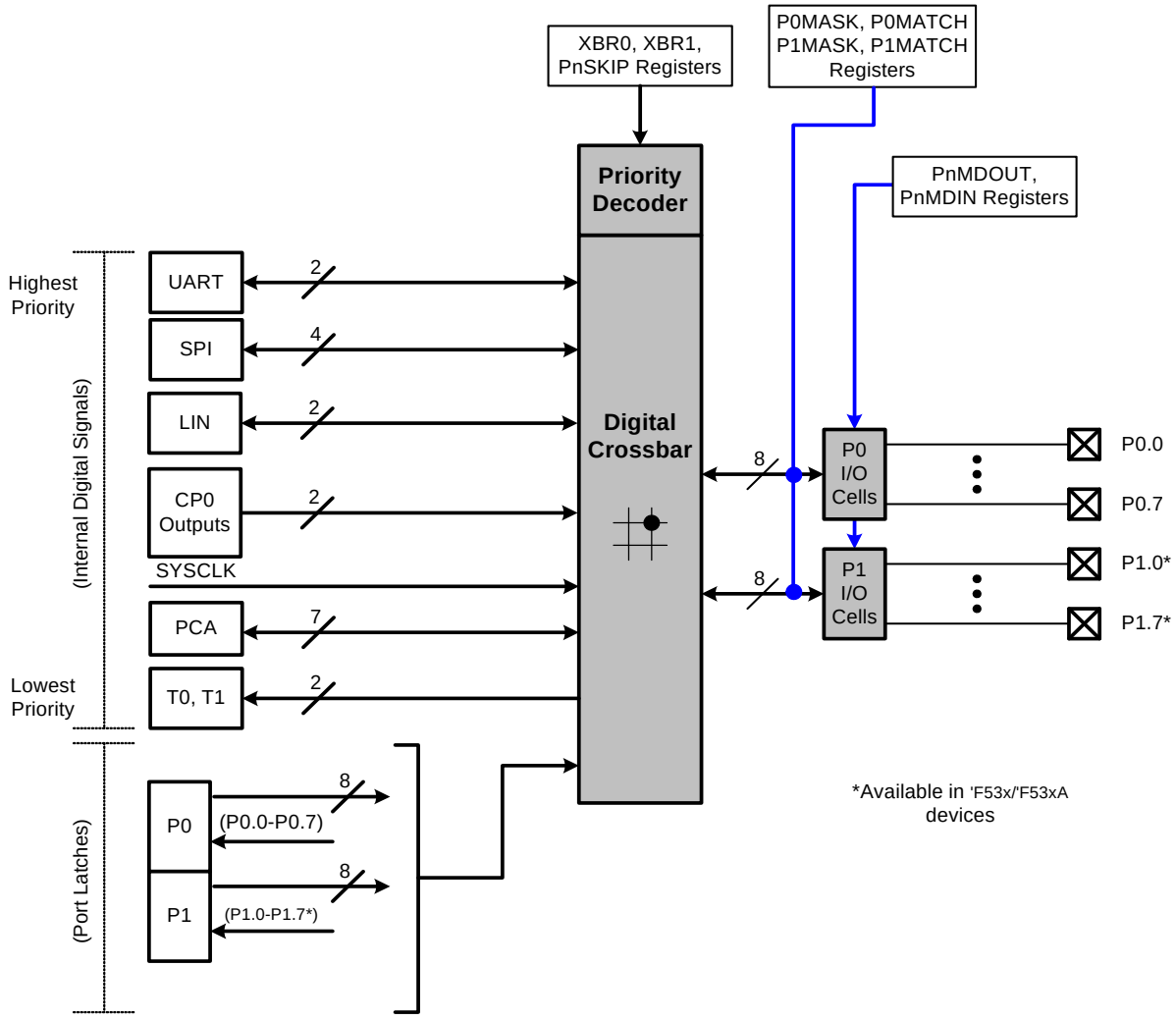


Figure 1.9. Port I/O Functional Block Diagram

Table 2.9. Flash Electrical Characteristics

V_{DD} = 1.8 to 2.75 V; –40 to +125 ºC unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Flash Size	’F520/0A/1/1A and ’F530/0A/1/1A ’F523/3A/4/4A and ’F533/3A/4/4A ’F526/6A/7/7A and ’F536/6A/7/7A	7680 4096 2048	—	—	bytes
Endurance[2]	$V_{DD} \geq V_{RST\text{-}HIGH}$[1]	20 k	150 k	—	Erase/Write
Erase Cycle Time		27	32	38	ms
Write Cycle Time		57	65	74	µs
V_{DD}	Write/Erase Operations	$V_{RST\text{-}HIGH}$[1]	—	—	V

Notes:

1. See Table 2.8 on page 32 for the $V_{RST\text{-}HIGH}$ specification.
2. For –I (industrial Grade) parts, flash should be programmed (erase/write) at a minimum temperature of 0 °C for reliable flash operation across the entire temperature range of –40 to +125 °C. This minimum programming temperature does not apply to –A (Automotive Grade) parts.

Table 2.10. Port I/O DC Electrical Characteristics

V_{REGIN} = 2.7 to 5.25 V, –40 to +125 °C unless otherwise specified

Parameters	Conditions	Min	Typ	Max	Units
Output High Voltage	I_{OH} = –3 mA, Port I/O push-pull I_{OH} = –10 µA, Port I/O push-pull I_{OH} = –10 mA, Port I/O push-pull	V_{REGIN} – 0.4 V_{REGIN} – 0.02 —	— — V_{REGIN} – 0.7	— — —	V
Output Low Voltage	**V_{REGIN} = 2.7 V:** I_{OL} = 70 µA I_{OL} = 8.5 mA **V_{REGIN} = 5.25 V:** I_{OL} = 70 µA I_{OL} = 8.5 mA	 — — — —	 — — — —	 45 550 40 400	mV
Input High Voltage		V_{REGIN} x 0.7	—	—	V
Input Low Voltage		—	—	V_{REGIN} x 0.3	V
Input Leakage Current	Weak Pullup Off **C8051F52xA/53xA:** Weak Pullup On, V_{IN} = 0 V; V_{REGIN} = 1.8 V **C8051F52x/52xA/53x/53xA:** Weak Pullup On, V_{IN} = 0 V; V_{REGIN} = 2.7 V Weak Pullup On, V_{IN} = 0 V; V_{REGIN} = 5.25 V	— — — —	— 5 20 65	±2 15 50 115	µA

3. Pinout and Package Definitions

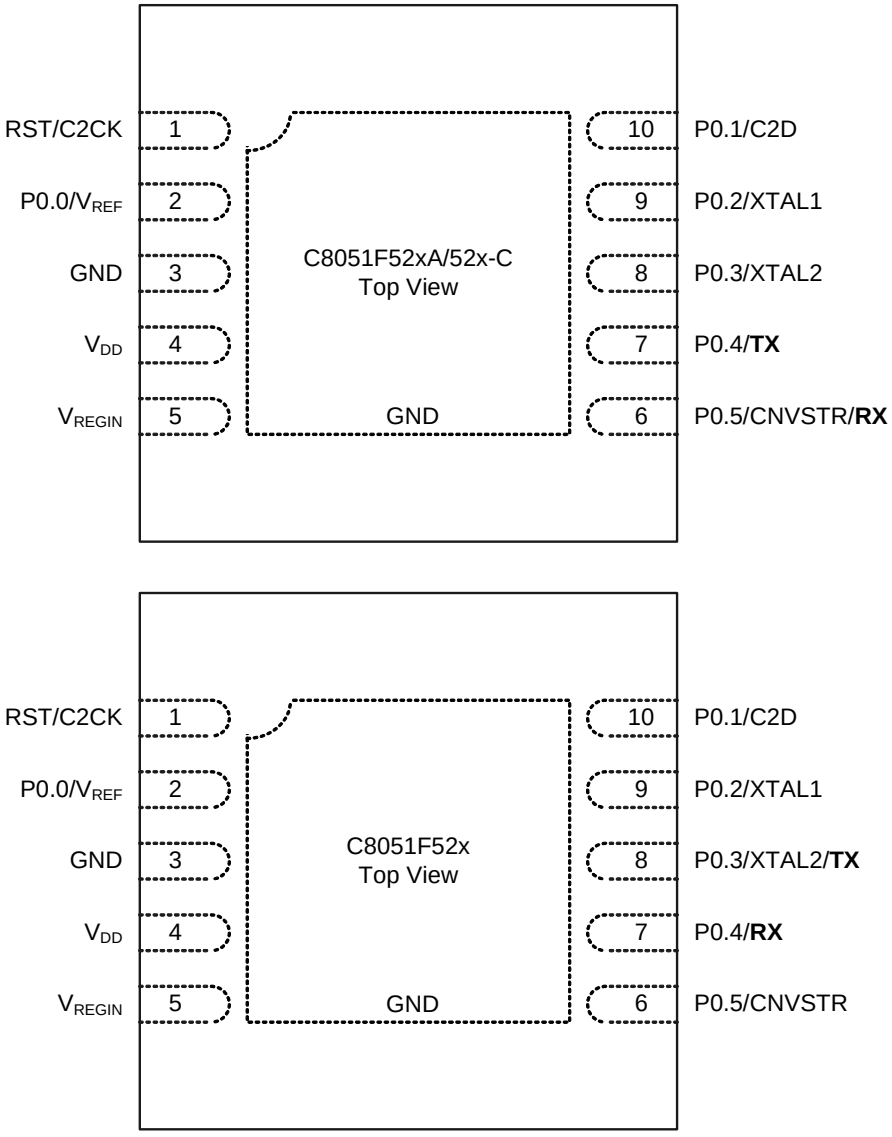


Figure 3.1. DFN-10 Pinout Diagram (Top View)

Table 3.4. Pin Definitions for the C8051F53x and C805153xA (TSSOP 20) (Continued)

Name	Pin Numbers		Type	Description
	'F53xA 'F53x-C	'F53x		
P0.4/TX*	19	—	D I/O or A In	Port 0.4. See Port I/O Section for a complete description.
P0.4/RX*	—	19	D I/O or A In	Port 0.4. See Port I/O Section for a complete description.
P0.3	20	—	D I/O or A In	Port 0.3. See Port I/O Section for a complete description.
P0.3/TX*	—	20	D I/O or A In	Port 0.3. See Port I/O Section for a complete description.
***Note:** Please refer to Section "20. Device Specific Behavior" on page 210.				

Table 3.9. QFN-20 Landing Diagram Dimensions

Symbol	Min	Max
C1	3.90	4.00
C2	3.90	4.00
E	0.50 BSC.	
X1	0.20	0.30
X2	2.75	2.85
Y1	0.65	0.75
Y2	2.75	2.85

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

Solder Mask Design

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 2x2 array of 1.10 x 1.10 mm openings on 1.30 mm pitch should be used for the center ground pad.

Card Assembly

8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

4.2. Temperature Sensor

An on-chip temperature sensor is included on the C8051F52x/F52xA/F53x/F53xA devices which can be directly accessed via the ADC0 multiplexer. To use ADC0 to measure the temperature sensor, the ADC multiplexer channel should be configured to connect to the temperature sensor. The temperature sensor transfer function is shown in Figure 5.2. The output voltage (V_{TEMP}) is the positive ADC input selected by bits AD0MX[4:0] in register ADC0MX. The TEMPE bit in register REF0CN enables/disables the temperature sensor, as described in SFR Definition 5.1. While disabled, the temperature sensor defaults to a high impedance state and any ADC measurements performed on the sensor will result in meaningless data. Refer to Table 5.1 for the slope and offset parameters of the temperature sensor.

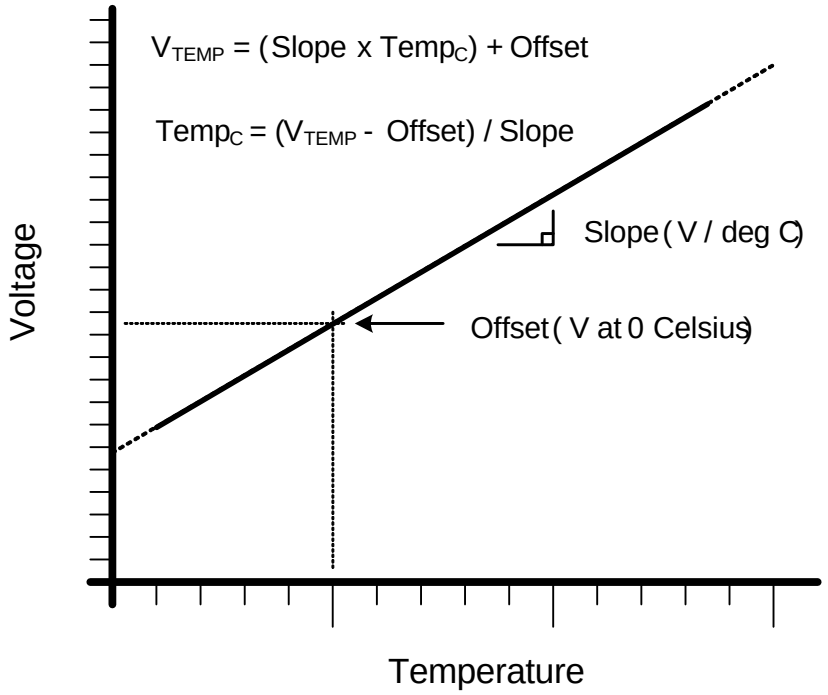


Figure 4.2. Typical Temperature Sensor Transfer Function

SFR Definition 4.8. ADC0CN: ADC0 Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
AD0EN	BURSTEN	AD0INT	AD0BUSY	AD0WINT	AD0LJST	AD0CM1	AD0CM0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
							(bit addressable)	0xE8

Bit7: **AD0EN**: ADC0 Enable Bit.
0: ADC0 Disabled. ADC0 is in low-power shutdown.
1: ADC0 Enabled. ADC0 is active and ready for data conversions.

Bit6: **BURSTEN**: ADC0 Burst Mode Enable Bit.
0: ADC0 Burst Mode Disabled.
1: ADC0 Burst Mode Enabled.

Bit5: **AD0INT**: ADC0 Conversion Complete Interrupt Flag.
0: ADC0 has not completed a data conversion since the last time AD0INT was cleared.
1: ADC0 has completed a data conversion.

Bit4: **AD0BUSY**: ADC0 Busy Bit.
Read:
0: ADC0 conversion is complete or a conversion is not currently in progress. AD0INT is set to logic 1 on the falling edge of AD0BUSY.
1: ADC0 conversion is in progress.
Write:
0: No Effect.
1: Initiates ADC0 Conversion if AD0CM1–0 = 00b

Bit3: **AD0WINT**: ADC0 Window Compare Interrupt Flag.
This bit must be cleared by software.
0: ADC0 Window Comparison Data match has not occurred since this flag was last cleared.
1: ADC0 Window Comparison Data match has occurred.

Bit2: **AD0LJST**: ADC0 Left Justify Select
0: Data in ADC0H:ADC0L registers is right justified.
1: Data in ADC0H:ADC0L registers is left justified. This option should not be used with a repeat count greater than 1 (when AD0RPT1–0 is 01b, 10b, or 11b).

Bits1–0: **AD0CM1–0**: ADC0 Start of Conversion Mode Select.
00: ADC0 conversion initiated on every write of 1 to AD0BUSY.
01: ADC0 conversion initiated on overflow of Timer 1.
10: ADC0 conversion initiated on rising edge of external CNVSTR.
11: ADC0 conversion initiated on overflow of Timer 2.

7. Comparator

C8051F52x/F52xA/F53x/F53xA devices include one on-chip programmable voltage comparator. The Comparator is shown in Figure 7.1.

The Comparator offers programmable response time and hysteresis, an analog input multiplexer, and two outputs that are optionally available at the Port pins: a synchronous “latched” output (CP0), or an asynchronous “raw” output (CP0A). The asynchronous CP0A signal is available even when the system clock is not active. This allows the Comparator to operate and generate an output with the device in STOP or SUSPEND mode. When assigned to a Port pin, the Comparator output may be configured as open drain or push-pull (see Section “13.2. Port I/O Initialization” on page 126). The Comparator may also be used as a reset source (see Section “11.5. Comparator Reset” on page 110).

The Comparator inputs are selected in the CPT0MX register (SFR Definition 7.2). The CMX0P3–CMX0P0 bits select the Comparator0 positive input; the CMX0N3–CMX0N0 bits select the Comparator0 negative input.

Important Note About Comparator Inputs: The Port pins selected as Comparator inputs should be configured as analog inputs in their associated Port configuration register and configured to be skipped by the Crossbar (for details on Port configuration, see Section “13.3. General Purpose Port I/O” on page 128).

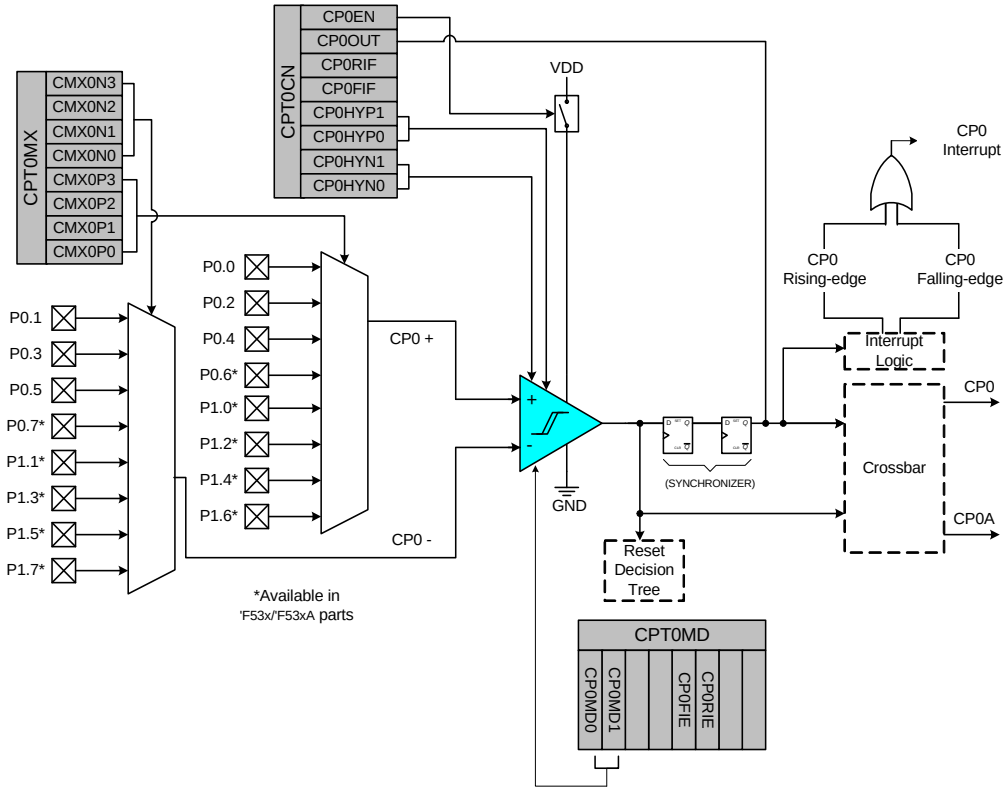


Figure 7.1. Comparator Functional Block Diagram

The Comparator output can be polled in software, used as an interrupt source, internal oscillator suspend awakening source and/or routed to a Port pin. When routed to a Port pin, the Comparator output is available asynchronous or synchronous to the system clock; the asynchronous output is available even in STOP or SUSPEND mode (with no system clock active). When disabled, the Comparator output (if assigned to a Port I/O pin via the Crossbar) defaults to the logic low state, and its supply current falls to

8. CIP-51 Microcontroller

The MCU system controller core is the CIP-51 microcontroller. The CIP-51 is fully compatible with the MCS-51™ instruction set. Standard 803x/805x assemblers and compilers can be used to develop software. The C8051F52x/F52xA/F53x/F53xA family has a superset of all the peripherals included with a standard 8051. See Section “1. System Overview” on page 13 for more information about the available peripherals. The CIP-51 includes on-chip debug hardware which interfaces directly with the analog and digital subsystems, providing a complete data acquisition or control-system solution in a single integrated circuit.

The CIP-51 Microcontroller core implements the standard 8051 organization and peripherals as well as additional custom peripherals and functions to extend its capability (see Figure 8.1 for a block diagram). The CIP-51 core includes the following features:

- Fully Compatible with MCS-51 Instruction Set
- 25 MIPS Peak Throughput
- 256 Bytes of Internal RAM
- Extended Interrupt Handler
- Reset Input
- Power Management Modes
- Integrated Debug Logic
- Program and Data Memory Security

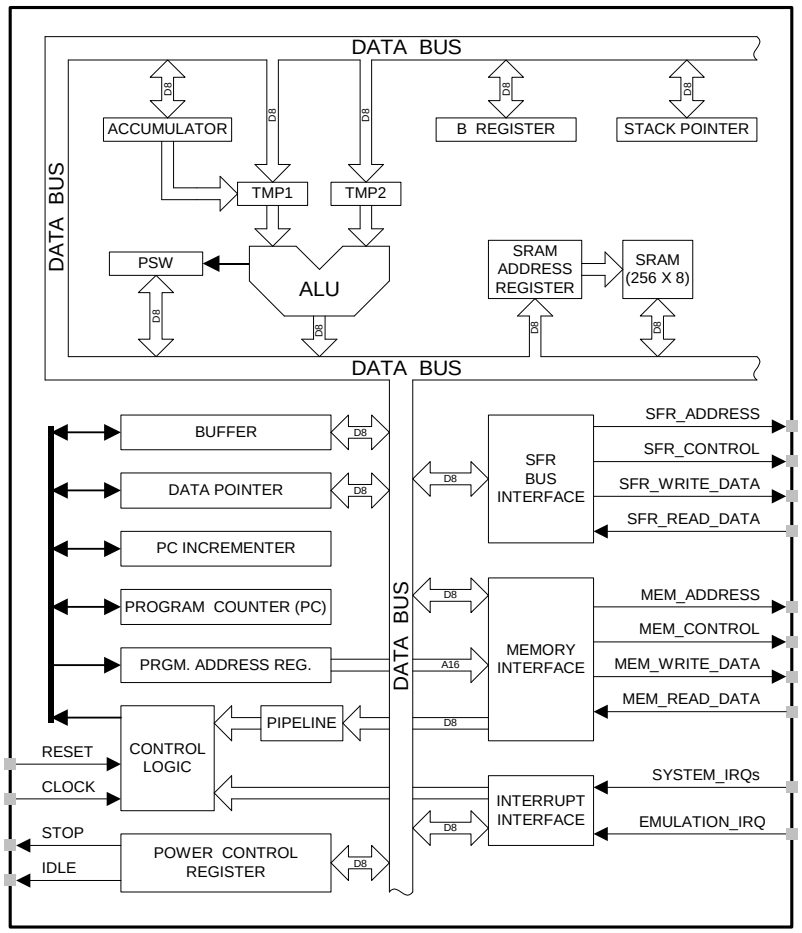
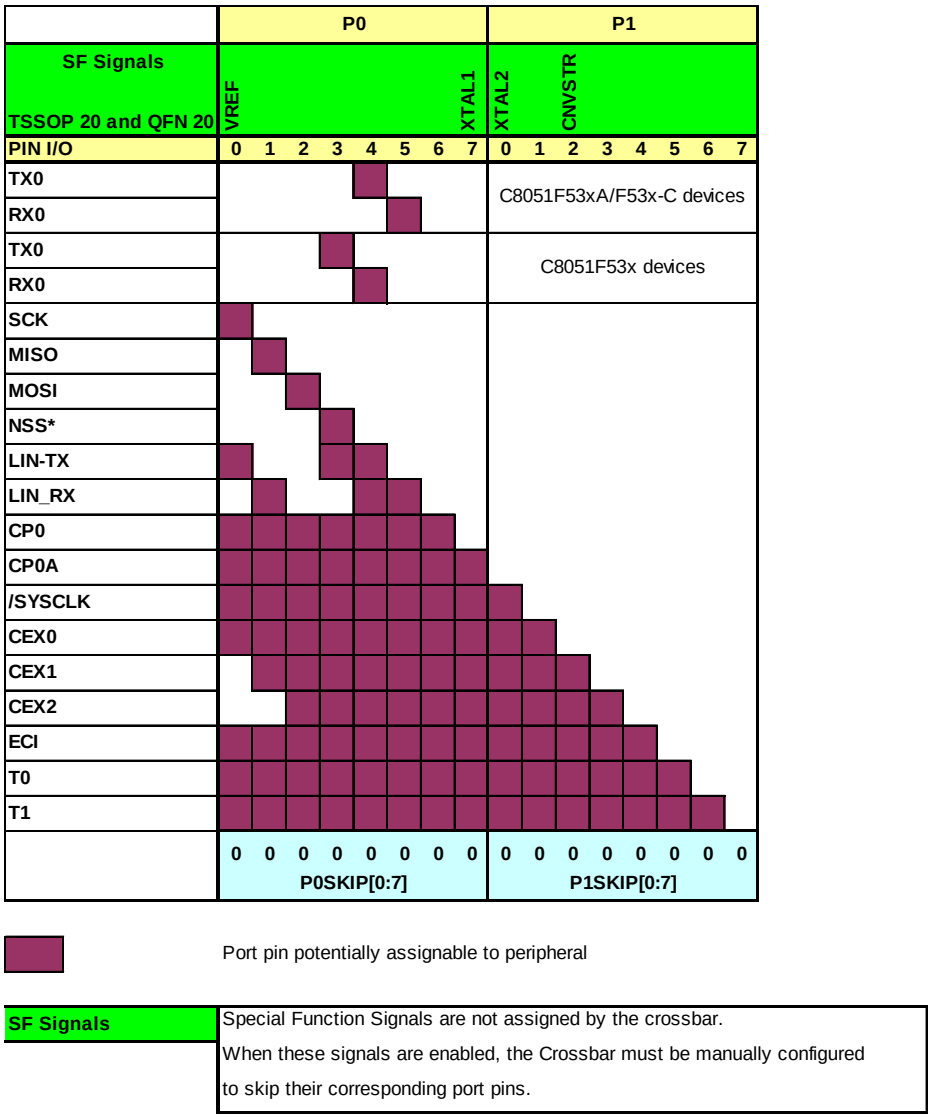


Figure 8.1. CIP-51 Block Diagram

13.1. Priority Crossbar Decoder

The Priority Crossbar Decoder (Figure 13.3) assigns a priority to each I/O function, starting at the top with UART0. When a digital resource is selected, the least-significant unassigned Port pin is assigned to that resource (excluding UART0, which will be assigned to pins P0.4 and P0.5). If a Port pin is assigned, the Crossbar skips that pin when assigning the next selected resource. Additionally, the Crossbar will skip Port pins whose associated bits in the PnSKIP registers are set. The PnSKIP registers allow software to skip Port pins that are to be used for analog input, dedicated functions, or GPIO.



Note: 4-Wire SPI Only.

Figure 13.3. Crossbar Priority Decoder with No Pins Skipped (TSSOP 20 and QFN 20)

Important Note on Crossbar Configuration: If a Port pin is claimed by a peripheral without use of the Crossbar, its corresponding PnSKIP bit should be set. This applies to P1.0 and/or P0.7 (F53x/F53xA) or P0.2 and/or P0.3 (F52x/F52xA) for the external oscillator, P0.0 for V_{REF}, P1.2 (F53x/F53xA) or P0.5

SFR Definition 13.5. P0MDOUT: Port0 Output Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xA4

Bits7–0: Output Configuration Bits for P0.7–P0.0 (respectively): ignored if corresponding bit in register P0MDIN is logic 0.
0: Corresponding P0.n Output is open-drain.
1: Corresponding P0.n Output is push-pull.

Note: When SDA and SCL appear on any of the Port I/O, each are open-drain regardless of the value of P0MDOUT.

SFR Definition 13.6. P0SKIP: Port0 Skip

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xD4

Bits7–0: **P0SKIP[7:0]**: Port0 Crossbar Skip Enable Bits.
These bits select Port pins to be skipped by the Crossbar Decoder. Port pins used as analog inputs (for ADC or Comparator) or used as special functions (V_{REF} input, external oscillator circuit, CNVSTR input) should be skipped by the Crossbar.
0: Corresponding P0.n pin is not skipped by the Crossbar.
1: Corresponding P0.n pin is skipped by the Crossbar.

SFR Definition 14.2. OSCICL: Internal Oscillator Calibration

R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
—	OSCICL							Varies
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
							SFR Address:	0xB3

Bit7: **UNUSED**. Read = 0b. Write = don't care.
Bits6–0: **OSCICL**: Internal Oscillator Calibration Register.
This register determines the internal oscillator period. On C8051F52x/53x devices, the reset value is factory calibrated to generate an internal oscillator frequency of 24.5 MHz.

SFR Definition 14.3. OSCIFIN: Internal Fine Oscillator Calibration

R/W	R/W	R/W	R	R	R/W	R/W	R/W	Reset Value
—	—	OSCIFIN						undetermined
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable
							SFR Address:	0xB0

Bits7–6: **UNUSED**. Read = 00b, Write = don't care.
Bits5–0: **OSCIFIN**. Internal oscillator fine adjustment bits.

The valid range is between 0x00 and 0x27.

This register is a fine adjustment for the internal oscillator period. On C8051F52x/52xA/53x/53xA devices, the reset value is factory calibrated to generate an internal oscillator frequency of 24.5 MHz.

SFR Definition 17.12. LIN0CTRL: LIN0 Control Register

W	W	W	R/W	R/W	R/W	R/W	R/W	Reset Value
STOP	SLEEP	TXRX	DTACK	RSTINT	RSTERR	WUPREQ	STREQ	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Address: 0x08 (indirect)

Bit7: **STOP**: Stop Communication Processing Bit (**slave mode only**).
This bit is to be set by the application to block the processing of the LIN Communications until the next SYNCH BREAK signal. It is used when the application is handling a data request interrupt and cannot use the frame content with the received identifier (always reads 0).

Bit6: **SLEEP**: Sleep Mode Warning.
This bit is to be set by the application to warn the peripheral that a Sleep Mode Frame was received and that the Bus is in sleep mode or if a Bus Idle timeout interrupt is requested. The application must reset it when a Wake-Up interrupt is requested.

Bit5: **TXRX**: Transmit/Receive Selection Bit.
This bit determines if the current frame is a transmit frame or a receive frame.
0: Current frame is a receive operation.
1: Current frame is a transmit operation.

Bit4: **DTACK**: Data acknowledge bit (**slave mode only**).
Set to 1 after handling a data request interrupt to acknowledge the transfer. The bit will automatically be cleared to 0 by the LIN controller.

Bit3: **RSTINT**: Interrupt Reset bit.
This bit always reads as 0.
0: No effect.
1: Reset the LININT bit (LIN0ST.3).

Bit2: **RSTERR**: Error Reset Bit.
This bit always reads as 0.
0: No effect.
1: Reset the error bits in LIN0ST and LIN0ERR.

Bit1: **WUPREQ**: Wake-Up Request Bit.
Set to 1 to terminate sleep mode by sending a wakeup signal. The bit will automatically be cleared to 0 by the LIN controller.

Bit0: **STREQ**: Start Request Bit (**master mode only**).
1: Start a LIN transmission. This should be set only after loading the identifier, data length and data buffer if necessary.
The bit is reset to 0 upon transmission completion or error detection.

clocked by the system clock. When T0M is cleared, Timer 0 is clocked by the source selected by the Clock Scale bits in CKCON (see SFR Definition 18.3).

Setting the TR0 bit (TCON.4) enables the timer when either GATE0 (TMOD.3) is logic 0 or the input signal INT0 is active as defined by bit IN0PL in register IT01CF (see SFR Definition 10.5. IT01CF: INT0/INT1 Configuration). Setting GATE0 to 1 allows the timer to be controlled by the external input signal INT0 (see Section “10.4. Interrupt Register Descriptions” on page 100), facilitating pulse width measurements.

TR0	GATE0	INT0	Counter/Timer
0	X	X	Disabled
1	0	X	Enabled
1	1	0	Disabled
1	1	1	Enabled
X = Don't Care			

Setting TR0 does not force the timer to reset. The timer registers should be loaded with the desired initial value before the timer is enabled.

TL1 and TH1 form the 13-bit register for Timer 1 in the same manner as described above for TL0 and TH0. Timer 1 is configured and controlled using the relevant TCON and TMOD bits just as with Timer 0. The input signal INT0 is used with Timer 1; the INT0 polarity is defined by bit IN1PL in register IT01CF (see SFR Definition 10.5. IT01CF: INT0/INT1 Configuration).

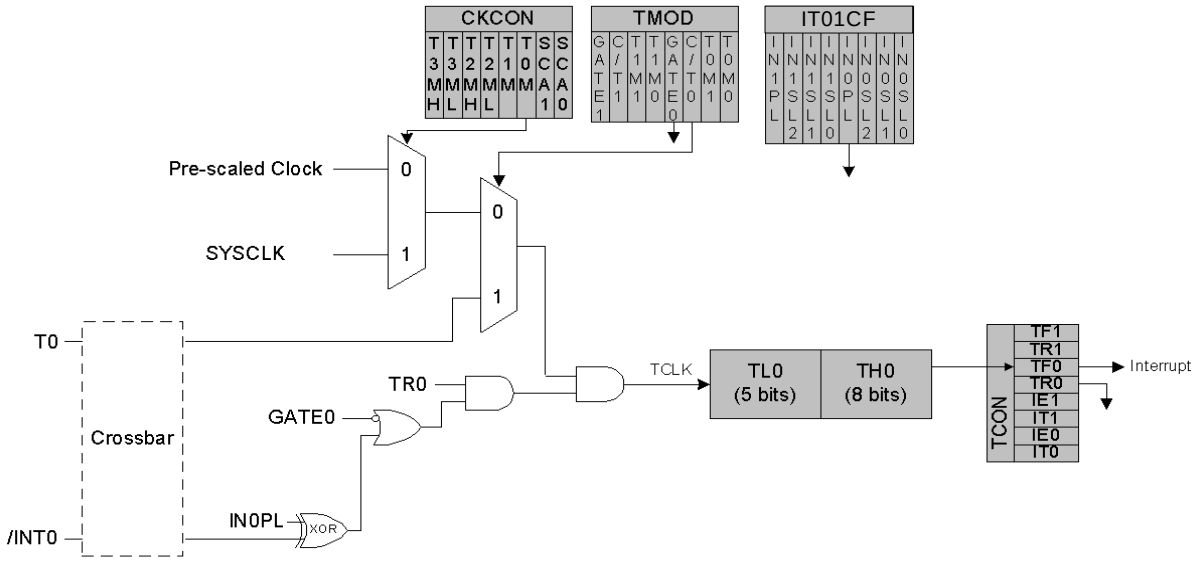


Figure 18.1. T0 Mode 0 Block Diagram

19.2. Capture/Compare Modules

Each module can be configured to operate independently in one of six operation modes: Edge-triggered Capture, Software Timer, High Speed Output, Frequency Output, 8-Bit Pulse Width Modulator, or 16-Bit Pulse Width Modulator. Each module has Special Function Registers (SFRs) associated with it in the CIP-51 system controller. These registers are used to exchange data with a module and configure the module's mode of operation.

Table 19.2 summarizes the bit settings in the PCA0CPMn registers used to select the PCA capture/compare module's operating modes. Setting the ECCFn bit in a PCA0CPMn register enables the module's CCFn interrupt. Note that PCA0 interrupts must be globally enabled before individual CCFn interrupts are recognized. PCA0 interrupts are globally enabled by setting the EA bit and the EPCA0 bit to logic 1. See Figure 19.3 for details on the PCA interrupt configuration.

Table 19.2. PCA0CPM Register Settings for PCA Capture/Compare Modules

PWM16	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	Operation Mode
X	X	1	0	0	0	0	X	Capture triggered by positive edge on CEXn
X	X	0	1	0	0	0	X	Capture triggered by negative edge on CEXn
X	X	1	1	0	0	0	X	Capture triggered by transition on CEXn
X	1	0	0	1	0	0	X	Software Timer
X	1	0	0	1	1	0	X	High Speed Output
X	1	0	0	X	1	1	X	Frequency Output
0	1	0	0	X	0	1	X	8-Bit Pulse Width Modulator
1	1	0	0	X	0	1	X	16-Bit Pulse Width Modulator
X = Don't Care								

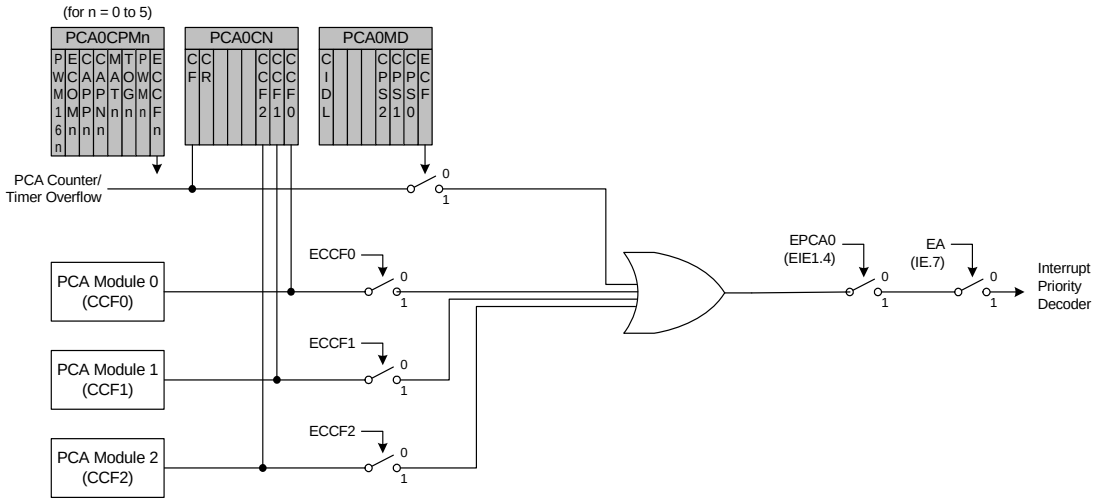


Figure 19.3. PCA Interrupt Block Diagram

19.2.2. Software Timer (Compare) Mode

In Software Timer mode, the PCA counter/timer value is compared to the module's 16-bit capture/compare register (PCA0CPHn and PCA0CPLn). When a match occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1 and an interrupt request is generated if CCF interrupts are enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Setting the ECOMn and MATn bits in the PCA0CPMn register enables Software Timer mode.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

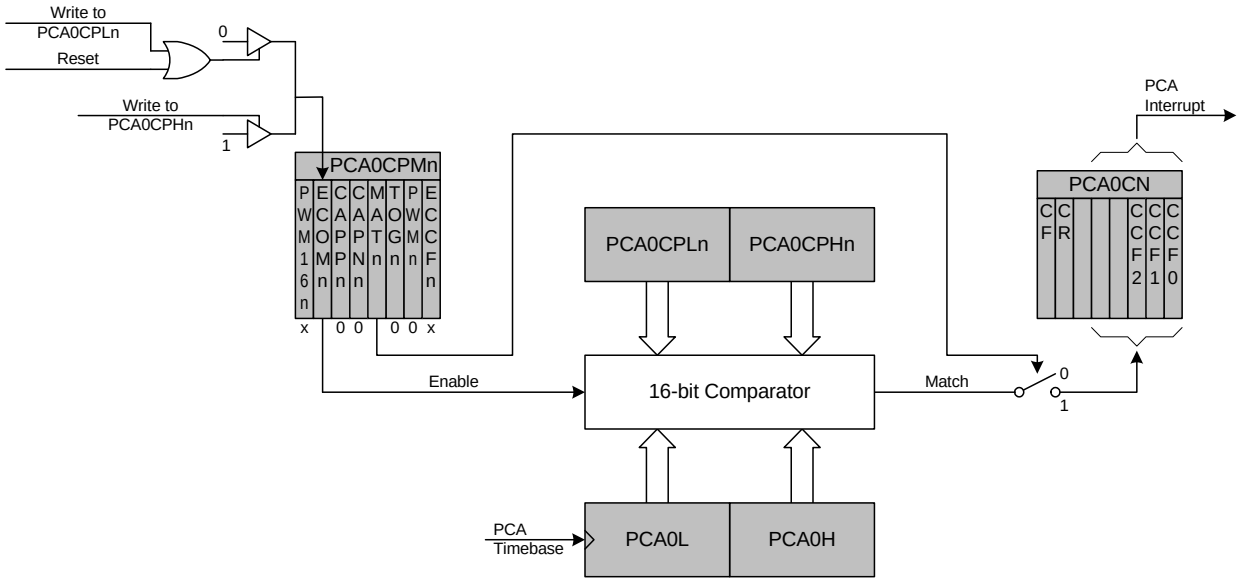


Figure 19.5. PCA Software Timer Mode Diagram

19.3.1. Watchdog Timer Operation

While the WDT is enabled:

- PCA counter is forced on.
- Writes to PCA0L and PCA0H are not allowed.
- PCA clock source bits (CPS2-CPS0) are frozen.
- PCA Idle control bit (CIDL) is frozen.
- Module 2 is forced into software timer mode.
- Writes to the Module 2 mode register (PCA0CPM2) are disabled.

While the WDT is enabled, writes to the CR bit will not change the PCA counter state; the counter will run until the WDT is disabled. The PCA counter run control (CR) will read zero if the WDT is enabled but user software has not enabled the PCA counter. If a match occurs between PCA0CPH2 and PCA0H while the WDT is enabled, a reset will be generated. To prevent a WDT reset, the WDT may be updated with a write of any value to PCA0CPH2. Upon a PCA0CPH2 write, PCA0H plus the offset held in PCA0CPL2 is loaded into PCA0CPH2 (See Figure 19.10).

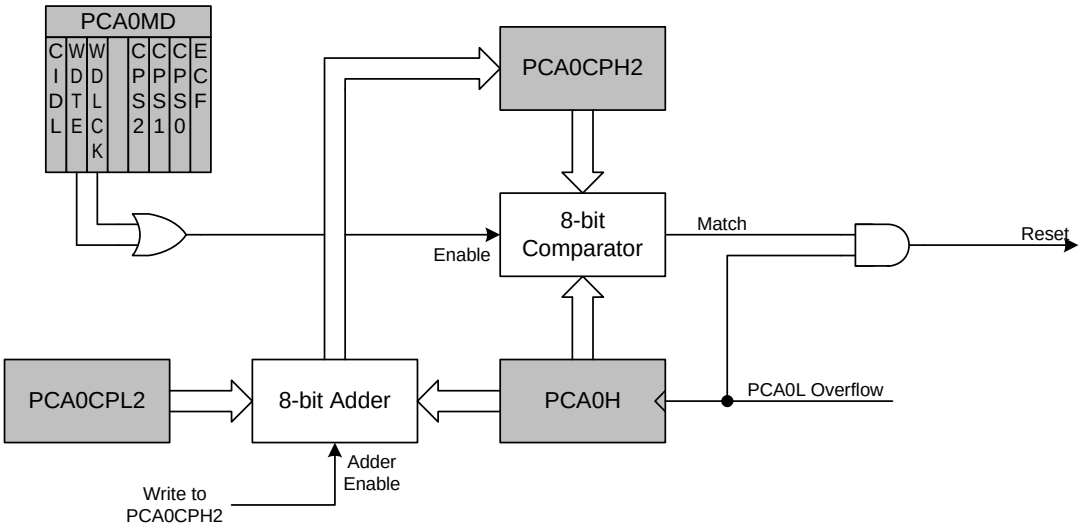


Figure 19.10. PCA Module 2 with Watchdog Timer Enabled

Note that the 8-bit offset held in PCA0CPH2 is compared to the upper byte of the 16-bit PCA counter. This offset value is the number of PCA0L overflows before a reset. Up to 256 PCA clocks may pass before the first PCA0L overflow occurs, depending on the value of the PCA0L when the update is performed. The total offset is then given (in PCA clocks) by Equation 19.4, where PCA0L is the value of the PCA0L register at the time of the update.

$$Offset = (256 \times PCA0CPL2) + (256 - PCA0L)$$

Equation 19.4. Watchdog Timer Offset in PCA Clocks

The WDT reset is generated when PCA0L overflows while there is a match between PCA0CPH2 and PCA0H. Software may force a WDT reset by writing a 1 to the CCF2 flag (PCA0CN.2) while the WDT is enabled.

20.8. UART Pins

The location of the pins used by the serial UART interface differs between the silicon revisions of C8051F52x/52xA/F53x/F53xA devices.

On Revision A devices, the TX and RX pins used by the UART interface are mapped to the P0.3 (TX) and P0.4 (RX) pins. Beginning with Revision B devices, the TX and RX pins used by the UART interface are mapped to the P0.4 (TX) and P0.5 (RX) pins.

Important Note: On Revision B and newer devices, the UART pins must be skipped if the UART is enabled in order for peripherals to appear on port pins beyond the UART on the crossbar. For example, with the SPI and UART enabled on the crossbar with the SPI on P1.0-P1.3, the UART pins must be skipped using P0SKIP for the SPI pins to appear correctly.

20.9. LIN

The LIN peripheral behavior differs between the silicon revisions of C8051F52x/52xA/F53x/F53xA devices. The differences are:

20.9.1. Stop Bit Check

On Revision A devices, the stop bits of the fields in the LIN frame are not checked and no error is generated if the stop bits could not be sent or received correctly. On Revision B and Revision C devices, the stop bits are checked, and an error will be generated if the stop bit was not sent or received correctly.

20.9.2. Synch Break and Synch Field Length Check

On Revision A devices, the check of sync field length versus sync break length is incorrect. On Revision B and Revision C devices, the sync break length must be larger than 10 bit times (of the measured bit time) to enable the synchronization.

21.2. C2 Pin Sharing

The C2 protocol allows the C2 pins to be shared with user functions so that in-system debugging and Flash programming functions may be performed. This is possible because C2 communication is typically performed when the device is in the halt state, where all on-chip peripherals and user software are stalled. In this halted state, the C2 interface can safely ‘borrow’ the C2CK (/RST) and C2D (P0.1 or P0.6) pins. In most applications, external resistors are required to isolate C2 interface traffic from the user application. A typical isolation configuration is shown in Figure 21.1.

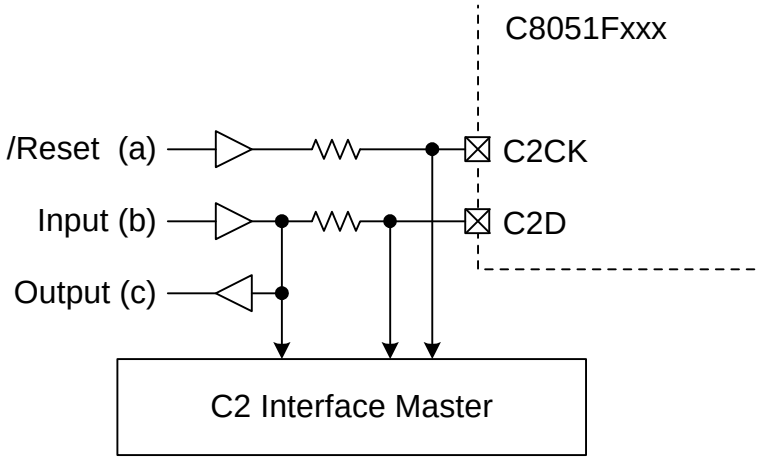


Figure 21.1. Typical C2 Pin Sharing

The configuration in Figure 21.1 assumes the following:

1. The user input (b) cannot change state while the target device is halted.
2. The /RST pin on the target device is used as an input only.

Additional resistors may be necessary depending on the specific application.