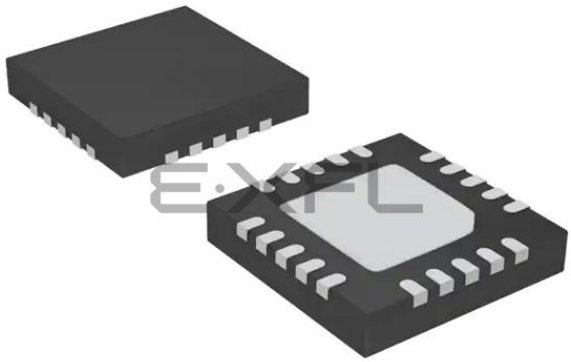

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	16
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f536a-imr

List of Figures

Table 1.2. Product Selection Guide (Not Recommended for New Designs)

Ordering Part Number	Flash Memory (kB)	Port I/Os	LIN	Package	Ordering Part Number	Flash Memory (kB)	Port I/Os	LIN	Package
C8051F520-IM C8051F520A-IM	8	6	✓	DFN-10	C8051F534-IM C8051F534A-IM	4	16	—	QFN-20
C8051F521-IM C8051F521A-IM	8	6	—	DFN-10	C8051F536-IM C8051F536A-IM	2	16	✓	QFN-20
C8051F523-IM C8051F523A-IM	4	6	✓	DFN-10	C8051F537-IM C8051F537A-IM	2	16	—	QFN-20
C8051F524-IM C8051F524A-IM	4	6	—	DFN-10	C8051F530-IT C8051F530A-IT	8	16	✓	TSSOP-20
C8051F526-IM C8051F526A-IM	2	6	✓	DFN-10	C8051F531-IT C8051F531A-IT	8	16	—	TSSOP-20
C8051F527-IM C8051F527A-IM	2	6	—	DFN-10	C8051F533-IT C8051F533A-IT	4	16	✓	TSSOP-20
C8051F530-IM C8051F530A-IM	8	16	✓	QFN-20	C8051F534-IT C8051F534A-IT	4	16	—	TSSOP-20
C8051F531-IM C8051F531A-IM	8	16	—	QFN-20	C8051F536-IT C8051F536A-IT	2	16	✓	TSSOP-20
C8051F533-IM C8051F533A-IM	4	16	✓	QFN-20	C8051F537-IT C8051F537A-IT	2	16	—	TSSOP-20

The part numbers in Table 1.2 are not recommended for new designs. Instead, select the corresponding part number from Table 1.1 (silicon revision C) for your design. In Table 1.2, the part numbers in the format similar to C8051F520-IM are silicon revision A devices. The part numbers in the format similar to C8051F520A-IM are silicon revision B devices.

1.5. 12-Bit Analog to Digital Converter

The C8051F52x/F52xA/F53x/F53xA devices include an on-chip 12-bit SAR ADC with a maximum throughput of 200 ksps. The ADC system includes a configurable analog multiplexer that selects the positive ADC input, which is measured with respect to GND. Ports 0 and 1 are available as ADC inputs; additionally, the ADC includes an innovative programmable gain stage which allows the ADC to sample inputs sources greater than the VREF voltage. The on-chip Temperature Sensor output and the core supply voltage (V_{DD}) are also available as ADC inputs. User firmware may shut down the ADC or use it in Burst Mode to save power.

Conversions can be initiated in four ways: a software command, an overflow of Timer 1, an overflow of Timer 2, or an external convert start signal. This flexibility allows the start of conversion to be triggered by software events, a periodic signal (timer overflows), or external HW signals. Conversion completions are indicated by a status bit and an interrupt (if enabled) and occur after 1, 4, 8, or 16 samples have been accumulated by a hardware accumulator. The resulting 12-bit to 16-bit data word is latched into the ADC data SFRs upon completion of a conversion. When the system clock is slow, Burst Mode allows ADC0 to automatically wake from a low power shutdown state, acquire and accumulate samples, then re-enter the low power shutdown state without CPU intervention.

Window compare registers for the ADC data can be configured to interrupt the controller when ADC data is either within or outside of a specified range. The ADC can monitor a key voltage continuously in background mode, but not interrupt the controller unless the converted data is within/outside the specified range.

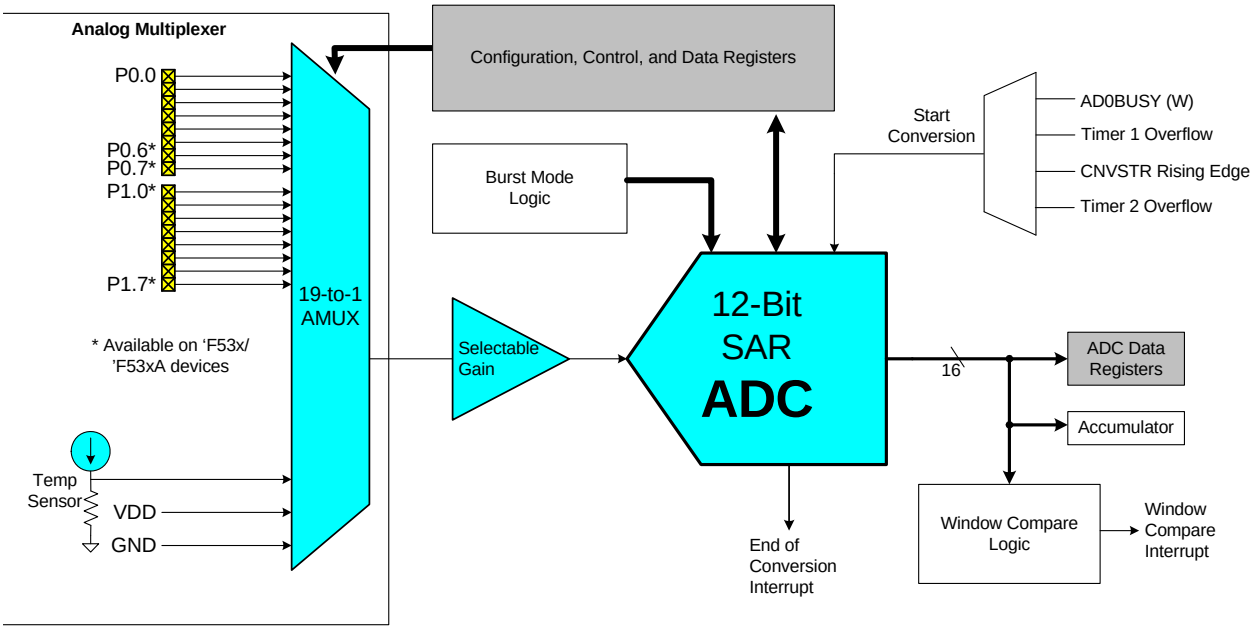

Figure 1.7. 12-Bit ADC Block Diagram

Table 2.9. Flash Electrical Characteristics

V_{DD} = 1.8 to 2.75 V; –40 to +125 ºC unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Flash Size	’F520/0A/1/1A and ’F530/0A/1/1A ’F523/3A/4/4A and ’F533/3A/4/4A ’F526/6A/7/7A and ’F536/6A/7/7A	7680 4096 2048	—	—	bytes
Endurance[2]	$V_{DD} \geq V_{RST\text{-}HIGH}$[1]	20 k	150 k	—	Erase/Write
Erase Cycle Time		27	32	38	ms
Write Cycle Time		57	65	74	µs
V_{DD}	Write/Erase Operations	$V_{RST\text{-}HIGH}$[1]	—	—	V

Notes:

1. See Table 2.8 on page 32 for the $V_{RST\text{-}HIGH}$ specification.
2. For –I (industrial Grade) parts, flash should be programmed (erase/write) at a minimum temperature of 0 °C for reliable flash operation across the entire temperature range of –40 to +125 °C. This minimum programming temperature does not apply to –A (Automotive Grade) parts.

Table 2.10. Port I/O DC Electrical Characteristics

V_{REGIN} = 2.7 to 5.25 V, –40 to +125 °C unless otherwise specified

Parameters	Conditions	Min	Typ	Max	Units
Output High Voltage	I_{OH} = –3 mA, Port I/O push-pull I_{OH} = –10 µA, Port I/O push-pull I_{OH} = –10 mA, Port I/O push-pull	V_{REGIN} – 0.4 V_{REGIN} – 0.02 —	— — V_{REGIN} – 0.7	— — —	V
Output Low Voltage	**V_{REGIN} = 2.7 V:** I_{OL} = 70 µA I_{OL} = 8.5 mA **V_{REGIN} = 5.25 V:** I_{OL} = 70 µA I_{OL} = 8.5 mA	 — — — —	 — — — —	 45 550 40 400	mV
Input High Voltage		V_{REGIN} x 0.7	—	—	V
Input Low Voltage		—	—	V_{REGIN} x 0.3	V
Input Leakage Current	Weak Pullup Off **C8051F52xA/53xA:** Weak Pullup On, V_{IN} = 0 V; V_{REGIN} = 1.8 V **C8051F52x/52xA/53x/53xA:** Weak Pullup On, V_{IN} = 0 V; V_{REGIN} = 2.7 V Weak Pullup On, V_{IN} = 0 V; V_{REGIN} = 5.25 V	— — — —	— 5 20 65	±2 15 50 115	µA

Table 3.1. Pin Definitions for the C8051F52x and C8051F52xA (DFN 10) (Continued)

Name	Pin Numbers		Type	Description
	‘F52xA ‘F52x-C	‘F52x		
P0.3/TX*/	—	8	D I/O or A In	Port 0.3. See Port I/O Section for a complete description.
XTAL2			D I/O	External Clock Output. For an external crystal or resonator, this pin is the excitation driver. This pin is the external clock input for CMOS, capacitor, or RC oscillator configurations. See Section “14. Oscillators” on page 135.
P0.2	9	9	D I/O or	Port 0.2. See Port I/O Section for a complete description.
XTAL1			A In	External Clock Input. This pin is the external oscillator return for a crystal or resonator. Section “14. Oscillators” on page 135.
P0.1/	10	10	D I/O or A In	Port 0.1. See Port I/O Section for a complete description.
C2D			D I/O	Bi-directional data signal for the C2 Debug Interface
Note: Please refer to Section “20. Device Specific Behavior” on page 210.				

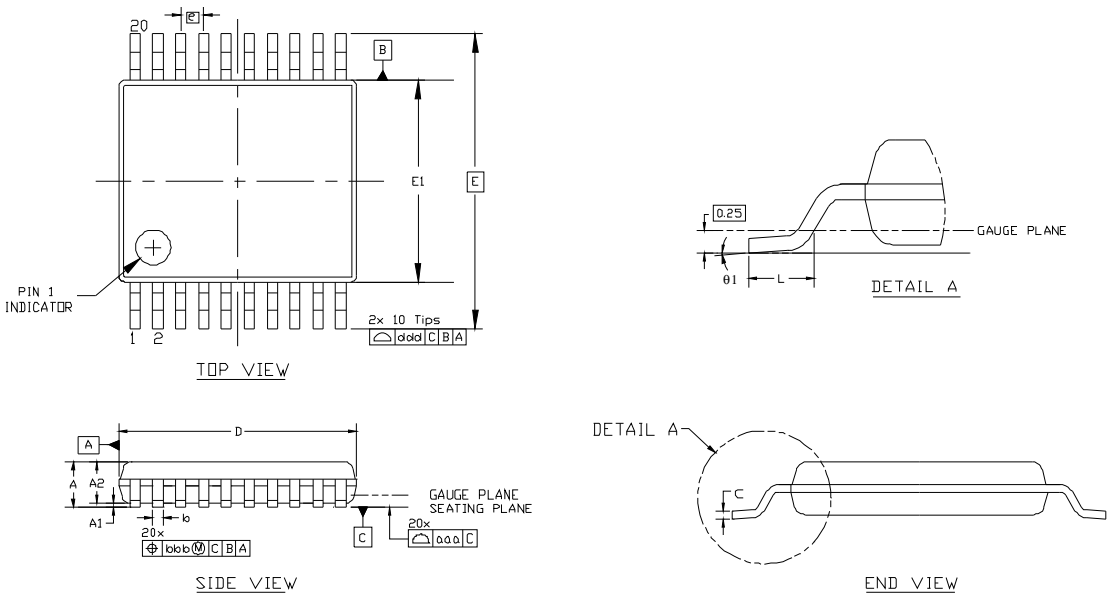

Figure 3.5. TSSOP-20 Package Diagram

Table 3.5. TSSOP-20 Package Diagram Dimensions

Symbol	Min	Nom	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
c	0.09	—	0.20
D	6.40	6.50	6.60
e	0.65 BSC.		
E	6.40 BSC.		
E1	4.30	4.40	4.50
L	0.45	0.60	0.75
θ1	0°	—	8°
aaa	0.10		
bbb	0.10		
ddd	0.20		

Notes:

1. All dimensions shown are in millimeters (mm).
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-153, variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Table 3.7. Pin Definitions for the C8051F53x and C805153xA (QFN 20)

Name	Pin Numbers		Type	Description
	‘F53xA ‘F53x-C	‘F53x		
$\overline{RST}$/ C2CK	1	1	D I/O D I/O	Device Reset. Open-drain output of internal POR or V_{DD} monitor. An external source can initiate a system reset by driving this pin low for at least the minimum $\overline{RST}$ low time to generate a system reset, as defined in Table 2.8 on page 32. A 1 kΩ pullup to V_{REGIN} is recommended. See Reset Sources Section for a complete description. Clock signal for the C2 Debug Interface.
P0.0/ V_{REF}	2	2	D I/O or A In A O or D In	Port 0.0. See Port I/O Section for a complete description. External V_{REF} Input. See V_{REF} Section.
GND	3	3		Ground.
V_{DD}	4	4		Core Supply Voltage.
V_{REGIN}	5	5		On-Chip Voltage Regulator Input.
P1.7	6	6	D I/O or A In	Port 1.7. See Port I/O Section for a complete description.
P1.6	7	7	D I/O or A In	Port 1.6. See Port I/O Section for a complete description.
P1.5	8	8	D I/O or A In	Port 1.5. See Port I/O Section for a complete description.
P1.4	9	9	D I/O or A In	Port 1.4. See Port I/O Section for a complete description.
P1.3	10	10	D I/O or A In	Port 1.3. See Port I/O Section for a complete description.
P1.2/ CNVSTR	11	11	D I/O or A In D In	Port 1.2. See Port I/O Section for a complete description. External Converter start input for the ADC0, see Section “4. 12-Bit ADC (ADC0)” on page 52 for a complete description.
P1.1	12	12	D I/O or A In	Port 1.1. See Port I/O Section for a complete description.
Note: Please refer to Section “20. Device Specific Behavior” on page 210.				

4.3.5. Output Conversion Code

The registers ADC0H and ADC0L contain the high and low bytes of the output conversion code. When the repeat count is set to 1, conversion codes are represented in 12-bit unsigned integer format and the output conversion code is updated after each conversion. Inputs are measured from 0 to V_{REF} x 4095/4096. Data can be right-justified or left-justified, depending on the setting of the AD0LJST bit (ADC0CN.2). Unused bits in the ADC0H and ADC0L registers are set to 0. Example codes are shown below for both right-justified and left-justified data.

Input Voltage	Right-Justified ADC0H:ADC0L (AD0LJST = 0)	Left-Justified ADC0H:ADC0L (AD0LJST = 1)
V_{REF} x 4095/4096	0x0FFF	0xFFF0
V_{REF} x 2048/4096	0x0800	0x8000
V_{REF} x 2047/4096	0x07FF	0x7FF0
0	0x0000	0x0000

When the ADC0 Repeat Count is greater than 1, the output conversion code represents the accumulated result of the conversions performed and is updated after the last conversion in the series is finished. Sets of 4, 8, or 16 consecutive samples can be accumulated and represented in unsigned integer format. The repeat count can be selected using the AD0RPT bits in the ADC0CF register. The value must be right-justified (AD0LJST = “0”), and unused bits in the ADC0H and ADC0L registers are set to '0'. The following example shows right-justified codes for repeat counts greater than 1. Notice that accumulating 2^n samples is equivalent to left-shifting by *n* bit positions when all samples returned from the ADC have the same value.

Input Voltage	Repeat Count = 4	Repeat Count = 8	Repeat Count = 16
V_{REF} x 4095/4096	0x3FFC	0x7FF8	0xFFF0
V_{REF} x 2048/4096	0x2000	0x4000	0x8000
V_{REF} x 2047/4096	0x1FFC	0x3FF8	0x7FF0
0	0x0000	0x0000	0x0000

4.3.6. Settling Time Requirements

A minimum tracking time is required before an accurate conversion can be performed. This tracking time is determined by the AMUX0 resistance, the ADC0 sampling capacitance, any external source resistance, and the accuracy required for the conversion.

Figure 4.6 shows the equivalent ADC0 input circuit. The required ADC0 settling time for a given settling accuracy (SA) may be approximated by Equation 4.1. When measuring the Temperature Sensor output, use the settling time specified in Table 2.3 on page 28. See Table 2.3 on page 28 for ADC0 minimum settling time requirements.

$$t = \ln\left(\frac{2^n}{SA}\right) \times R_{TOTAL} C_{SAMPLE}$$

Equation 4.1. ADC0 Settling Time Requirements

Where:
SA is the settling accuracy, given as a fraction of an LSB (for example, 0.25 to settle within 1/4 LSB)
t is the required settling time in seconds
R_{TOTAL} is the sum of the AMUX0 resistance and any external source resistance.
n is the ADC resolution in bits (12).

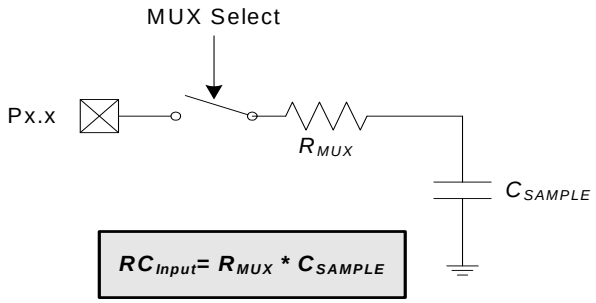

Figure 4.6. ADC0 Equivalent Input Circuits

4.4. Selectable Gain

ADC0 on the C8051F52x/52xA/53x/53xA family of devices implements a selectable gain adjustment option. By writing a value to the gain adjust address range, the user can select gain values between 0 and 1.016.

For example, three analog sources to be measured have full-scale outputs of 5.0 V, 4.0 V, and 3.0 V, respectively. Each ADC measurement would ideally use the full dynamic range of the ADC with an internal voltage reference of 1.5 V or 2.2 V (set to 2.2 V for this example). When selecting signal one (5.0 V full-scale), a gain value of 0.44 (5 V full scale * 0.44 = 2.2 V full scale) provides a full-scale signal of 2.2 V when the input signal is 5.0 V. Likewise, a gain value of 0.55 (4 V full scale * 0.55 = 2.2 V full scale) for the second source and 0.73 (3 V full scale * 0.73 = 2.2 V full scale) for the third source provide full-scale ADC0 measurements when the input signal is full-scale.

Additionally, some sensors or other input sources have small part-to-part variations that must be accounted for to achieve accurate results. In this case, the programmable gain value could be used as a calibration value to eliminate these part-to-part variations.

SFR Definition 4.8. ADC0CN: ADC0 Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
AD0EN	BURSTEN	AD0INT	AD0BUSY	AD0WINT	AD0LJST	AD0CM1	AD0CM0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
							(bit addressable)	0xE8

Bit7: **AD0EN**: ADC0 Enable Bit.
0: ADC0 Disabled. ADC0 is in low-power shutdown.
1: ADC0 Enabled. ADC0 is active and ready for data conversions.

Bit6: **BURSTEN**: ADC0 Burst Mode Enable Bit.
0: ADC0 Burst Mode Disabled.
1: ADC0 Burst Mode Enabled.

Bit5: **AD0INT**: ADC0 Conversion Complete Interrupt Flag.
0: ADC0 has not completed a data conversion since the last time AD0INT was cleared.
1: ADC0 has completed a data conversion.

Bit4: **AD0BUSY**: ADC0 Busy Bit.
Read:
0: ADC0 conversion is complete or a conversion is not currently in progress. AD0INT is set to logic 1 on the falling edge of AD0BUSY.
1: ADC0 conversion is in progress.
Write:
0: No Effect.
1: Initiates ADC0 Conversion if AD0CM1–0 = 00b

Bit3: **AD0WINT**: ADC0 Window Compare Interrupt Flag.
This bit must be cleared by software.
0: ADC0 Window Comparison Data match has not occurred since this flag was last cleared.
1: ADC0 Window Comparison Data match has occurred.

Bit2: **AD0LJST**: ADC0 Left Justify Select
0: Data in ADC0H:ADC0L registers is right justified.
1: Data in ADC0H:ADC0L registers is left justified. This option should not be used with a repeat count greater than 1 (when AD0RPT1–0 is 01b, 10b, or 11b).

Bits1–0: **AD0CM1–0**: ADC0 Start of Conversion Mode Select.
00: ADC0 conversion initiated on every write of 1 to AD0BUSY.
01: ADC0 conversion initiated on overflow of Timer 1.
10: ADC0 conversion initiated on rising edge of external CNVSTR.
11: ADC0 conversion initiated on overflow of Timer 2.

SFR Definition 6.1. REG0CN: Regulator Control

R/W	R/W	R	R/W	R	R	R	R	Reset Value
REGDIS	Reserved	—	REG0MD	—	—	—	DROPOUT	01010000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xC9

Bit7: **REGDIS**: Voltage Regulator Disable Bit.
This bit disables/enables the Voltage Regulator.
0: Voltage Regulator Enabled.
1: Voltage Regulator Disabled.
Bit6: **RESERVED**. Read = 1b. Must write 1b.
Bit5: **UNUSED**. Read = 0b. Write = don't care.
Bit4: **REG0MD**: Voltage Regulator Mode Select Bit.
This bit selects the Voltage Regulator output voltage.
0: Voltage Regulator output is 2.1 V.
1: Voltage Regulator output is 2.6 V (default).
Bits3–1: **UNUSED**. Read = 000b. Write = don't care.
Bit0: **DROPOUT**: Voltage Regulator Dropout Indicator Bit.
0: Voltage Regulator is not in dropout.
1: Voltage Regulator is in or near dropout.

SFRs used to configure and access the sub-systems unique to the MCU. This allows the addition of new functionality while retaining compatibility with the MCS-51™ instruction set. Table 9.1 lists the SFRs implemented in the CIP-51 System Controller.

The SFR registers are accessed anytime the direct addressing mode is used to access memory locations from 0x80 to 0xFF. SFRs with addresses ending in 0x0 or 0x8 (e.g. P0, TCON, IE, etc.) are bit-addressable as well as byte-addressable. All other SFRs are byte-addressable only. Unoccupied addresses in the SFR space are reserved for future use. Accessing these areas will have an indeterminate effect and should be avoided. Refer to the corresponding pages of the data sheet, as indicated in Table 9.2, for a detailed description of each register.

Table 9.1. Special Function Register (SFR) Memory Map

F8	SPI0CN	PCA0L	PCA0H	PCA0CPL0	PCA0CPH0			VDDMON
F0	B	P0MDIN	P1MDIN				EIP1	
E8	ADC0CN	PCA0CPL1	PCA0CPH1	PCA0CPL2	PCA0CPH2			RSTSRC
E0	ACC	XBR0	XBR1		IT01CF		EIE1	
D8	PCA0CN	PCA0MD	PCA0CPM0	PCA0CPM1	PCA0CPM2			
D0	PSW	REF0CN			P0SKIP	P1SKIP		P0MAT
C8	TMR2CN	REG0CN	TMR2RLL	TMR2RLH	TMR2L	TMR2H		P1MAT
C0				ADC0GTL	ADC0GTH	ADC0LTL	ADC0LTH	P0MASK
B8	IP		ADC0TK	ADC0MX	ADC0CF	ADC0L	ADC0	P1MASK
B0	OSCIFIN	OSCXCN	OSCICN	OSCICL				FLKEY
A8	IE	CLKSEL						
A0		SPI0CFG	SPI0CKR	SPI0DAT	P0MDOUT	P1MDOUT		
98	SCON0	SBUF0		CPT0CN		CPT0MD		CPT0MX
90	P1		LINADDR	LINDATA		LINCF		
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	PSCTL
80	P0	SP	DPL	DPH				PCON
	0(8) (bit addressable)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)

Table 9.2. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Description	Page
OSCICN	0xB2	Internal Oscillator Control	137
OSCXCN	0xB1	External Oscillator Control	142
P0	0x80	Port 0 Latch	129
P0MASK	0xC7	Port 0 Mask	131
P0MAT	0xD7	Port 0 Match	131
P0MDIN	0xF1	Port 0 Input Mode Configuration	129
P0MDOUT	0xA4	Port 0 Output Mode Configuration	130
P0SKIP	0xD4	Port 0 Skip	130
P1	0x90	Port 1 Latch	132
P1MASK	0xBF	Port 1 Mask	134
P1MAT	0xCF	Port 1 Match	134
P1MDIN	0xF2	Port 1 Input Mode Configuration	132
P1MDOUT	0xA5	Port 1 Output Mode Configuration	133
P1SKIP	0xD5	Port 1 Skip	133
PCA0CN	0xD8	PCA Control	206
PCA0CPH0	0xFC	PCA Capture 0 High	209
PCA0CPH1	0xEA	PCA Capture 1 High	209
PCA0CPH2	0xEC	PCA Capture 2 High	209
PCA0CPL0	0xFB	PCA Capture 0 Low	209
PCA0CPL1	0xE9	PCA Capture 1 Low	209
PCA0CPL2	0xEB	PCA Capture 2 Low	209
PCA0CPM0	0xDA	PCA Module 0 Mode	208
PCA0CPM1	0xDB	PCA Module 1 Mode	208
PCA0CPM2	0xDC	PCA Module 2 Mode	208
PCA0H	0xFA	PCA Counter High	209
PCA0L	0xF9	PCA Counter Low	209
PCA0MD	0xD9	PCA Mode	207
PCON	0x87	Power Control	91
PSCTL	0x8F	Program Store R/W Control	119
PSW	0xD0	Program Status Word	88

The level of Flash security depends on the Flash access method. The three Flash access methods that can be restricted are reads, writes, and erases from the C2 debug interface, user firmware executing on unlocked pages, and user firmware executing on locked pages. Table 12.1 summarizes the Flash security features of the ’F52x/’F52xA/’F53x/’F53xA devices.

Table 12.1. Flash Security Summary

Action	C2 Debug Interface	User Firmware executing from:	
		an unlocked page	a locked page
Read, Write or Erase unlocked pages (except page with Lock Byte)	Permitted	Permitted	Permitted
Read, Write or Erase locked pages (except page with Lock Byte)	Not Permitted	Flash Error Reset	Permitted
Read or Write page containing Lock Byte (if no pages are locked)	Permitted	Permitted	Permitted
Read or Write page containing Lock Byte (if any page is locked)	Not Permitted	Flash Error Reset	Permitted
Read contents of Lock Byte (if no pages are locked)	Permitted	Permitted	Permitted
Read contents of Lock Byte (if any page is locked)	Not Permitted	Flash Error Reset	Permitted
Erase page containing Lock Byte (if no pages are locked)	Permitted	Flash Error Reset	Flash Error Reset
Erase page containing Lock Byte—Unlock all pages (if any page is locked)	C2 Device Erase Only	Flash Error Reset	Flash Error Reset
Lock additional pages (change 1s to 0s in the Lock Byte)	Not Permitted	Flash Error Reset	Flash Error Reset
Unlock individual pages (change 0s to 1s in the Lock Byte)	Not Permitted	Flash Error Reset	Flash Error Reset
Read, Write or Erase Reserved Area	Not Permitted	Flash Error Reset	Flash Error Reset

C2 Device Erase—Erases all Flash pages including the page containing the Lock Byte.

Flash Error Reset—Not permitted; Causes Flash Error Device Reset (FERROR bit in RSTSRC is 1 after reset).

- All prohibited operations that are performed via the C2 interface are ignored (do not cause device reset).
- Locking any Flash page also locks the page containing the Lock Byte.
- Once written to, the Lock Byte cannot be modified except by performing a C2 Device Erase.
- If user code writes to the Lock Byte, the Lock does not take effect until the next device reset.

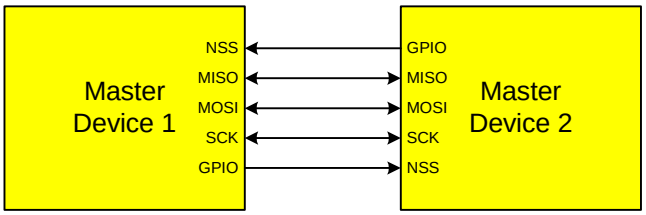

Figure 16.2. Multiple-Master Mode Connection Diagram

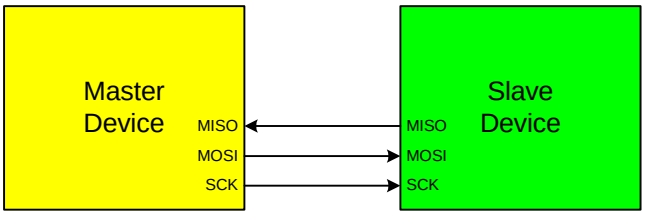

Figure 16.3. 3-Wire Single Master and Slave Mode Connection Diagram

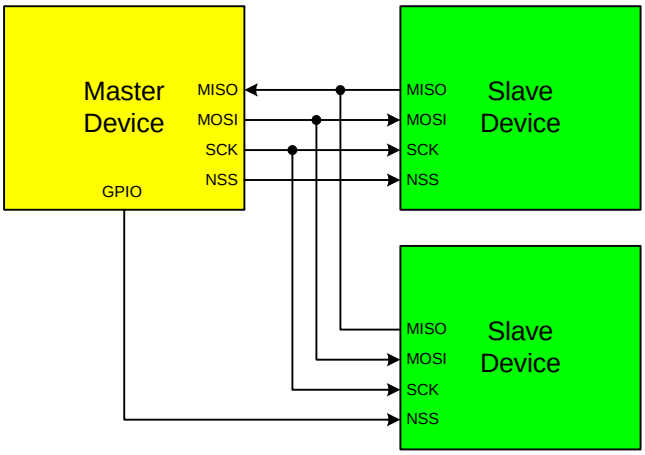

Figure 16.4. 4-Wire Single Master and Slave Mode Connection Diagram

16.3. SPI0 Slave Mode Operation

When SPI0 is enabled and not configured as a master, it will operate as a SPI slave. As a slave, bytes are shifted in through the MOSI pin and out through the MISO pin by a master device controlling the SCK signal. A bit counter in the SPI0 logic counts SCK edges. When 8 bits have been shifted into the shift register, the SPIF flag is set to logic 1, and the byte is copied into the receive buffer. Data is read from the receive buffer by reading SPI0DAT. A slave device cannot initiate transfers. Data to be transferred to the master device is pre-loaded into the shift register by writing to SPI0DAT. Writes to SPI0DAT are double-buffered, and are placed in the transmit buffer first. If the shift register is empty, the contents of the transmit buffer will immediately be transferred into the shift register. When the shift register already contains data, the SPI will load the shift register with the transmit buffer's contents after the last SCK edge of the next (or current) SPI transfer.

SFR Definition 16.3. SPI0CKR: SPI0 Clock Rate

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
SCR7	SCR6	SCR5	SCR4	SCR3	SCR2	SCR1	SCR0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xA2

Bits7–0: **SCR7–SCR0**: SPI0 Clock Rate.
These bits determine the frequency of the SCK output when the SPI0 module is configured for master mode operation. The SCK clock frequency is a divided version of the system clock, and is given in the following equation, where *SYSCLK* is the system clock frequency and *SPI0CKR* is the 8-bit value held in the SPI0CKR register.

$$f_{SCK} = \frac{SYSCLK}{2 \times (SPI0CKR + 1)}$$

for 0 <= SPI0CKR <= 255

Example: If SYSCLK = 2 MHz and SPI0CKR = 0x04,

$$f_{SCK} = \frac{2000000}{2 \times (4 + 1)}$$

$$f_{SCK} = 200kHz$$

SFR Definition 18.9. TMR2RLL: Timer 2 Reload Register Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xCA

Bits7–0: **TMR2RLL**: Timer 2 Reload Register Low Byte.
TMR2RLL holds the low byte of the reload value for Timer 2.

SFR Definition 18.10. TMR2RLH: Timer 2 Reload Register High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xCB

Bits7–0: **TMR2RLH**: Timer 2 Reload Register High Byte.
The TMR2RLH holds the high byte of the reload value for Timer 2.

SFR Definition 18.11. TMR2L: Timer 2 Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xCC

Bits7–0: **TMR2L**: Timer 2 Low Byte.
In 16-bit mode, the TMR2L register contains the low byte of the 16-bit Timer 2. In 8-bit mode, TMR2L contains the 8-bit low byte timer value.

SFR Definition 18.12. TMR2H Timer 2 High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xCD

Bits7–0: **TMR2H**: Timer 2 High Byte.
In 16-bit mode, the TMR2H register contains the high byte of the 16-bit Timer 2. In 8-bit mode, TMR2H contains the 8-bit high byte timer value.

19.2. Capture/Compare Modules

Each module can be configured to operate independently in one of six operation modes: Edge-triggered Capture, Software Timer, High Speed Output, Frequency Output, 8-Bit Pulse Width Modulator, or 16-Bit Pulse Width Modulator. Each module has Special Function Registers (SFRs) associated with it in the CIP-51 system controller. These registers are used to exchange data with a module and configure the module's mode of operation.

Table 19.2 summarizes the bit settings in the PCA0CPMn registers used to select the PCA capture/compare module's operating modes. Setting the ECCFn bit in a PCA0CPMn register enables the module's CCFn interrupt. Note that PCA0 interrupts must be globally enabled before individual CCFn interrupts are recognized. PCA0 interrupts are globally enabled by setting the EA bit and the EPCA0 bit to logic 1. See Figure 19.3 for details on the PCA interrupt configuration.

Table 19.2. PCA0CPM Register Settings for PCA Capture/Compare Modules

PWM16	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	Operation Mode
X	X	1	0	0	0	0	X	Capture triggered by positive edge on CEXn
X	X	0	1	0	0	0	X	Capture triggered by negative edge on CEXn
X	X	1	1	0	0	0	X	Capture triggered by transition on CEXn
X	1	0	0	1	0	0	X	Software Timer
X	1	0	0	1	1	0	X	High Speed Output
X	1	0	0	X	1	1	X	Frequency Output
0	1	0	0	X	0	1	X	8-Bit Pulse Width Modulator
1	1	0	0	X	0	1	X	16-Bit Pulse Width Modulator
X = Don't Care								

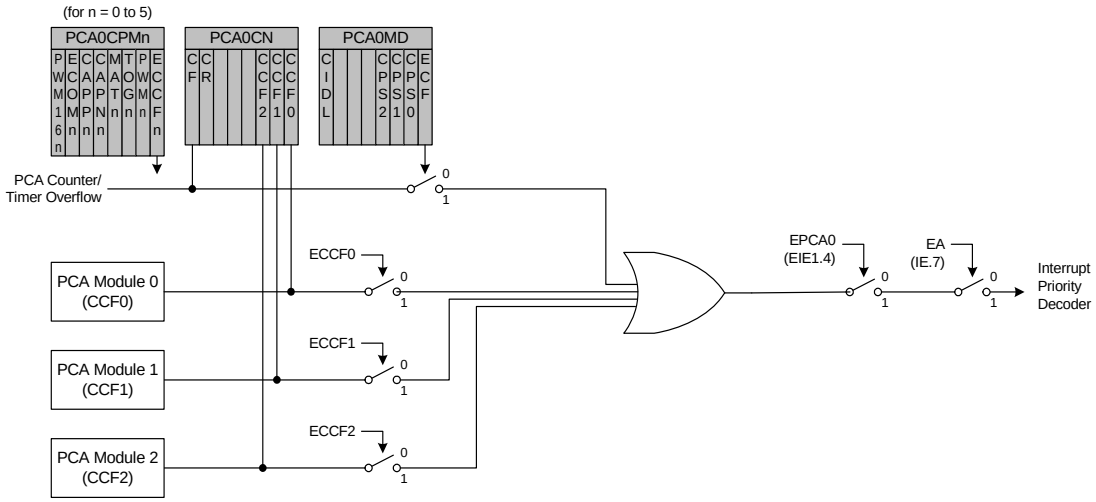

Figure 19.3. PCA Interrupt Block Diagram

Document Change List

Revision 0.3 to 0.4

- Updated all specification tables.
- Added 'F52xA and 'F53xA information.
- Updated the Selectable Gain section in the ADC section.
- Updated the External Crystal Example in the Oscillators section.
- Updated the LIN section.

Revision 0.4 to 0.5

- Updated all specification tables.
- Updated Figures 1.1, 1.2, 1.3, and 1.4.
- Updated Section 4 pinout diagrams and tables.

Revision 0.5 to 1.0

- Updated all specification tables and moved them to one section.
- Added Figure 3.1 and Figure 3.2.
- Updated Section 4 pinout diagrams and tables.
- Updated Figure 5.6.
- Added Figure 15.3.
- Updated equations in Section 17.
- Updated Figure 21.3.

Revision 1.0 to 1.1

- Updated Table 2.3, “ADC0 Electrical Characteristics,” on page 28 with new Burst Mode Oscillator specification, new Power Supply Current maximum, and made corrections to Temperature Sensor Offset and Offset Error conditions.
- Updated Table 2.9, “Flash Electrical Characteristics,” on page 33 with new Flash Write and Erase timing.
- Made correction in Equivalent Gain table in Section “4.4. Selectable Gain” on page 60.
- Updated Section “11.2. Power-Fail Reset / VDD Monitors (VDDMON0 and VDDMON1)” on page 108 regarding higher V_{DD} monitor threshold.

Revision 1.1 to 1.2

- Updated “Ordering Information” on page 14 and Table 1.1, “Product Selection Guide (Recommended for New Designs),” on page 14 to include -A (Automotive) devices and automotive qualification information.
- Updated Table 2.3, “ADC0 Electrical Characteristics,” on page 28 to include Temperature Sensor tracking time requirement and update INL maximum specification.
- Updated Figure 3.2. ’DFN-10 Package Diagram’ on page 38 with new Pin-1 detail drawing.
- Updated Table 8.1, “CIP-51 Instruction Set Summary,” on page 83 with correct CJNE and CPL timing.
- Updated “Power-Fail Reset / VDD Monitors (VDDMON0 and VDDMON1)” on page 108 to clarify the recommendations for the VDD monitor.

Note: All items from the C8051F52xA-F53xA Errata dated August 26, 2009 are incorporated into this data sheet.