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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | 8051 |
| Core Size | 8-Bit |
| Speed | 25MHz |
| Connectivity | LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT |
| Number of I/O | 16 |
| Program Memory Size | 2KB (2K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.25V |
| Data Converters | A/D 16x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-TSSOP (0.173", 4.40mm Width) |
| Supplier Device Package | 20-TSSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/c8051f536a-itr |

## 1.9. Port Input/Output

C8051F52x/F52xA/F53x/F53xA devices include up to 16 I/O pins. Port pins are organized as two byte-wide ports. The port pins behave like typical 8051 ports with a few enhancements. Each port pin can be configured as a digital or analog I/O pin. Pins selected as digital I/O can be configured for push-pull or open-drain operation. The “weak pullups” that are fixed on typical 8051 devices may be globally disabled to save power.

The Digital Crossbar allows mapping of internal digital system resources to port I/O pins. On-chip counter/timers, serial buses, hardware interrupts, and other digital signals can be configured to appear on the port pins using the Crossbar control registers. This allows the user to select the exact mix of general-purpose port I/O, digital, and analog resources needed for the application.

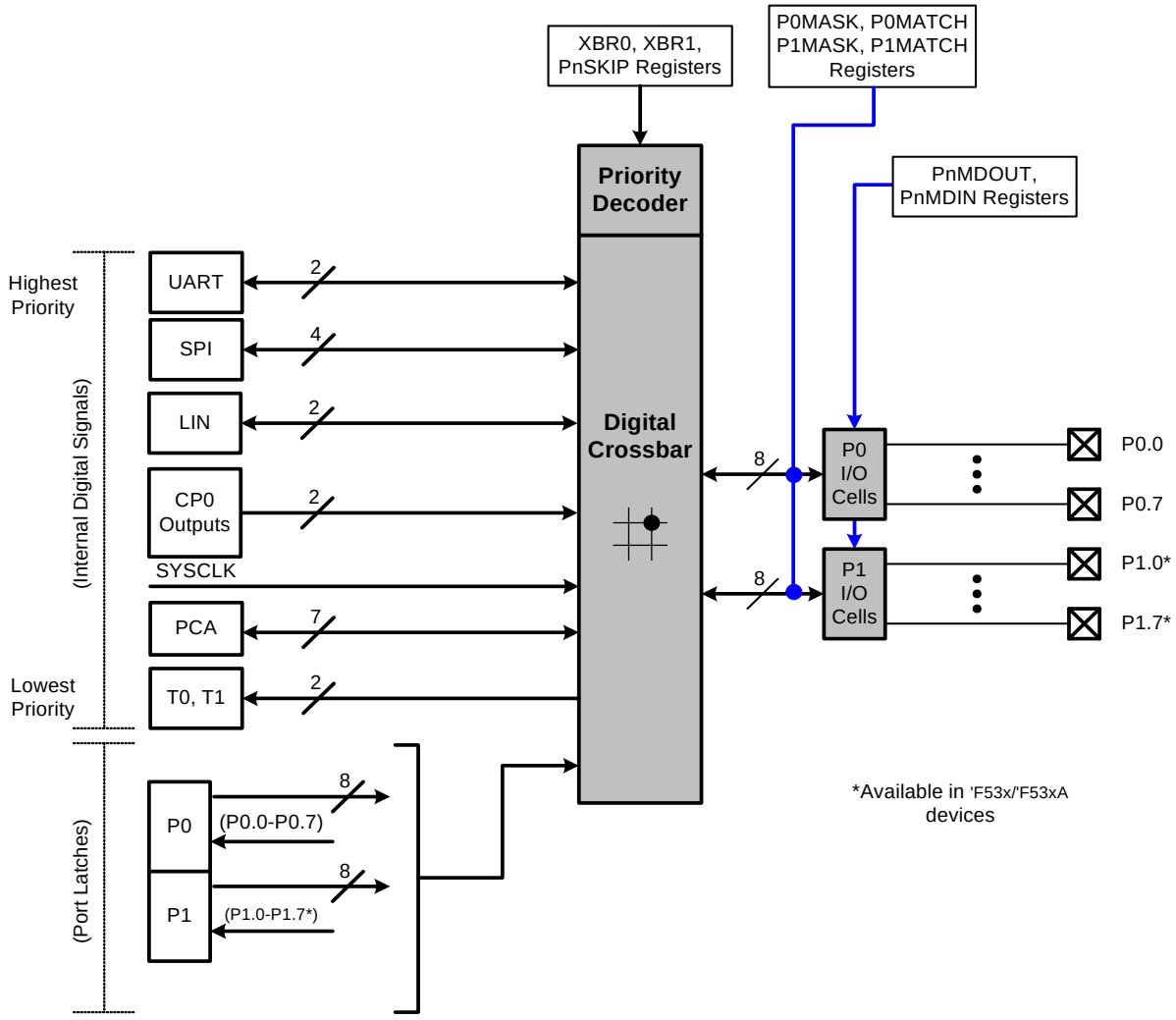


**Figure 1.9. Port I/O Functional Block Diagram**

**Table 2.6. Voltage Regulator Electrical Specifications**

$V_{DD}$ = 2.1 or 2.6 V; –40 to +125 °C unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Input Voltage Range ($V_{REGIN}$) | C8051F52x/53x | 2.7[1] | — | 5.25 | V |
| | C8051F52xA/53xA | | | | |
| | $V_{DD}$ connected to $V_{REGIN}$ | 1.8 | — | 2.7 | |
| | $V_{DD}$ not connected to $V_{REGIN}$ | 2.2[2] | — | 5.25 | |
| | C8051F52x-C/53x-C | | | | |
| | $V_{DD}$ connected to $V_{REGIN}$ | 2.0 | — | 2.75 | |
| | $V_{DD}$ not connected to $V_{REGIN}$ | 2.2[2] | — | 5.25 | |
| Dropout Voltage ($V_{DO}$) | Output Current = 1-50 mA | — | 10 | — | mV/mA |
| Output Voltage ($V_{DD}$) | Output Current = 1 to 50 mA | | | | V |
| | REG0MD = 0 | 2.0 | 2.1 | 2.25 | |
| | REG0MD = 1 | 2.5 | 2.6 | 2.75 | |
| Bias Current | 2.1 V operation (REG0MD = 0; T = 25 °C) | — | 1 | 5 | µA |
| | 2.6 V operation (REG0MD = 1; T = 25 °C) | — | 1 | 5 | |
| Dropout Indicator Detection Threshold | | — | 75 | — | mV |
| Output Voltage Temperature Coefficient | | — | 0.25 | — | mV/ºC |
| VREG Settling Time | 50 mA load with $V_{REGIN}$ = 2.4 V and $V_{DD}$ load capacitor of 4.8 µF | — | 250 | — | µs |

**Notes:**

1. The minimum input voltage is 2.7 V or $V_{DD}$ + $V_{DO}$(max load), whichever is greater.
2. The minimum input voltage is 2.2 V or $V_{DD}$ + $V_{DO}$(max load), whichever is greater.

### Table 2.7. Comparator Electrical Characteristics

$V_{REGIN}$ = 2.7–5.25 V, –40 to +125 °C unless otherwise noted.
All specifications apply to both Comparator0 and Comparator1 unless otherwise noted.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Response Time: Mode 0, Vcm[1] = 1.5 V | CP0+ – CP0– = 100 mV | — | 780 | — | ns |
| | CP0+ – CP0– = –100 mV | — | 980 | — | ns |
| Response Time: Mode 1, Vcm[1] = 1.5 V | CP0+ – CP0– = 100 mV | — | 850 | — | ns |
| | CP0+ – CP0– = –100 mV | — | 1120 | — | ns |
| Response Time: Mode 2, Vcm[1] = 1.5 V | CP0+ – CP0– = 100 mV | — | 870 | — | ns |
| | CP0+ – CP0– = –100 mV | — | 1310 | — | ns |
| Response Time: Mode 3, Vcm[1] = 1.5 V | CP0+ – CP0– = 100 mV | — | 1980 | — | ns |
| | CP0+ – CP0– = –100 mV | — | 4770 | — | ns |
| Common-Mode Rejection Ratio | | — | 3 | 9 | mV/V |
| Positive Hysteresis 1 | CP0HYP1-0 = 00 | — | 0.7 | 2 | mV |
| Positive Hysteresis 2 | CP0HYP1-0 = 01 | 2 | 5 | 10 | mV |
| Positive Hysteresis 3 | CP0HYP1-0 = 10 | 5 | 10 | 20 | mV |
| Positive Hysteresis 4 | CP0HYP1-0 = 11 | 13 | 20 | 40 | mV |
| Negative Hysteresis 1 | CP0HYN1-0 = 00 | — | 0.7 | 2 | mV |
| Negative Hysteresis 2 | CP0HYN1-0 = 01 | 2 | 5 | 10 | mV |
| Negative Hysteresis 3 | CP0HYN1-0 = 10 | 5 | 10 | 20 | mV |
| Negative Hysteresis 4 | CP0HYN1-0 = 11 | 13 | 20 | 40 | mV |
| Inverting or Non-Inverting Input Voltage Range[2] | | –0.25 | — | $V_{DD}$ + 0.25 | V |
| Input Capacitance[2] | | — | 4 | — | pF |
| Input Bias Current | | — | 0.5 | — | nA |
| Input Offset Voltage | | –15 | — | 15 | mV |
| Input Impedance | | — | 1.5 | — | kΩ |
| **Power Supply** | | | | | |
| Power Supply Rejection[2] | | — | 0.2 | 4 | mV/V |
| Power-up Time | | — | 2.3 | — | µs |
| Supply Current at DC | Mode 0 | — | 6 | 30 | µA |
| | Mode 1 | — | 3 | 15 | µA |
| | Mode 2 | — | 2 | 7.5 | µA |
| | Mode 3 | — | 0.3 | 3.8 | µA |

**Notes:**
1. Vcm is the common-mode voltage on CP0+ and CP0–.
2. Guaranteed by design and/or characterization.

## 4.2. Temperature Sensor

An on-chip temperature sensor is included on the C8051F52x/F52xA/F53x/F53xA devices which can be directly accessed via the ADC0 multiplexer. To use ADC0 to measure the temperature sensor, the ADC multiplexer channel should be configured to connect to the temperature sensor. The temperature sensor transfer function is shown in Figure 5.2. The output voltage ($V_{TEMP}$) is the positive ADC input selected by bits AD0MX[4:0] in register ADC0MX. The TEMPE bit in register REF0CN enables/disables the temperature sensor, as described in SFR Definition 5.1. While disabled, the temperature sensor defaults to a high impedance state and any ADC measurements performed on the sensor will result in meaningless data. Refer to Table 5.1 for the slope and offset parameters of the temperature sensor.

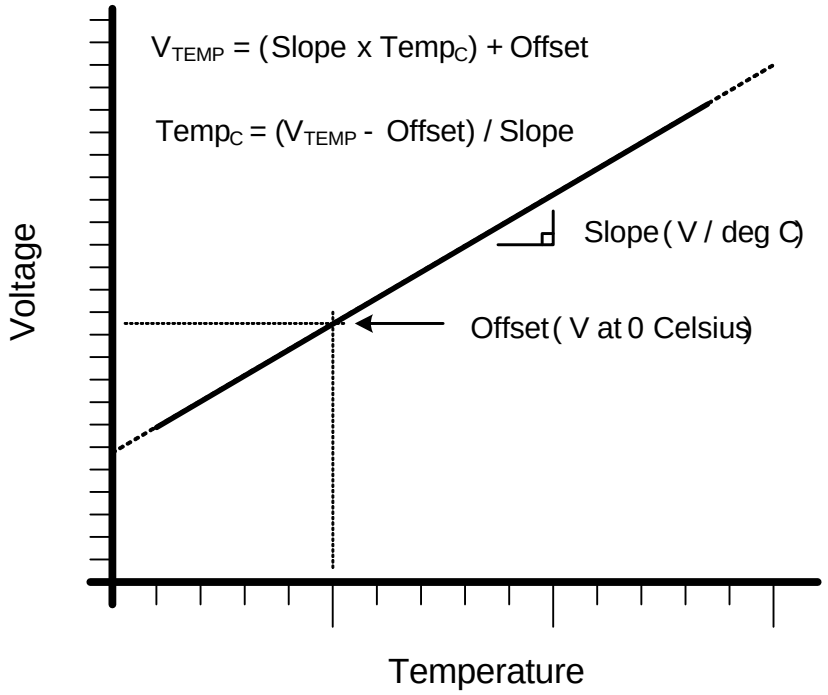


**Figure 4.2. Typical Temperature Sensor Transfer Function**

## SFR Definition 4.8. ADC0CN: ADC0 Control

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| AD0EN | BURSTEN | AD0INT | AD0BUSY | AD0WINT | AD0LJST | AD0CM1 | AD0CM0 | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | SFR Address: |
| | | | | | | | (bit addressable) | 0xE8 |

**Bit7**: **AD0EN**: ADC0 Enable Bit.
0: ADC0 Disabled. ADC0 is in low-power shutdown.
1: ADC0 Enabled. ADC0 is active and ready for data conversions.

**Bit6**: **BURSTEN**: ADC0 Burst Mode Enable Bit.
0: ADC0 Burst Mode Disabled.
1: ADC0 Burst Mode Enabled.

**Bit5**: **AD0INT**: ADC0 Conversion Complete Interrupt Flag.
0: ADC0 has not completed a data conversion since the last time AD0INT was cleared.
1: ADC0 has completed a data conversion.

**Bit4**: **AD0BUSY**: ADC0 Busy Bit.
Read:
0: ADC0 conversion is complete or a conversion is not currently in progress. AD0INT is set to logic 1 on the falling edge of AD0BUSY.
1: ADC0 conversion is in progress.
Write:
0: No Effect.
1: Initiates ADC0 Conversion if AD0CM1–0 = 00b

**Bit3**: **AD0WINT**: ADC0 Window Compare Interrupt Flag.
This bit must be cleared by software.
0: ADC0 Window Comparison Data match has not occurred since this flag was last cleared.
1: ADC0 Window Comparison Data match has occurred.

**Bit2**: **AD0LJST**: ADC0 Left Justify Select
0: Data in ADC0H:ADC0L registers is right justified.
1: Data in ADC0H:ADC0L registers is left justified. This option should not be used with a repeat count greater than 1 (when AD0RPT1–0 is 01b, 10b, or 11b).

**Bits1–0**: **AD0CM1–0**: ADC0 Start of Conversion Mode Select.
00: ADC0 conversion initiated on every write of 1 to AD0BUSY.
01: ADC0 conversion initiated on overflow of Timer 1.
10: ADC0 conversion initiated on rising edge of external CNVSTR.
11: ADC0 conversion initiated on overflow of Timer 2.

## SFR Definition 4.12. ADC0LTH: ADC0 Less-Than Data High Byte

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | SFR Address: 0xC6 |

**Bits7–0**: High byte of ADC0 Less-Than Data Word.

## SFR Definition 4.13. ADC0LTL: ADC0 Less-Than Data Low Byte

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | SFR Address: 0xC5 |

**Bits7–0**: Low byte of ADC0 Less-Than Data Word.

### 4.5.1. Window Detector In Single-Ended Mode

Figure 4.7 shows two example window comparisons for right-justified data with ADC0LTH:ADC0LTL = 0x0200 (512d) and ADC0GTH:ADC0GTL = 0x0100 (256d). The input voltage can range from 0 to $V_{REF}$ x (4095/4096) with respect to GND, and is represented by a 12-bit unsigned integer value. The repeat count is set to one. In the left example, an AD0WINT interrupt will be generated if the ADC0 conversion word (ADC0H:ADC0L) is within the range defined by ADC0GTH:ADC0GTL and ADC0LTH:ADC0LTL (if 0x0100 < ADC0H:ADC0L < 0x0200). In the right example, and AD0WINT interrupt will be generated if the ADC0 conversion word is outside of the range defined by the ADC0GT and ADC0LT registers (if ADC0H:ADC0L < 0x0100 or ADC0H:ADC0L > 0x0200). Figure 4.8 shows an example using left-justified data with the same comparison values.

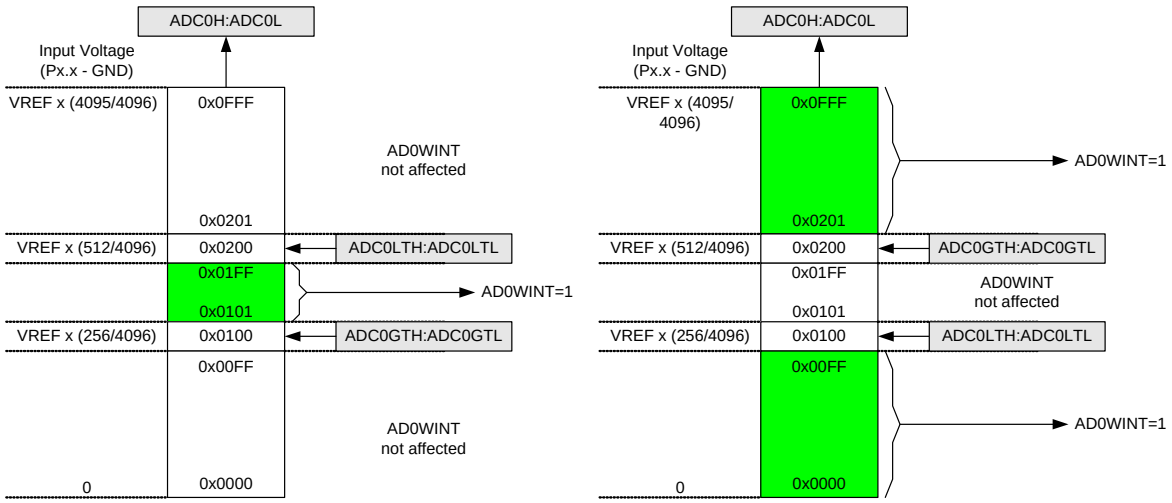


**Figure 4.7. ADC Window Compare Example: Right-Justified Single-Ended Data**

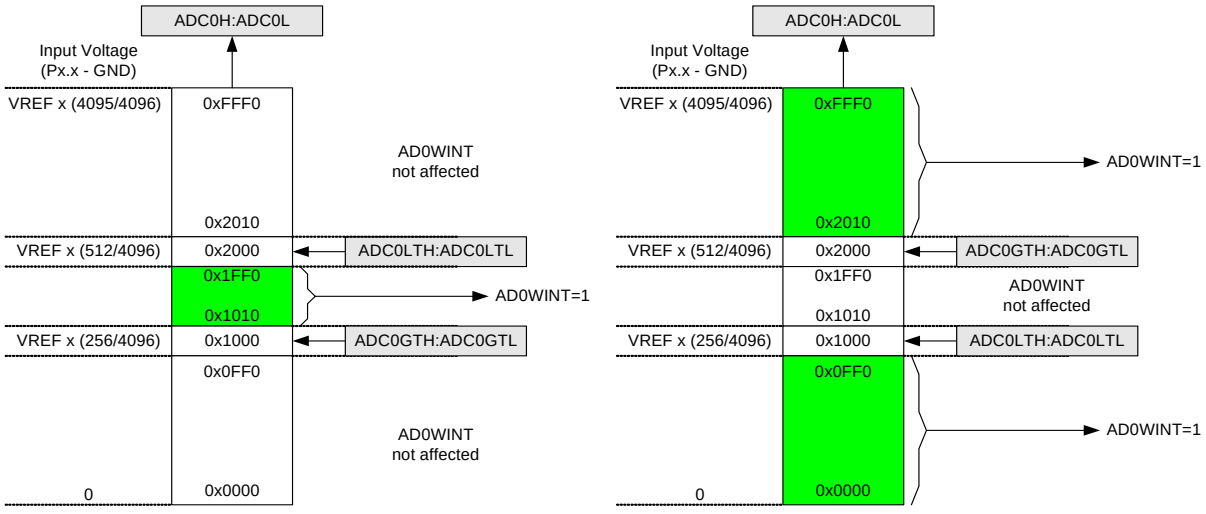


**Figure 4.8. ADC Window Compare Example: Left-Justified Single-Ended Data**

### 8.3.1. Idle Mode

Setting the Idle Mode Select bit (PCON.0) causes the CIP-51 to halt the CPU and enter Idle mode as soon as the instruction that sets the bit completes execution. All internal registers and memory maintain their original data. All analog and digital peripherals can remain active during Idle mode.

Idle mode is terminated when an enabled interrupt is asserted or a reset occurs. The assertion of an enabled interrupt will cause the Idle Mode Selection bit (PCON.0) to be cleared and the CPU to resume operation. The pending interrupt will be serviced and the next instruction to be executed after the return from interrupt (RETI) will be the instruction immediately following the one that set the Idle Mode Select bit. If Idle mode is terminated by an internal or external reset, the CIP-51 performs a normal reset sequence and begins program execution at address 0x0000.

If enabled, the Watchdog Timer (WDT) will eventually cause an internal watchdog reset and thereby terminate the Idle mode. This feature protects the system from an unintended permanent shutdown in the event of an inadvertent write to the PCON register. If this behavior is not desired, the WDT may be disabled by software prior to entering the Idle mode if the WDT was initially configured to allow this operation. This provides the opportunity for additional power savings, allowing the system to remain in the Idle mode indefinitely, waiting for an external stimulus to wake up the system.

### 8.3.2. Stop Mode

Setting the Stop Mode Select bit (PCON.1) causes the CIP-51 to enter Stop mode as soon as the instruction that sets the bit completes execution. In Stop mode the internal oscillator, CPU, and all digital peripherals are stopped; the state of the external oscillator circuit is not affected. Each analog peripheral (including the external oscillator circuit) may be shut down individually prior to entering Stop Mode. Stop mode can only be terminated by an internal or external reset. On reset, the CIP-51 performs the normal reset sequence and begins program execution at address 0x0000.

If enabled, the Missing Clock Detector will cause an internal reset and thereby terminate the Stop mode. The Missing Clock Detector should be disabled if the CPU is to be put to in STOP mode for longer than the MCD timeout period of 100 µs.

### 8.3.3. Suspend Mode

The C8051F52x/F52xA/F53x/F53xA devices feature a low-power Suspend mode, which stops the internal oscillator until a wakening event occurs. See Section Section “14.1.1. Internal Oscillator Suspend Mode” on page 136 for more information.

Note: When entering Suspend mode, firmware must set the ZTCEN bit in REF0CN (SFR Definition 5.1).

## SFR Definition 10.4. EIP1: Extended Interrupt Priority 1

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| PMAT | PREG0 | PLIN | PCPR | PCPF | PPAC0 | PREG0 | PWADC0 | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |

SFR Address: 0xF6

**Bit7**: **PMAT**. Port Match Interrupt Priority Control.
This bit sets the priority of the Port Match interrupt.
0: Port Match interrupt set to low priority level.
1: Port Match interrupt set to high priority level.

**Bit6**: **PREG0**: Voltage Regulator Interrupt Priority Control.
This bit sets the priority of the Voltage Regulator interrupt.
0: Voltage Regulator interrupt set to low priority level.
1: Voltage Regulator interrupt set to high priority level.

**Bit5**: **PLIN**: LIN Interrupt Priority Control.
This bit sets the priority of the CP0 interrupt.
0: LIN interrupt set to low priority level.
1: LIN interrupt set to high priority level.

**Bit4**: **PCPR**: Comparator Rising Edge Interrupt Priority Control.
This bit sets the priority of the Rising Edge Comparator interrupt.
0: Comparator interrupt set to low priority level.
1: Comparator interrupt set to high priority level.

**Bit3**: **PCPF**: Comparator falling Edge Interrupt Priority Control.
This bit sets the priority of the Falling Edge Comparator interrupt.
0: Comparator interrupt set to low priority level.
1: Comparator interrupt set to high priority level.

**Bit2**: **PPAC0**: Programmable Counter Array (PCA0) Interrupt Priority Control.
This bit sets the priority of the PCA0 interrupt.
0: PCA0 interrupt set to low priority level.
1: PCA0 interrupt set to high priority level.

**Bit1**: **PREG0**: ADC0 Conversion Complete Interrupt Priority Control.
This bit sets the priority of the ADC0 Conversion Complete interrupt.
0: ADC0 Conversion Complete interrupt set to low priority level.
1: ADC0 Conversion Complete interrupt set to high priority level.

**Bit0**: **PWADC0**: ADC0 Window Comparison Interrupt Priority Control.
This bit sets the priority of the ADC0 Window Comparison interrupt.
0: ADC0 Window Comparison interrupt set to low priority level.
1: ADC0 Window Comparison interrupt set to high priority level.

## SFR Definition 10.5. IT01CF: INT0/INT1 Configuration

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| IN1PL | IN1SL2 | IN1SL1 | IN1SL0 | IN0PL | IN0SL2 | IN0SL1 | IN0SL0 | 00000001 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |

SFR Address: 0xE4

Note: Refer to SFR Definition 18.1. "TCON: Timer Control" on page 186 for INT0/1 edge- or level-sensitive interrupt selection.

**Bit 7:** **IN1PL**: $\overline{\text{INT0}}$ Polarity
0: $\overline{\text{INT0}}$ input is active low.
1: $\overline{\text{INT0}}$ input is active high.

**Bits 6–4**: **IN1SL2–0**: $\overline{\text{INT0}}$ Port Pin Selection Bits
These bits select which Port pin is assigned to $\overline{\text{INT0}}$. Note that this pin assignment is independent of the Crossbar; $\overline{\text{INT0}}$ will monitor the assigned Port pin without disturbing the peripheral that has been assigned the Port pin via the Crossbar. The Crossbar will not assign the Port pin to a peripheral if it is configured to skip the selected pin (accomplished by setting to 1 the corresponding bit in register P0SKIP).

| IN1SL2-0 | $\overline{\text{INT1}}$ Port Pin |
|---|---|
| 000 | P0.0 |
| 001 | P0.1 |
| 010 | P0.2 |
| 011 | P0.3 |
| 100 | P0.4 |
| 101 | P0.5 |
| 110 | P0.6* |
| 111 | P0.7* |
| **Note:** Available in the C80151F53x/C8051F53xA parts. | |

**Bit 3**: **IN0PL**: $\overline{\text{INT0}}$ Polarity
0: $\overline{\text{INT0}}$ interrupt is active low.
1: $\overline{\text{INT0}}$ interrupt is active high.

**Bits 2–0**: **INT0SL2–0**: $\overline{\text{INT0}}$ Port Pin Selection Bits
These bits select which Port pin is assigned to $\overline{\text{INT0}}$. Note that this pin assignment is independent of the Crossbar. $\overline{\text{INT0}}$ will monitor the assigned Port pin without disturbing the peripheral that has been assigned the Port pin via the Crossbar. The Crossbar will not assign the Port pin to a peripheral if it is configured to skip the selected pin (accomplished by setting to 1 the corresponding bit in register P0SKIP).

| IN0SL2-0 | $\overline{\text{INT0}}$ Port Pin |
|---|---|
| 000 | P0.0 |
| 001 | P0.1 |
| 010 | P0.2 |
| 011 | P0.3 |
| 100 | P0.4 |
| 101 | P0.5 |
| 110 | P0.6* |
| 111 | P0.7* |
| **Note:** Available in the C80151F53x/C8051F53xA parts. | |

### SFR Definition 13.2. XBR1: Port I/O Crossbar Register 1

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| WEAKPUD | XBARE | T1E | T0E | ECIE | Reserved | PCA0ME | | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |

SFR Address: 0xE2

**Bit7**: **WEAKPUD**: Port I/O Weak Pullup Disable.
0: Weak Pullups enabled (except for Ports whose I/O are configured as analog input).
1: Weak Pullups disabled.
**Bit6**: **XBARE**: Crossbar Enable.
0: Crossbar disabled.
1: Crossbar enabled.
**Bit5**: **T1E**: T1 Enable
0: T1 unavailable at Port pin.
1: T1 routed to Port pin.
**Bit4**: **T0E**: T0 Enable
0: T0 unavailable at Port pin.
1: T0 routed to Port pin.
**Bit3**: **ECIE**: PCA0 External Counter Input Enable
0: ECI unavailable at Port pin.
1: ECI routed to Port pin.
**Bit2**: **Reserved**. Must Write 0b.
**Bits1–0**: **PCA0ME**: PCA Module I/O Enable Bits.
00: All PCA I/O unavailable at Port pins.
01: CEX0 routed to Port pin.
10: CEX0, CEX1 routed to Port pins.
11: CEX0, CEX1, CEX2 routed to Port pins.

## 13.3. General Purpose Port I/O

Port pins that remain unassigned by the Crossbar and are not used by analog peripherals can be used for general purpose I/O. Ports P0–P1 are accessed through corresponding special function registers (SFRs) that are both byte addressable and bit addressable. When writing to a Port, the value written to the SFR is latched to maintain the output data value at each pin. When reading, the logic levels of the Port's input pins are returned regardless of the XBRn settings (i.e., even when the pin is assigned to another signal by the Crossbar, the Port register can always read its corresponding Port I/O pin). The exception to this is the execution of the read-modify-write instructions that target a Port Latch register as the destination. The read-modify-write instructions when operating on a Port SFR are the following: ANL, ORL, XRL, JBC, CPL, INC, DEC, DJNZ and MOV, CLR or SETB, when the destination is an individual bit in a Port SFR. For these instructions, the value of the latch register (not the pin) is read, modified, and written back to the SFR.

## SFR Definition 13.11. P1MDOUT: Port1 Output Mode

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |

SFR Address: 0xA5

**Bits7–0**: Output Configuration Bits for P1.7–P1.0 (respectively): ignored if corresponding bit in register P1MDIN is logic 0.
0: Corresponding P1.n Output is open-drain.
1: Corresponding P1.n Output is push-pull.

**Note:** When SDA and SCL appear on any of the Port I/O, each are open-drain regardless of the value of P0MDOUT.

## SFR Definition 13.12. P1SKIP: Port1 Skip

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |

SFR Address: 0xD5

**Bits7–0**: **P1SKIP[7:0]**: Port1 Crossbar Skip Enable Bits.
These bits select Port pins to be skipped by the Crossbar Decoder. Port pins used as analog inputs (for ADC or Comparator) or used as special functions ($V_{REF}$ input, external oscillator circuit, CNVSTR input) should be skipped by the Crossbar.
0: Corresponding P1.n pin is not skipped by the Crossbar.
1: Corresponding P1.n pin is skipped by the Crossbar.

# 14. Oscillators

C8051F52x/F52xA/F53x/F53xA devices include a programmable internal oscillator, an external oscillator drive circuit. The internal oscillator can be enabled/disabled and calibrated using the OSCICN and OSCICL registers, as shown in Figure 14.1. The system clock (SYSCLK) can be derived from the internal oscillator, external oscillator circuit. Oscillator electrical specifications are given in Table 2.11 on page 34.

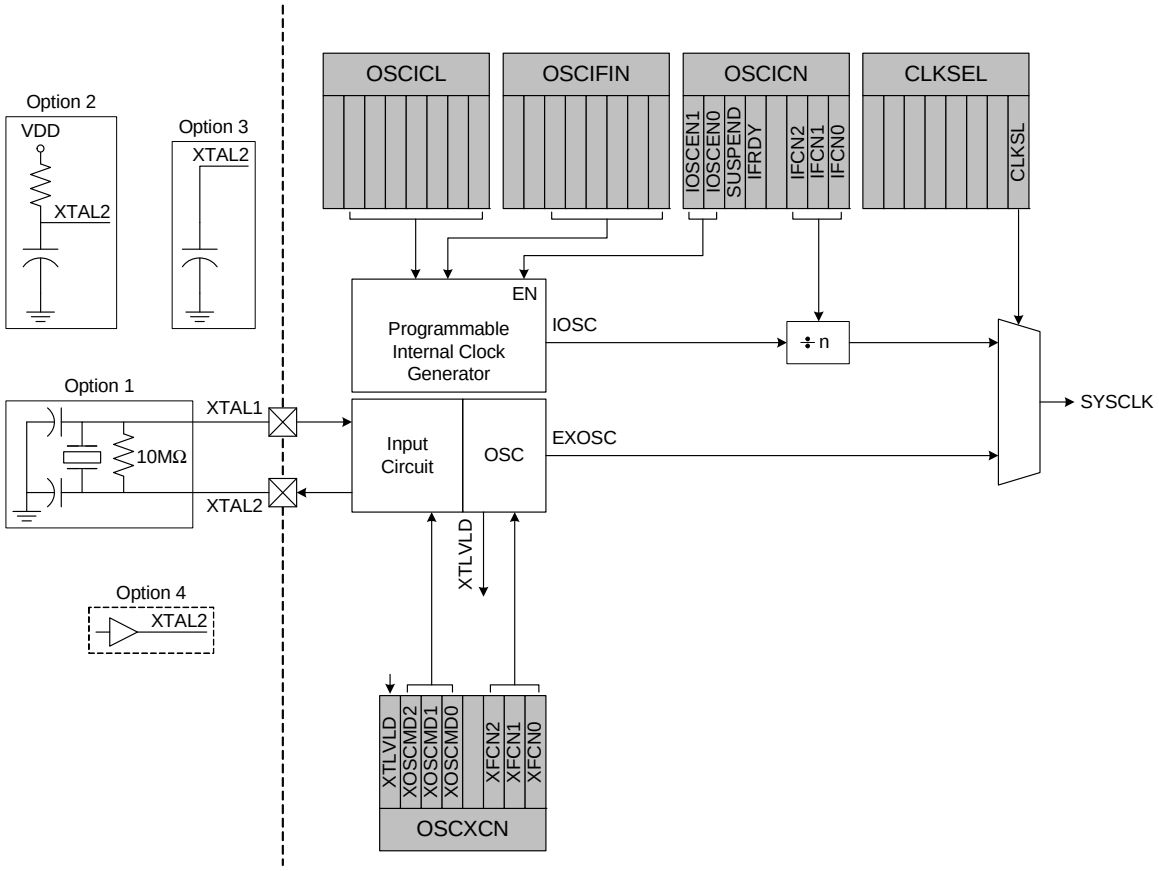


**Figure 14.1. Oscillator Diagram**

## 14.1. Programmable Internal Oscillator

All C8051F52x/53x devices include a programmable internal oscillator that defaults as the system clock after a system reset. The internal oscillator period can be programmed via the OSCICL and OSCIFIN registers, shown in SFR Definition 14.2 and SFR Definition 14.3. On C8051F52x/53x devices, OSCICL and OSCIFIN are factory calibrated to obtain a 24.5 MHz frequency.

Electrical specifications for the precision internal oscillator are given in Table 2.11 on page 34. Note that the system clock may be derived from the programmed internal oscillator divided by 1, 2, 4, 8, 16, 32, 64, or 128 as defined by the IFCN bits in register OSCICN. The divide value defaults to 128 following a reset.

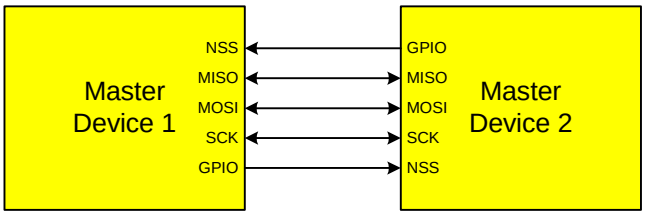


**Figure 16.2. Multiple-Master Mode Connection Diagram**

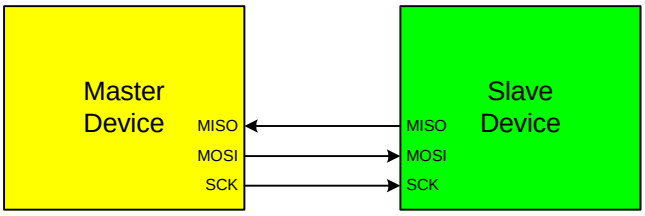


**Figure 16.3. 3-Wire Single Master and Slave Mode Connection Diagram**

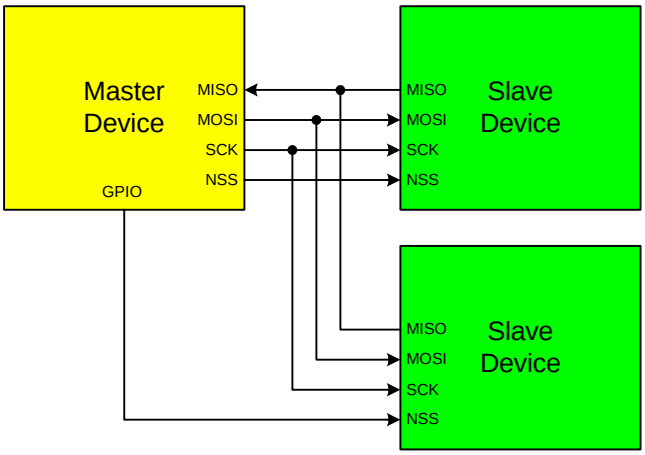


**Figure 16.4. 4-Wire Single Master and Slave Mode Connection Diagram**

## 16.3. SPI0 Slave Mode Operation

When SPI0 is enabled and not configured as a master, it will operate as a SPI slave. As a slave, bytes are shifted in through the MOSI pin and out through the MISO pin by a master device controlling the SCK signal. A bit counter in the SPI0 logic counts SCK edges. When 8 bits have been shifted into the shift register, the SPIF flag is set to logic 1, and the byte is copied into the receive buffer. Data is read from the receive buffer by reading SPI0DAT. A slave device cannot initiate transfers. Data to be transferred to the master device is pre-loaded into the shift register by writing to SPI0DAT. Writes to SPI0DAT are double-buffered, and are placed in the transmit buffer first. If the shift register is empty, the contents of the transmit buffer will immediately be transferred into the shift register. When the shift register already contains data, the SPI will load the shift register with the transmit buffer's contents after the last SCK edge of the next (or current) SPI transfer.

## 17.4. LIN Slave Mode Operation

When the device is configured for slave mode operation, it must wait for a command from a master node. Access from the firmware to data buffer and ID registers of the LIN peripheral is only possible when a data request is pending (DTREQ bit (LIN0ST.4) is 1) and also when the LIN bus is not active (ACTIVE bit (LIN0ST.7) is set to 0).

The LIN peripheral in slave mode detects the header of the message frame sent by the LIN master. If slave synchronization is enabled (autobaud), the slave synchronizes its internal bit time to the master bit time.

The LIN peripheral configured for slave mode will generated an interrupt in one of three situations:

1. After the reception of the IDENTIFIER FIELD.
2. When an error is detected.
3. When the message transfer is completed.

The application should perform the following steps when an interrupt is detected:

1. Check the status of the DTREQ bit (LIN0ST.4). This bit is set when the IDENTIFIER FIELD has been received.
2. If DTREQ (LIN0ST.4) is set, read the identifier from LIN0ID and process it. If DTREQ (LIN0ST.4) is not set, continue to step 7.
3. Set the TXRX bit (LIN0CTRL.5) to 1 if the current frame is a transmit operation for the slave and set to 0 if the current frame is a receive operation for the slave.
4. Load the data length into LIN0SIZE.
5. For a slave transmit operation, load the data to transmit into the data buffer.
6. Set the DTACK bit (LIN0CTRL.4). Continue to step 10.
7. If DTREQ (LIN0ST.4) is not set, check the DONE bit (LIN0ST.0). The transmission was successful if the DONE bit is set.
8. If the transmission was successful and the current frame was a receive operation for the slave, load the received data bytes from the data buffer.
9. If the transmission was not successful, check LIN0ERR to determine the nature of the error. Further error handling has to be done by the application.
10. Set the RSTINT (LIN0CTRL.3) and RSTERR bits (LIN0CTRL.2) to reset the interrupt request and the error flags.

In addition to these steps, the application should be aware of the following:

1. If the current frame is a transmit operation for the slave, steps 1 through 5 must be completed during the IN-FRAME RESPONSE SPACE. If it is not completed in time, a timeout will be detected by the master.
2. If the current frame is a receive operation for the slave, steps 1 through 5 have to be finished until the reception of the first byte after the IDENTIFIER FIELD. Otherwise, the internal receive buffer of the LIN peripheral will be overwritten and a timeout error will be detected in the LIN peripheral.
3. The LIN module does not directly support LIN Version 1.3 Extended Frames. If the application detects an unknown identifier (e.g. extended identifier), it has to write a 1 to the STOP bit (LIN0CTRL.7) instead of setting the DTACK (LIN0CTRL.4) bit. At that time, steps 2 through 5 can then be skipped. In this situation, the LIN peripheral stops the processing of the LIN communication until the next SYNC BREAK is received.
4. Changing the configuration of the checksum during a transaction will cause the interface to reset and the transaction to be lost. To prevent this, the checksum should not be configured while a transaction is

in progress. The same applies to changes in the LIN interface mode from slave mode to master mode and from master mode to slave mode.

## 17.5. Sleep Mode and Wake-Up

To reduce the system's power consumption, the LIN Protocol Specification defines a Sleep Mode. The message used to broadcast a Sleep Mode request must be transmitted by the LIN master application in the same way as a normal transmit message. The LIN slave application must decode the Sleep Mode Frame from the Identifier and data bytes. After that, the LIN slave node must be put into the Sleep Mode by setting the SLEEP bit (LIN0CTRL.6).

If the SLEEP bit (LIN0CTRL.6) of the LIN slave application is not set and there is no bus activity for four seconds (specified bus idle timeout), the IDLTOUT bit (LIN0ST.6) is set and an interrupt request is generated. After that the application may assume that the LIN bus is in Sleep Mode and set the SLEEP bit (LIN0CTRL.6).

Sending a Wakeup signal from the master or any slave node terminates the Sleep Mode of the LIN bus. To send a Wakeup signal, the application has to set the WUPREQ bit (LIN0CTRL.1). After successful transmission of the wakeup signal, the DONE bit (LIN0ST.0) of the master node is set and an interrupt request is generated. The LIN slave does not generate an interrupt request after successful transmission of the Wakeup signal but it generates an interrupt request if the master does not respond to the Wakeup signal within 150 milliseconds. In that case, the ERROR bit (LIN0ST.2) and TOUT bit (LIN0ERR.2) are set. The application then has to decide whether or not to transmit another Wakeup signal.

All LIN nodes that detect a wakeup signal will set the WAKEUP (LIN0ST.1) and DONE bits (LIN0ST.0) and generate an interrupt request. After that, the application has to clear the SLEEP bit (LIN0CTRL.6) in the LIN slave.

## 17.6. Error Detection and Handling

The LIN peripheral generates an interrupt request and stops the processing of the current frame if it detects an error. The application has to check the type of error by processing LIN0ERR. After that, it has to reset the error register and the ERROR bit (LIN0ST.2) by writing a 1 to the RSTERR bit (LIN0CTRL.2). Starting a new message with the LIN peripheral selected as master or sending a Wakeup signal with the LIN peripheral selected as a master or slave is possible only if ERROR bit (LIN0ST.2) is set to 0.

## SFR Definition 17.3. LINCF Control Mode Register

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| LINEN | MODE | ABAUD | | | | | | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |

SFR Address: 0x95

**Bit7**: **LINEN**: LIN Interface Enable bit
0: LIN0 is disabled.
1: LIN0 is enabled.

**Bit6**: **MODE**: LIN Mode Selection
0: LIN0 operates in Slave mode.
1: LIN0 operates in Master mode.

**Bit5**: **ABAUD**: LIN Mode Automatic Baud Rate Selection (**slave mode only**).
0: Manual baud rate selection is enabled.
1: Automatic baud rate selection is enabled.

## SFR Definition 17.12. LIN0CTRL: LIN0 Control Register

| W | W | W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| STOP | SLEEP | TXRX | DTACK | RSTINT | RSTERR | WUPREQ | STREQ | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |

Address: 0x08 (indirect)

**Bit7**: **STOP**: Stop Communication Processing Bit (**slave mode only**).
This bit is to be set by the application to block the processing of the LIN Communications until the next SYNCH BREAK signal. It is used when the application is handling a data request interrupt and cannot use the frame content with the received identifier (always reads 0).

**Bit6**: **SLEEP**: Sleep Mode Warning.
This bit is to be set by the application to warn the peripheral that a Sleep Mode Frame was received and that the Bus is in sleep mode or if a Bus Idle timeout interrupt is requested. The application must reset it when a Wake-Up interrupt is requested.

**Bit5**: **TXRX**: Transmit/Receive Selection Bit.
This bit determines if the current frame is a transmit frame or a receive frame.
0: Current frame is a receive operation.
1: Current frame is a transmit operation.

**Bit4**: **DTACK**: Data acknowledge bit (**slave mode only**).
Set to 1 after handling a data request interrupt to acknowledge the transfer. The bit will automatically be cleared to 0 by the LIN controller.

**Bit3**: **RSTINT**: Interrupt Reset bit.
This bit always reads as 0.
0: No effect.
1: Reset the LININT bit (LIN0ST.3).

**Bit2**: **RSTERR**: Error Reset Bit.
This bit always reads as 0.
0: No effect.
1: Reset the error bits in LIN0ST and LIN0ERR.

**Bit1**: **WUPREQ**: Wake-Up Request Bit.
Set to 1 to terminate sleep mode by sending a wakeup signal. The bit will automatically be cleared to 0 by the LIN controller.

**Bit0**: **STREQ**: Start Request Bit (**master mode only**).
1: Start a LIN transmission. This should be set only after loading the identifier, data length and data buffer if necessary.
The bit is reset to 0 upon transmission completion or error detection.

## SFR Definition 17.13. LIN0ST: LIN0 STATUS Register

| R | R | R | R | R/W | R | R | R | Reset Value |
|---|---|---|---|---|---|---|---|---|
| ACTIVE | IDLTOUT | ABORT | DTREQ | LININT | ERROR | WAKEUP | DONE | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |

Address: 0x09 (indirect)

**Bit7**: **ACTIVE**: LIN Bus Activity Bit.
0: No transmission activity detected on the LIN bus.
1: Transmission activity detected on the LIN bus.

**Bit6**: **IDLTOUT**: Bus Idle Timeout Bit (**slave mode only**).
0: The bus has not been idle for four seconds.
1: No bus activity has been detected for four seconds, but the bus is not yet in Sleep mode.

**Bit5**: **ABORT**: Aborted transmission signal (**slave mode only**).
0: The current transmission has not been interrupted or stopped. This bit is reset to 0 after receiving a SYNCH BREAK that does not interrupt a pending transmission.
1: New SYNCH BREAK detected before the end of the last transmission or the STOP bit (LIN0CTRL.7) has been set.

**Bit4**: **DTREQ**: Data Request bit (**slave mode only**).
0: Data identifier has not been received.
1: Data identifier has been received.

**Bit3**: **LININT**: Interrupt Request bit.
0: An interrupt is not pending. This bit is cleared by setting RSTINT (LIN0CTRL.3)
1: There is a pending LIN0 interrupt.

**Bit2**: **ERROR**: Communication Error Bit.
0: No error has been detected. This bit is cleared by setting RSTERR (LIN0CTRL.2)
1: An error has been detected.

**Bit1**: **WAKEUP**: Wakeup Bit.
0: A wakeup signal is not being transmitted and has not been received.
1: A wakeup signal is being transmitted or has been received.

**Bit0**: **DONE**: Transmission Complete Bit.
0: A transmission is not in progress or has not been started. This bit is cleared at the start of a transmission.
1: The current transmission is complete.