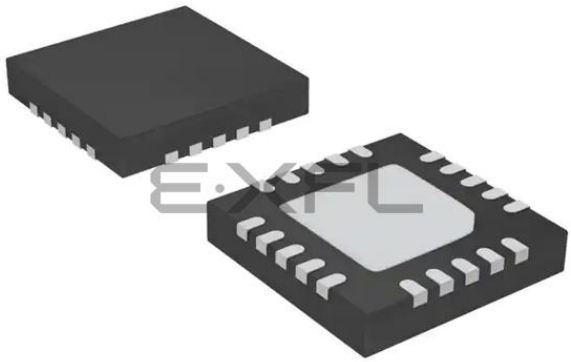

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | 8051 |
| Core Size | 8-Bit |
| Speed | 25MHz |
| Connectivity | SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT |
| Number of I/O | 16 |
| Program Memory Size | 2KB (2K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.25V |
| Data Converters | A/D 16x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-VFQFN Exposed Pad |
| Supplier Device Package | 20-QFN (4x4) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/c8051f537a-im |

## List of Registers

**Table 1.2. Product Selection Guide (Not Recommended for New Designs)**

| Ordering Part Number | Flash Memory (kB) | Port I/Os | LIN | Package | Ordering Part Number | Flash Memory (kB) | Port I/Os | LIN | Package |
|---|---|---|---|---|---|---|---|---|---|
| C8051F520-IM<br>C8051F520A-IM | 8 | 6 | ✓ | DFN-10 | C8051F534-IM<br>C8051F534A-IM | 4 | 16 | — | QFN-20 |
| C8051F521-IM<br>C8051F521A-IM | 8 | 6 | — | DFN-10 | C8051F536-IM<br>C8051F536A-IM | 2 | 16 | ✓ | QFN-20 |
| C8051F523-IM<br>C8051F523A-IM | 4 | 6 | ✓ | DFN-10 | C8051F537-IM<br>C8051F537A-IM | 2 | 16 | — | QFN-20 |
| C8051F524-IM<br>C8051F524A-IM | 4 | 6 | — | DFN-10 | C8051F530-IT<br>C8051F530A-IT | 8 | 16 | ✓ | TSSOP-20 |
| C8051F526-IM<br>C8051F526A-IM | 2 | 6 | ✓ | DFN-10 | C8051F531-IT<br>C8051F531A-IT | 8 | 16 | — | TSSOP-20 |
| C8051F527-IM<br>C8051F527A-IM | 2 | 6 | — | DFN-10 | C8051F533-IT<br>C8051F533A-IT | 4 | 16 | ✓ | TSSOP-20 |
| C8051F530-IM<br>C8051F530A-IM | 8 | 16 | ✓ | QFN-20 | C8051F534-IT<br>C8051F534A-IT | 4 | 16 | — | TSSOP-20 |
| C8051F531-IM<br>C8051F531A-IM | 8 | 16 | — | QFN-20 | C8051F536-IT<br>C8051F536A-IT | 2 | 16 | ✓ | TSSOP-20 |
| C8051F533-IM<br>C8051F533A-IM | 4 | 16 | ✓ | QFN-20 | C8051F537-IT<br>C8051F537A-IT | 2 | 16 | — | TSSOP-20 |

The part numbers in Table 1.2 are not recommended for new designs. Instead, select the corresponding part number from Table 1.1 (silicon revision C) for your design. In Table 1.2, the part numbers in the format similar to C8051F520-IM are silicon revision A devices. The part numbers in the format similar to C8051F520A-IM are silicon revision B devices.

## 1.2. CIP-51™ Microcontroller

### 1.2.1. Fully 8051 Compatible Instruction Set

The C8051F52x/F52xA/F53x/F53xA devices use Silicon Laboratories' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51™ instruction set. Standard 803x/805x assemblers and compilers can be used to develop software. The C8051F52x/F52xA/F53x/F53xA family has a superset of all the peripherals included with a standard 8052.

### 1.2.2. Improved Throughput

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute, and usually have a maximum system clock of 12-to-24 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with no instructions taking more than eight system clock cycles.

With the CIP-51's system clock running at 25 MHz, it has a peak throughput of 25 MIPS. The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

| Clocks to Execute | 1 | 2 | 2/3 | 3 | 3/4 | 4 | 4/5 | 5 | 8 |
|---|---|---|---|---|---|---|---|---|---|
| Number of Instructions | 26 | 50 | 5 | 14 | 7 | 3 | 1 | 2 | 1 |

### 1.2.3. Additional Features

The C8051F52x/F52xA/F53x/F53xA family includes several key enhancements to the CIP-51 core and peripherals to improve performance and ease of use in end applications.

An extended interrupt handler allows the numerous analog and digital peripherals to operate independently of the controller core and interrupt the controller only when necessary. By requiring less intervention from the microcontroller core, an interrupt-driven system is more efficient and allows for easier implementation of multi-tasking, real-time systems.

Eight reset sources are available: power-on reset circuitry (POR), an on-chip $V_{DD}$ monitor, a Watchdog Timer, a Missing Clock Detector, a voltage level detection from Comparator, a forced software reset, an external reset pin, and an illegal Flash access protection circuit. Each reset source except for the POR, Reset Input Pin, or Flash error may be disabled by the user in software. The WDT may be permanently enabled in software after a power-on reset during MCU initialization.

The internal oscillator is factory calibrated to 24.5 MHz ±0.5% across the entire operating temperature and voltage range. An external oscillator drive circuit is also included, allowing an external crystal, ceramic resonator, capacitor, RC, or CMOS clock source to generate the system clock.

### 1.2.4. On-Chip Debug Circuitry

The C8051F52x/F52xA/F53x/F53xA devices include on-chip Silicon Laboratories 2-Wire (C2) debug circuitry that provides non-intrusive, full speed, in-circuit debugging of the production part *installed in the end application.*

Silicon Laboratories' debugging system supports inspection and modification of memory and registers, breakpoints, and single stepping. No additional target RAM, program memory, timers, or communications channels are required. All the digital and analog peripherals are functional and work correctly while debugging. All the peripherals (except for the ADC) are stalled when the MCU is halted, during single stepping, or at a breakpoint in order to keep them synchronized.

The C8051F530DK development kit provides all the hardware and software necessary to develop application code and perform in-circuit debugging with the C8051F52x/F52xA/F53x/F53xA MCUs. The kit

## 2.2. Electrical Characteristics

### Table 2.2. Global DC Electrical Characteristics

–40 to +125 °C, 25 MHz System Clock unless otherwise specified. Typical values are given at 25 °C

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Supply Input Voltage ($V_{REGIN}$)[1] | Output Current ≤ 1 mA | | | | |
| | C8051F52x/53x | 2.7 | — | 5.25 | V |
| | C8051F52xA/53xA | 1.8[1] | — | 5.25 | V |
| | C8051F52x-C/53x-C | 2.0[1] | — | 5.25 | V |
| Digital Supply Voltage ($V_{DD}$) | C8051F52x/53x | 2.0 | — | 2.7 | V |
| | C8051F52xA/53xA | 1.8 | — | 2.7 | V |
| | C8051F52x-C/53x-C | 2.0 | — | 2.75 | V |
| Core Supply RAM Data Retention Voltage | | — | 1.5 | — | V |
| SYSCLK (System Clock)[2] | | 0 | — | 25 | MHz |
| Specified Operating Temperature Range | | –40 | — | +125 | °C |
| Digital Supply Current—CPU Active (Normal Mode, fetching instructions from Flash) | | | | | |
| $I_{DD}$[3,4] | **$V_{DD}$ = 2.1 V:** | | | | |
| | Clock = 32 kHz | — | 13 | — | µA |
| | Clock = 200 kHz | — | 60 | — | µA |
| | Clock = 1 MHz | — | 0.28 | — | mA |
| | Clock = 25 MHz | — | 5.1 | 9 | mA |
| | **$V_{DD}$ = 2.6 V:** | | | | |
| | Clock = 32 kHz | — | 22 | — | µA |
| | Clock = 200 kHz | — | 105 | — | µA |
| | Clock = 1 MHz | — | 0.5 | — | mA |
| | Clock = 25 MHz | — | 7.3 | 13 | mA |
| $I_{DD}$ Frequency Sensitivity[3,5] | T = 25 °C: | | | | |
| | $V_{DD}$ = 2.1 V, F ≤ 12 MHz | — | 0.276 | — | mA/MHz |
| | $V_{DD}$ = 2.1 V, F > 12 MHz | — | 0.140 | — | mA/MHz |
| | $V_{DD}$ = 2.6 V, F ≤ 12 MHz | — | 0.424 | — | mA/MHz |
| | $V_{DD}$ = 2.6 V, F > 12 MHz | — | 0.184 | — | mA/MHz |

**Notes:**

1. For more information on $V_{REGIN}$ characteristics, see Table 2.6 on page 30.
2. SYSCLK must be at least 32 kHz to enable debugging.
3. Based on device characterization data; Not production tested.
4. Does not include internal oscillator or internal regulator supply current.
5. $I_{DD}$ can be estimated for frequencies <= 12 MHz by multiplying the frequency of interest by the frequency sensitivity number for that range. When using these numbers to estimate $I_{DD}$ > 12 MHz, the estimate should be the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: $V_{DD}$ = 2.6 V; F= 20 MHz, $I_{DD}$ = 7.3 mA – (25 MHz – 20 MHz) x 0.184 mA/MHz = 6.38 mA.
6. Idle $I_{DD}$ can be estimated for frequencies <= 1 MHz by multiplying the frequency of interest by the frequency sensitivity number for that range. When using these numbers to estimate $I_{DD}$ > 1 MHz, the estimate should be the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: $V_{DD}$ = 2.6 V; F= 5 MHz, Idle $I_{DD}$ = 3 mA – (25 MHz– 5 MHz) x 118 µA/MHz = 0.64 mA.

# 4. 12-Bit ADC (ADC0)

The ADC0 on the C8051F52x/F52xA/F53x/F53xA Family consists of an analog multiplexer (AMUX0) with 16/6 total input selections, and a 200 ksps, 12-bit successive-approximation-register (SAR) ADC with integrated track-and-hold, programmable window detector, programmable gain, and hardware accumulator. The ADC0 subsystem has a special Burst Mode which can automatically enable ADC0, capture and accumulate samples, then place ADC0 in a low power shutdown mode without CPU intervention. The AMUX0, data conversion modes, and window detector are all configurable under software control via the Special Function Registers shown in Figure 4.1. ADC0 inputs are single-ended and may be configured to measure P0.0-P1.7, the Temperature Sensor output, $V_{DD}$, or GND with respect to GND. The voltage reference for the ADC is selected as described in Section “5. Voltage Reference” on page 72. ADC0 is enabled when the AD0EN bit in the ADC0 Control register (ADC0CN) is set to logic 1, or when performing conversions in Burst Mode. ADC0 is in low power shutdown when AD0EN is logic 0 and no Burst Mode conversions are taking place.

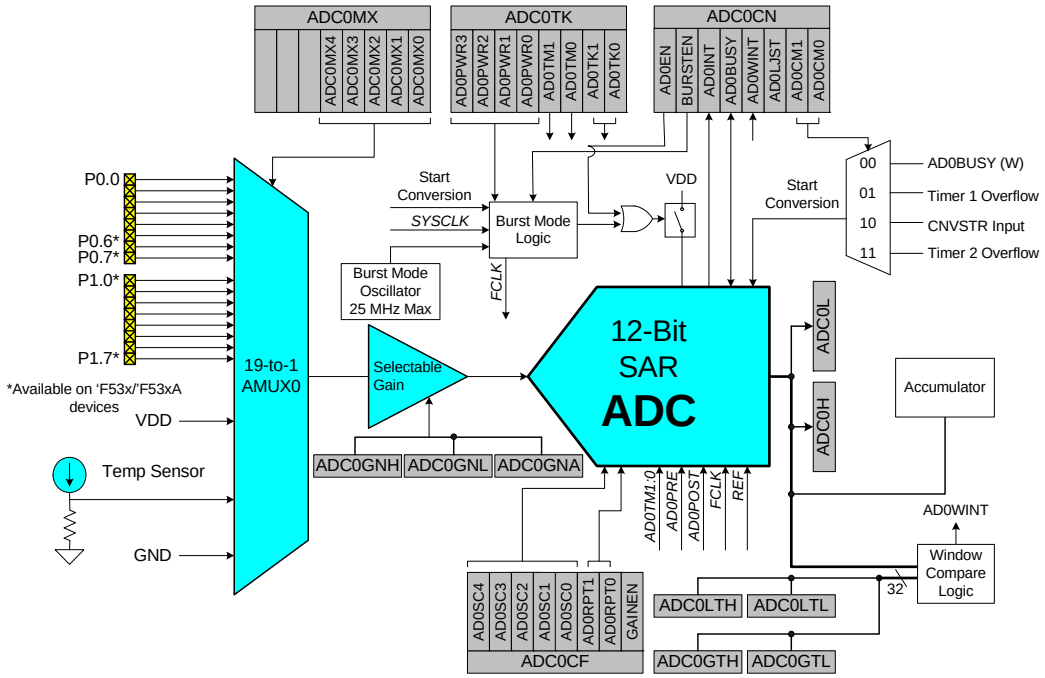



**Figure 4.1. ADC0 Functional Block Diagram**

## 4.1. Analog Multiplexer

AMUX0 selects the input channel to the ADC. Any of the following may be selected as an input: P0.0–P1.7, the on-chip temperature sensor, the core power supply ($V_{DD}$), or ground (GND). **ADC0 is single-ended and all signals measured are with respect to GND.** The ADC0 input channels are selected using the ADC0MX register as described in SFR Definition 4.4.

**Important Note About ADC0 Input Configuration:** Port pins selected as ADC0 inputs should be configured as analog inputs, and should be skipped by the Digital Crossbar. To configure a Port pin for analog input, set to 0 the corresponding bit in register PnMDIN (for n = 0,1). To force the Crossbar to skip a Port pin, set to 1 the corresponding bit in register PnSKIP (for n = 0,1). See Section “13. Port Input/Output” on page 120 for more Port I/O configuration details.

## 4.3. ADC0 Operation

In a typical system, ADC0 is configured using the following steps:

1. If a gain adjustment is required, refer to Section “4.4. Selectable Gain” on page 60.
2. Choose the start of conversion source.
3. Choose Normal Mode or Burst Mode operation.
4. If Burst Mode, choose the ADC0 Idle Power State and set the Power-Up Time.
5. Choose the tracking mode. Note that Pre-Tracking Mode can only be used with Normal Mode.
6. Calculate required settling time and set the post convert-start tracking time using the AD0TK bits.
7. Choose the repeat count.
8. Choose the output word justification (Right-Justified or Left-Justified).
9. Enable or disable the End of Conversion and Window Comparator Interrupts.

### 4.3.1. Starting a Conversion

A conversion can be initiated in one of four ways, depending on the programmed states of the ADC0 Start of Conversion Mode bits (AD0CM1–0) in register ADC0CN. Conversions may be initiated by one of the following:

- Writing a 1 to the AD0BUSY bit of register ADC0CN
- A rising edge on the CNVSTR input signal (pin P0.6)
- A Timer 1 overflow (i.e., timed continuous conversions)
- A Timer 2 overflow (i.e., timed continuous conversions)

Writing a 1 to AD0BUSY provides software control of ADC0 whereby conversions are performed "on-demand.” During conversion, the AD0BUSY bit is set to logic 1 and reset to logic 0 when the conversion is complete. The falling edge of AD0BUSY triggers an interrupt (when enabled) and sets the ADC0 interrupt flag (AD0INT). Note: When polling for ADC conversion completions, the ADC0 interrupt flag (AD0INT) should be used. Converted data is available in the ADC0 data registers, ADC0H:ADC0L, when bit AD0INT is logic 1. Note that when Timer 2 overflows are used as the conversion source, Low Byte overflows are used if Timer2 is in 8-bit mode; High byte overflows are used if Timer 2 is in 16-bit mode. See Section “18. Timers” on page 182 for timer configuration.

**Important Note:** The CNVSTR input pin also functions as Port pin P0.5 on C8051F52x/52xA devices and P1.2 on C8051F53x/53xA devices. When the CNVSTR input is used as the ADC0 conversion source, Port pin P0.5 or P1.2 should be skipped by the Digital Crossbar. To configure the Crossbar to skip P0.5 or P1.2, set to 1 to the appropriate bit in the PnSKIP register. See Section “13. Port Input/Output” on page 120 for details on Port I/O configuration.

### 4.3.2. Tracking Modes

Each ADC0 conversion must be preceded by a minimum tracking time for the converted result to be accurate, as shown in Table 2.3 on page 28. ADC0 has three tracking modes: Pre-Tracking, Post-Tracking, and Dual-Tracking. Pre-Tracking Mode provides the minimum delay between the convert start signal and end of conversion by tracking continuously before the convert start signal. This mode requires software management in order to meet minimum tracking requirements. In Post-Tracking Mode, a programmable tracking time starts after the convert start signal and is managed by hardware. Dual-Tracking Mode maximizes tracking time by tracking before and after the convert start signal. Figure 4.3 shows examples of the three tracking modes.

Pre-Tracking Mode is selected when AD0TM is set to 10b. Conversions are started immediately following the convert start signal. ADC0 is tracking continuously when not performing a conversion. Software must allow at least the minimum tracking time between each end of conversion and the next convert start signal. The minimum tracking time must also be met prior to the first convert start signal after ADC0 is enabled.

## SFR Definition 4.4. ADC0MX: ADC0 Channel Select

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| - | - | - | AD0MX | | | | | 00011111 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | SFR Address: |
| | | | | | | | | 0xBB |

**Bits7–5**: **UNUSED**. Read = 000b; Write = don't care.
**Bits4–0**: **AD0MX4–0**: AMUX0 Positive Input Selection

| AD0MX4–0 | ADC0 Input Channel |
|---|---|
| 00000 | P0.0 |
| 00001 | P0.1 |
| 00010 | P0.2 |
| 00011 | P0.3 |
| 00100 | P0.4 |
| 00101 | P0.5 |
| 00110 | P0.6* |
| 00111 | P0.7* |
| 01000 | P1.0* |
| 01001 | P1.1* |
| 01010 | P1.2* |
| 01011 | P1.3* |
| 01100 | P1.4* |
| 01101 | P1.5* |
| 01110 | P1.6* |
| 01111 | P1.7* |
| 11000 | Temp Sensor |
| 11001 | $V_{DD}$ |
| 11010 - 11111 | GND |

**Note:** Only applies to C8051F53x/C8051F53xA parts.

## 5. Voltage Reference

The Voltage reference MUX on C8051F52x/F52xA/F53x/F53xA devices is configurable to use an externally connected voltage reference, the internal reference voltage generator, or the $V_{DD}$ power supply voltage (see Figure 5.1). The REFSL bit in the Reference Control register (REF0CN) selects the reference source. For an external source or the internal reference applied to the $V_{REF}$ pin, REFSL should be set to 0. To use $V_{DD}$ as the reference source, REFSL should be set to 1.

The BIASE bit enables the internal voltage bias generator, which is used by the ADC, Temperature Sensor, and internal oscillators. This bit is forced to logic 1 when any of the aforementioned peripherals are enabled. The bias generator may be enabled manually by writing a 1 to the BIASE bit in register REF0CN; see SFR Definition 5.1 for REF0CN register details. The electrical specifications for the voltage reference circuit are given in Table 2.5 on page 29.

The internal voltage reference circuit consists of a temperature stable bandgap voltage reference generator and a gain-of-two output buffer amplifier. The output voltage is selectable between 1.5 V and 2.2 V. The internal voltage reference can be driven out on the $V_{REF}$ pin by setting the REFBE bit in register REF0CN to a 1 (see Figure 5.1). The load seen by the $V_{REF}$ pin must draw less than 200 µA to GND. When using the internal voltage reference, bypass capacitors of 0.1 µF and 4.7 µF are recommended from the $V_{REF}$ pin to GND. If the internal reference is not used, the REFBE bit should be cleared to 0. Electrical specifications for the internal voltage reference are given in Table 2.5 on page 29.

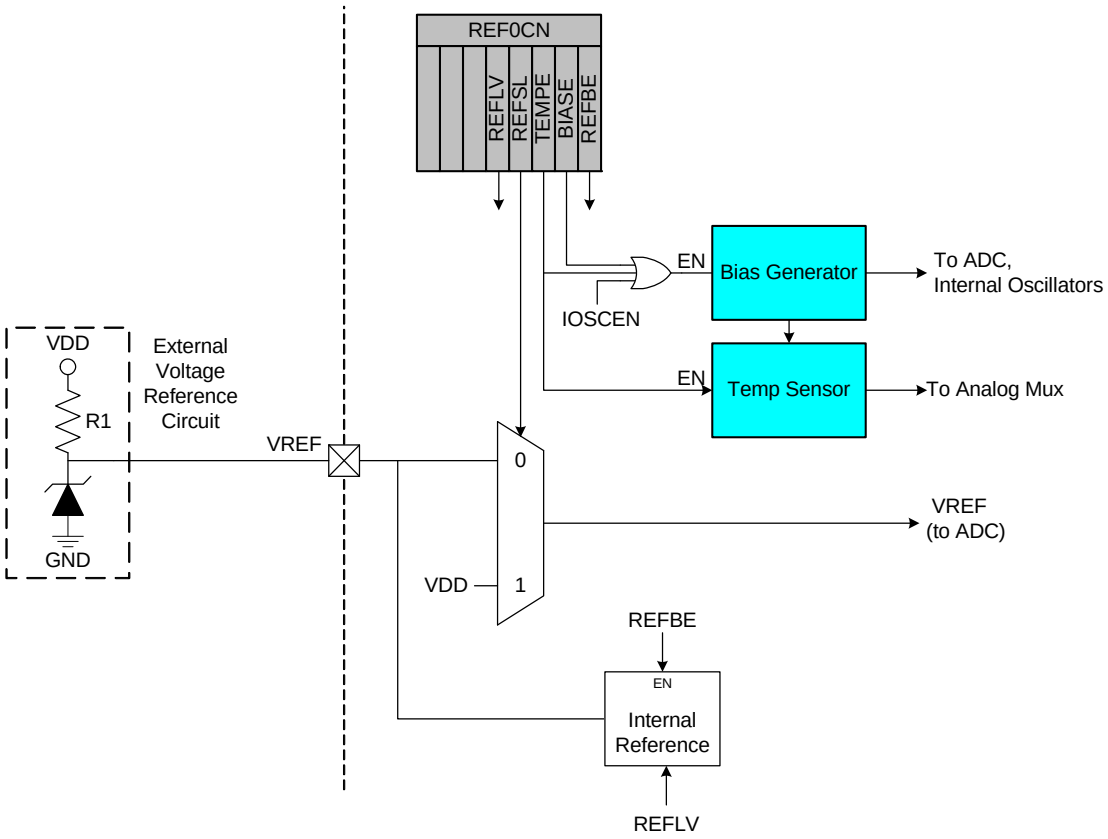



**Figure 5.1. Voltage Reference Functional Block Diagram**

**Table 9.2. Special Function Registers (Continued)**

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

| Register | Address | Description | Page |
|---|---|---|---|
| OSCICN | 0xB2 | Internal Oscillator Control | 137 |
| OSCXCN | 0xB1 | External Oscillator Control | 142 |
| P0 | 0x80 | Port 0 Latch | 129 |
| P0MASK | 0xC7 | Port 0 Mask | 131 |
| P0MAT | 0xD7 | Port 0 Match | 131 |
| P0MDIN | 0xF1 | Port 0 Input Mode Configuration | 129 |
| P0MDOUT | 0xA4 | Port 0 Output Mode Configuration | 130 |
| P0SKIP | 0xD4 | Port 0 Skip | 130 |
| P1 | 0x90 | Port 1 Latch | 132 |
| P1MASK | 0xBF | Port 1 Mask | 134 |
| P1MAT | 0xCF | Port 1 Match | 134 |
| P1MDIN | 0xF2 | Port 1 Input Mode Configuration | 132 |
| P1MDOUT | 0xA5 | Port 1 Output Mode Configuration | 133 |
| P1SKIP | 0xD5 | Port 1 Skip | 133 |
| PCA0CN | 0xD8 | PCA Control | 206 |
| PCA0CPH0 | 0xFC | PCA Capture 0 High | 209 |
| PCA0CPH1 | 0xEA | PCA Capture 1 High | 209 |
| PCA0CPH2 | 0xEC | PCA Capture 2 High | 209 |
| PCA0CPL0 | 0xFB | PCA Capture 0 Low | 209 |
| PCA0CPL1 | 0xE9 | PCA Capture 1 Low | 209 |
| PCA0CPL2 | 0xEB | PCA Capture 2 Low | 209 |
| PCA0CPM0 | 0xDA | PCA Module 0 Mode | 208 |
| PCA0CPM1 | 0xDB | PCA Module 1 Mode | 208 |
| PCA0CPM2 | 0xDC | PCA Module 2 Mode | 208 |
| PCA0H | 0xFA | PCA Counter High | 209 |
| PCA0L | 0xF9 | PCA Counter Low | 209 |
| PCA0MD | 0xD9 | PCA Mode | 207 |
| PCON | 0x87 | Power Control | 91 |
| PSCTL | 0x8F | Program Store R/W Control | 119 |
| PSW | 0xD0 | Program Status Word | 88 |

## 11.3. External Reset

The external RST pin provides a means for external circuitry to force the device into a reset state. Asserting an active-low signal on the RST pin generates a reset; an external pullup and/or decoupling of the RST pin may be necessary to avoid erroneous noise-induced resets. See Table 2.8 on page 32 for complete RST pin specifications. The PINRSF flag (RSTSRC.0) is set on exit from an external reset.

**Note:** Please refer to Section “20.6. Reset Low Time” on page 212 for restrictions on reset low time in older silicon revisions A and B.

## 11.4. Missing Clock Detector Reset

The Missing Clock Detector (MCD) is a one-shot circuit that is triggered by the system clock. If the system clock remains high or low for more than 100 µs, the one-shot will time out and generate a reset. After a MCD reset, the MCDRSF flag (RSTSRC.2) will read 1, signifying the MCD as the reset source; otherwise, this bit reads 0. Writing a 1 to the MCDRSF bit enables the Missing Clock Detector; writing a 0 disables it. The state of the RST pin is unaffected by this reset.

## 11.5. Comparator Reset

Comparator0 can be configured as a reset source by writing a 1 to the C0RSEF flag (RSTSRC.5). Comparator0 should be enabled and allowed to settle prior to writing to C0RSEF to prevent any turn-on chatter on the output from generating an unwanted reset. The Comparator0 reset is active-low: if the non-inverting input voltage (on CP0+) is less than the inverting input voltage (on CP0-), the device is put into the reset state. After a Comparator0 reset, the C0RSEF flag (RSTSRC.5) will read 1 signifying Comparator0 as the reset source; otherwise, this bit reads 0. The state of the RST pin is unaffected by this reset.

## 11.6. PCA Watchdog Timer Reset

The programmable Watchdog Timer (WDT) function of the Programmable Counter Array (PCA) can be used to prevent software from running out of control during a system malfunction. The PCA WDT function can be enabled or disabled by software as described in Section “19.3. Watchdog Timer Mode” on page 203; the WDT is enabled and clocked by SYSCLK / 12 following any reset. If a system malfunction prevents user software from updating the WDT, a reset is generated and the WDTRSF bit (RSTSRC.5) is set to 1. The state of the RST pin is unaffected by this reset.

## 11.7. Flash Error Reset

If a Flash read/write/erase or program read targets an illegal address, a system reset is generated. This may occur due to any of the following:

- A Flash write or erase is attempted above user code space. This occurs when PSWE is set to 1 and a MOVX write operation targets an address above the Lock Byte address.
- A Flash read is attempted above user code space. This occurs when a MOVC operation targets an address above the Lock Byte address.
- A program read is attempted above user code space. This occurs when user code attempts to branch to an address above the Lock Byte address.
- A Flash read, write or erase attempt is restricted due to a Flash security setting (see Section “12.4. Security Options” on page 117).
- A Flash write or erase is attempted while the $V_{DD}$ Monitor (VDDMON0) is disabled or not set to its high threshold setting.

The FERROR bit (RSTSRC.6) is set following a Flash error reset. The state of the RST pin is unaffected by this reset.

## 12.3. Non-volatile Data Storage

The Flash memory can be used for non-volatile data storage as well as program code. This allows data such as calibration coefficients to be calculated and stored at run time. Data is written using the MOVX write instruction and read using the MOVC instruction. Note: MOVX read instructions always target XRAM.

**Note**: See Section “12.1. Programming The Flash Memory” on page 113 for minimum $V_{DD}$ and temperature requirements for flash erase and write operations.

## 12.4. Security Options

The CIP-51 provides security options to protect the Flash memory from inadvertent modification by software as well as to prevent the viewing of proprietary program code and constants. The Program Store Write Enable (bit PSWE in register PSCTL) and the Program Store Erase Enable (bit PSEE in register PSCTL) bits protect the Flash memory from accidental modification by software. PSWE must be explicitly set to 1 before software can modify the Flash memory; both PSWE and PSEE must be set to 1 before software can erase Flash memory. Additional security features prevent proprietary program code and data constants from being read or altered across the C2 interface.

A Security Lock Byte located at the last byte of Flash user space offers protection of the Flash program memory from access (reads, writes, or erases) by unprotected code or the C2 interface. The Flash security mechanism allows the user to lock *n* 512-byte Flash pages, starting at page 0 (addresses 0x0000 to 0x01FF), where *n* is the 1’s complement number represented by the Security Lock Byte. **Note that the page containing the Flash Security Lock Byte is unlocked when no other Flash pages are locked (all bits of the Lock Byte are 1) and locked when any other Flash pages are locked (any bit of the Lock Byte is 0).** See example below.

| | |
|---|---|
| Security Lock Byte: | 11111101b |
| 1’s Complement: | 00000010b |
| Flash pages locked: | 3 (First two Flash pages + Lock Byte Page) |
| Addresses locked: | 0x0000 to 0x03FF (first two Flash pages)<br>0x1C00 to 0x1DFF in ’F520/0A/1/1A and ’F530/0A/1/1A<br>0x0C00 to 0x0FFF in ’F523/3A/4/4A and ’F533/3A/4/4A and<br>0x0600 to 0x07FF in ’F526/6A/7/7A and ’F536/6A/7/7A |

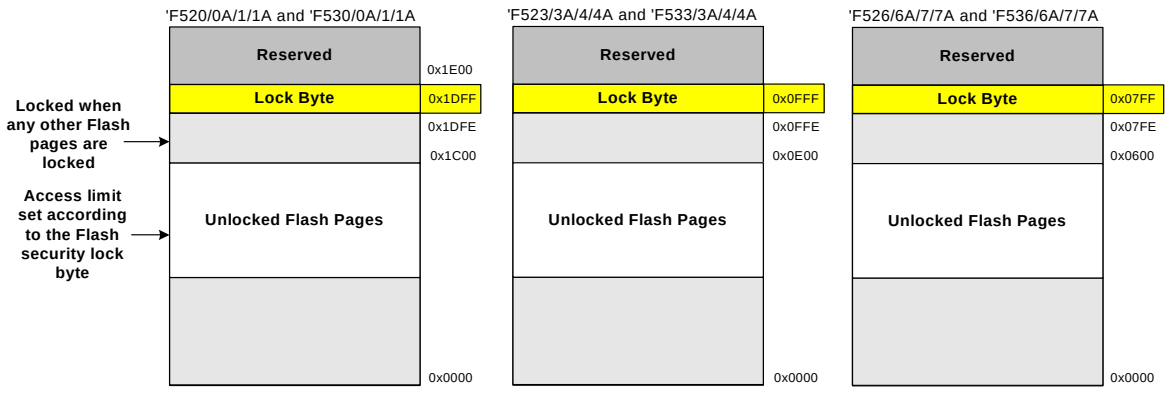



**Figure 12.1. Flash Program Memory Map**

## SFR Definition 14.2. OSCICL: Internal Oscillator Calibration

| R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| — | OSCICL | | | | | | | Varies |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| | | | | | | | SFR Address: | 0xB3 |

**Bit7**: **UNUSED**. Read = 0b. Write = don't care.
**Bits6–0**: **OSCICL**: Internal Oscillator Calibration Register.
This register determines the internal oscillator period. On C8051F52x/53x devices, the reset value is factory calibrated to generate an internal oscillator frequency of 24.5 MHz.

## SFR Definition 14.3. OSCIFIN: Internal Fine Oscillator Calibration

| R/W | R/W | R/W | R | R | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| — | — | OSCIFIN | | | | | | undetermined |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Bit Addressable |
| | | | | | | | SFR Address: | 0xB0 |

**Bits7–6**: **UNUSED**. Read = 00b, Write = don't care.
**Bits5–0**: **OSCIFIN**. Internal oscillator fine adjustment bits.

The valid range is between 0x00 and 0x27.

This register is a fine adjustment for the internal oscillator period. On C8051F52x/52xA/53x/53xA devices, the reset value is factory calibrated to generate an internal oscillator frequency of 24.5 MHz.

## 15.2. Operational Modes

UART0 provides standard asynchronous, full duplex communication. The UART mode (8-bit or 9-bit) is selected by the S0MODE bit (SCON0.7). Typical UART connection options are shown below.

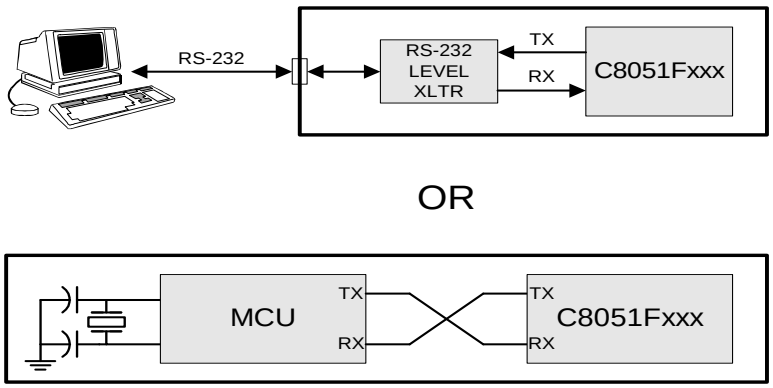



**Figure 15.3. UART Interconnect Diagram**

### 15.2.1. 8-Bit UART

8-Bit UART mode uses a total of 10 bits per data byte: one start bit, eight data bits (LSB first), and one stop bit. Data are transmitted LSB first from the TX0 pin and received at the RX0 pin. On receive, the eight data bits are stored in SBUF0 and the stop bit goes into RB80 (SCON0.2).

Data transmission begins when software writes a data byte to the SBUF0 register. The TI0 Transmit Interrupt Flag (SCON0.1) is set at the end of the transmission (the beginning of the stop-bit time). Data reception can begin any time after the REN0 Receive Enable bit (SCON0.4) is set to logic 1. After the stop bit is received, the data byte will be loaded into the SBUF0 receive register if the following conditions are met: RI0 must be logic 0, and if MCE0 is logic 1, the stop bit must be logic 1. In the event of a receive data overrun, the first received 8 bits are latched into the SBUF0 receive register and the following overrun data bits are lost.

If these conditions are met, the eight bits of data is stored in SBUF0, the stop bit is stored in RB80 and the RI0 flag is set. If these conditions are not met, SBUF0 and RB80 will not be loaded and the RI0 flag will not be set. An interrupt will occur if enabled when either TI0 or RI0 is set.

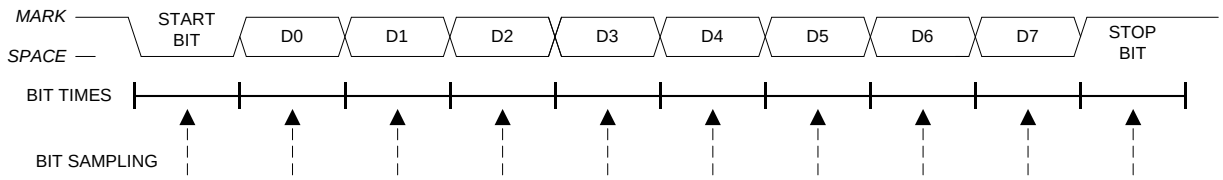



**Figure 15.4. 8-Bit UART Timing Diagram**

# 16. Enhanced Serial Peripheral Interface (SPI0)

The Serial Peripheral Interface (SPI0) provides access to a flexible, full-duplex synchronous serial bus. SPI0 can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select SPI0 in slave mode, or to disable Master Mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a chip-select output in master mode, or disabled for 3-wire operation. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

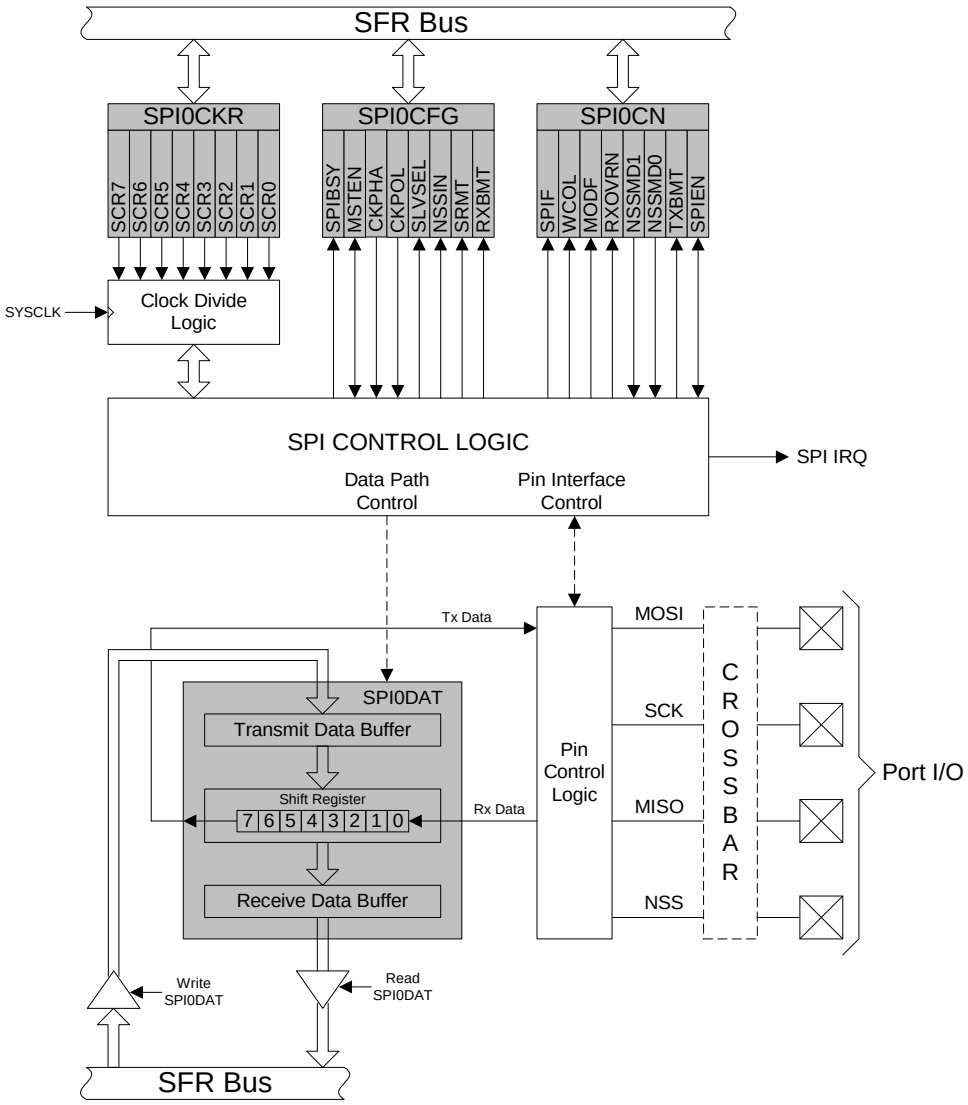



**Figure 16.1. SPI Block Diagram**

## SFR Definition 16.2. SPI0CN: SPI0 Control

| R/W | R/W | R/W | R/W | R/W | R/W | R | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| SPIF | WCOL | MODF | RXOVRN | NSSMD1 | NSSMD0 | TXBMT | SPIEN | 00000110 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Bit Addressable |

SFR Address: 0xF8

**Bit7**: **SPIF**: SPI0 Interrupt Flag.
This bit is set to logic 1 by hardware at the end of a data transfer. If interrupts are enabled, setting this bit causes the CPU to vector to the SPI0 interrupt service routine. This bit is not automatically cleared by hardware. It must be cleared by software.

**Bit6**: **WCOL**: Write Collision Flag.
This bit is set to logic 1 by hardware (and generates a SPI0 interrupt) if a write to SPI0DAT is attempted when the transmit buffer has not been emptied to the SPI shift register. When this occurs, the write to SPI0DAT will be ignored, and the transmit buffer will not be written. This bit is not automatically cleared by hardware. It must be cleared by software.

**Bit5**: **MODF**: Mode Fault Flag.
This bit is set to logic 1 by hardware (and generates a SPI0 interrupt) when a master mode collision is detected (NSS is low, MSTEN = 1, and NSSMD[1:0] = 01). This bit is not automatically cleared by hardware. It must be cleared by software.

**Bit4**: **RXOVRN**: Receive Overrun Flag (Slave Mode only).
This bit is set to logic 1 by hardware (and generates a SPI0 interrupt) when the receive buffer still holds unread data from a previous transfer and the last bit of the current transfer is shifted into the SPI0 shift register. This bit is not automatically cleared by hardware. It must be cleared by software.

**Bits3–2**: **NSSMD1–NSSMD0**: Slave Select Mode.
Selects between the following NSS operation modes:
(See Section “16.2. SPI0 Master Mode Operation” on page 153 and Section “16.3. SPI0 Slave Mode Operation” on page 154).
00: 3-Wire Slave or 3-wire Master Mode. NSS signal is not routed to a port pin.
01: 4-Wire Slave or Multi-Master Mode (Default). NSS is always an input to the device.
1x: 4-Wire Single-Master Mode. NSS signal is mapped as an output from the device and will assume the value of NSSMD0.

**Bit1**: **TXBMT**: Transmit Buffer Empty.
This bit will be set to logic 0 when new data has been written to the transmit buffer. When data in the transmit buffer is transferred to the SPI shift register, this bit will be set to logic 1, indicating that it is safe to write a new byte to the transmit buffer.

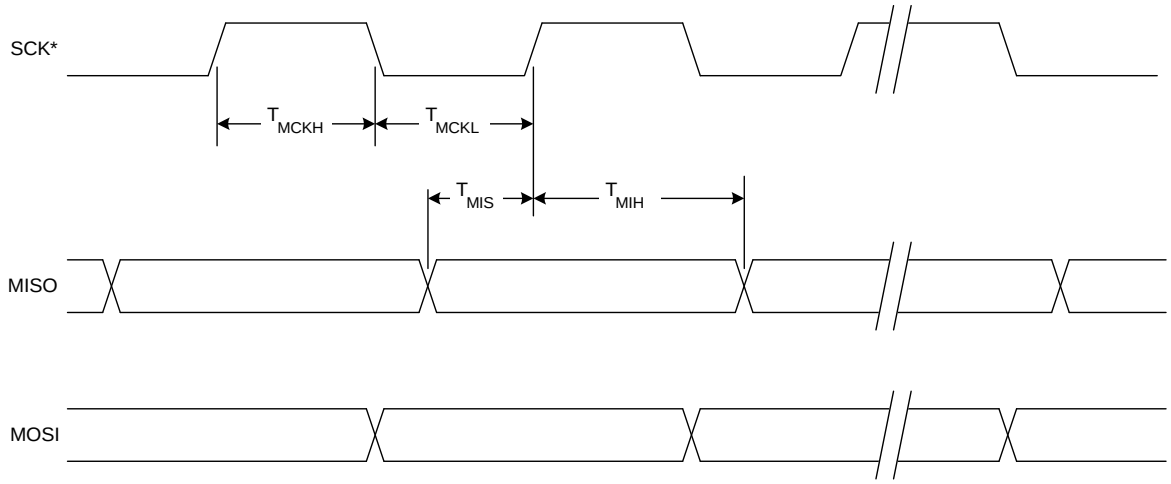
**Bit0**: **SPIEN**: SPI0 Enable.
This bit enables/disables the SPI.
0: SPI disabled.
1: SPI enabled.

## SFR Definition 16.4. SPI0DAT: SPI0 Data

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |

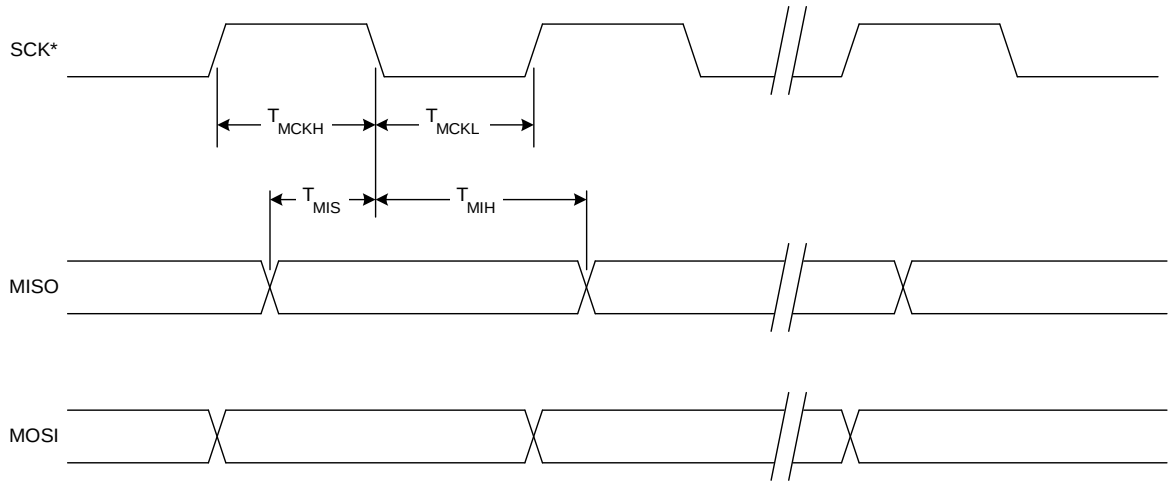
SFR Address: 0xA3

**Bits7–0**: **SPI0DAT**: SPI0 Transmit and Receive Data.
The SPI0DAT register is used to transmit and receive SPI0 data. Writing data to SPI0DAT places the data into the transmit buffer and initiates a transfer when in Master Mode. A read of SPI0DAT returns the contents of the receive buffer.




* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

**Figure 16.6. SPI Master Timing (CKPHA = 0)**




* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

**Figure 16.7. SPI Master Timing (CKPHA = 1)**

# 18. Timers

Each MCU includes three counter/timers: two are 16-bit counter/timers compatible with those found in the standard 8051, and one is a 16-bit auto-reload timer for use with other device peripherals or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. Timer 2 offer 16-bit and split 8-bit timer functionality with auto-reload.

| Timer 0 and Timer 1 Modes | Timer 2 Modes |
|---|---|
| 13-bit counter/timer | 16-bit timer with auto-reload |
| 16-bit counter/timer | |
| 8-bit counter/timer with auto-reload | Two 8-bit timers with auto-reload |
| Two 8-bit counter/timers (Timer 0 only) | |

Timers 0 and 1 may be clocked by one of five sources, determined by the Timer Mode Select bits (T1M–T0M) and the Clock Scale bits (SCA1–SCA0). The Clock Scale bits define a pre-scaled clock from which Timer 0 and/or Timer 1 may be clocked (See SFR Definition 18.3 for pre-scaled clock selection).

Timer 0/1 may then be configured to use this pre-scaled clock signal or the system clock. Timer 2 may be clocked by the system clock, the system clock divided by 12, or the external oscillator clock source divided by 8.

Timer 0 and Timer 1 may also be operated as counters. When functioning as a counter, a counter/timer register is incremented on each high-to-low transition at the selected input pin (T0 or T1). Events with a frequency of up to one-fourth the system clock's frequency can be counted. The input signal need not be periodic, but it must be held at a given level for at least two full system clock cycles to ensure the level is properly sampled.

## 18.1. Timer 0 and Timer 1

Each timer is implemented as a 16-bit register accessed as two separate bytes: a low byte (TL0 or TL1) and a high byte (TH0 or TH1). The Counter/Timer Control register (TCON) is used to enable Timer 0 and Timer 1 as well as indicate status. Timer 0 interrupts can be enabled by setting the ET0 bit in the IE register (Section “10.4. Interrupt Register Descriptions” on page 100); Timer 1 interrupts can be enabled by setting the ET1 bit in the IE register (Section 10.4). Both counter/timers operate in one of four primary modes selected by setting the Mode Select bits T1M1–T0M0 in the Counter/Timer Mode register (TMOD). Each timer can be configured independently. Each operating mode is described below.

### 18.1.1. Mode 0: 13-bit Counter/Timer

Timer 0 and Timer 1 operate as 13-bit counter/timers in Mode 0. The following describes the configuration and operation of Timer 0. However, both timers operate identically, and Timer 1 is configured in the same manner as described for Timer 0.

The TH0 register holds the eight MSBs of the 13-bit counter/timer. TL0 holds the five LSBs in bit positions TL0.4–TL0.0. The three upper bits of TL0 (TL0.7–TL0.5) are indeterminate and should be masked out or ignored when reading. As the 13-bit timer register increments and overflows from 0x1FFF (all ones) to 0x0000, the timer overflow flag TF0 (TCON.5) is set and an interrupt will occur if Timer 0 interrupts are enabled.

The C/T0 bit (TMOD.2) selects the counter/timer's clock source. When C/T0 is set to logic 1, high-to-low transitions at the selected Timer 0 input pin (T0) increment the timer register (Refer to Section “13.1. Priority Crossbar Decoder” on page 122 for information on selecting and configuring external I/O pins). Clearing C/T selects the clock defined by the T0M bit (CKCON.3). When T0M is set, Timer 0 is

clocked by the system clock. When T0M is cleared, Timer 0 is clocked by the source selected by the Clock Scale bits in CKCON (see SFR Definition 18.3).

Setting the TR0 bit (TCON.4) enables the timer when either GATE0 (TMOD.3) is logic 0 or the input signal INT0 is active as defined by bit IN0PL in register IT01CF (see SFR Definition 10.5. IT01CF: INT0/INT1 Configuration). Setting GATE0 to 1 allows the timer to be controlled by the external input signal INT0 (see Section “10.4. Interrupt Register Descriptions” on page 100), facilitating pulse width measurements.

| TR0 | GATE0 | INT0 | Counter/Timer |
|---|---|---|---|
| 0 | X | X | Disabled |
| 1 | 0 | X | Enabled |
| 1 | 1 | 0 | Disabled |
| 1 | 1 | 1 | Enabled |
| X = Don't Care | | | |

Setting TR0 does not force the timer to reset. The timer registers should be loaded with the desired initial value before the timer is enabled.

TL1 and TH1 form the 13-bit register for Timer 1 in the same manner as described above for TL0 and TH0. Timer 1 is configured and controlled using the relevant TCON and TMOD bits just as with Timer 0. The input signal INT0 is used with Timer 1; the INT0 polarity is defined by bit IN1PL in register IT01CF (see SFR Definition 10.5. IT01CF: INT0/INT1 Configuration).

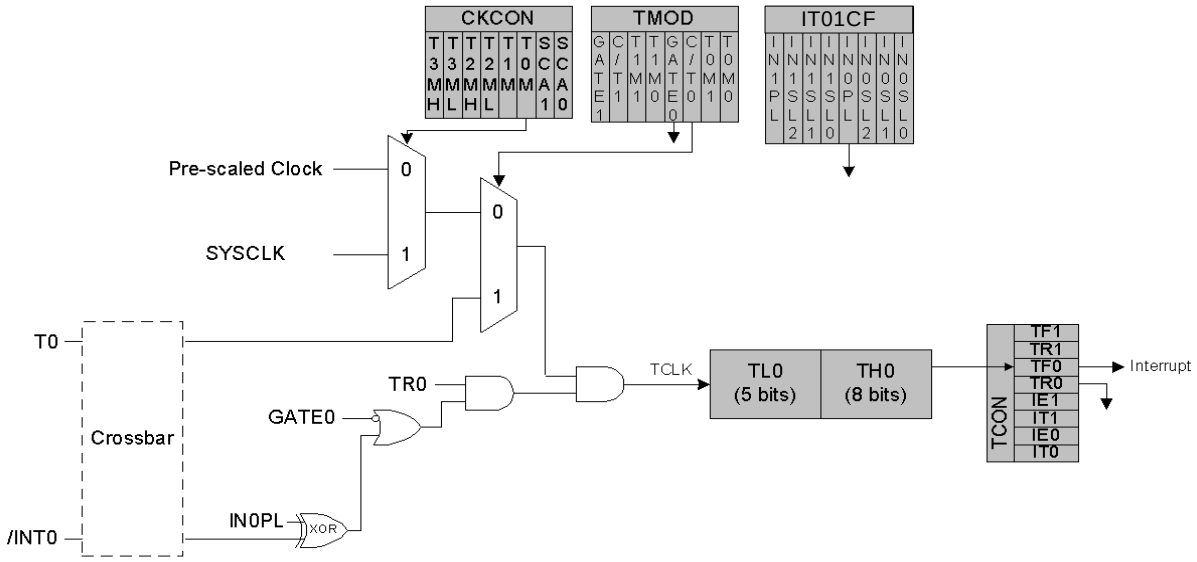



**Figure 18.1. T0 Mode 0 Block Diagram**

## Revision 1.2 to 1.3

- Updated “System Overview” on page 13 with a voltage range specification for the internal oscillator.
- Updated Table 2.11 on page 34 with new conditions for the internal oscillator accuracy. The internal oscillator accuracy is dependent on the operating voltage range.
- Updated Section 2 to remove the internal oscillator curve across temperature diagram.
- Updated Figure “4.5 12-Bit ADC Burst Mode Example with Repeat Count Set to 4” on page 58 with new timing diagram when using CNVSTR pin.
- Updated SFR Definition 5.1 (REF0CN) with oscillator suspend requirement for ZTCEN.
- Updated SFR Definition 6.1 (REG0CN) with a new definition for Bit 6. The bit 6 reset value is 1b and must be written to 1b.
- Updated Section “8.3.3. Suspend Mode” on page 90 with note regarding ZTCEN.
- Updated Section “17. LIN (C8051F520/0A/3/3A/6/6A and C8051F530/0A/3/3A/6/6A)” on page 164 with a voltage range specification for the internal oscillator.

## Revision 1.3 to 1.4

- Added ‘AEC-Q100’ qualification information on page 1.
- Changed page headers throughout the document from ‘C8051F52x/F52xA/F53x/F53xA’ to ‘C8051F52x/53x’.
- Updated supply voltage to "2.0 to 5.25 V" on page 1 and in Section 1 on page 13.
- Corrected reference to development kit (C8051F530DK) in Section “1.2.4. On-Chip Debug Circuitry” on page 18.
- Updated minimum Supply Input Voltage ($V_{REGIN}$) for C8051F52x-C/F53x-C devices in Table 2.2 on page 26 and Table 2.6 on page 30.
- Updated digital supply current ($I_{DD}$ and Idle $I_{DD}$) typical values for condition ‘Clock = 25 MHz’ in Table 2.2 on page 26.
- Updated $I_{DD}$ Frequency Sensitivity and Idle $I_{DD}$ Frequency Sensitivity values in Table 2.2 on page 26; removed Figure 2.1 and Figure 2.2 that used to provide the same frequency sensitivity slopes. Also removed IDD Supply Sensitivity and Idle IDD Supply Sensitivity typical values.
- Added Digital Supply Current (Stop or Suspend Mode) values at multiple temperatures Table 2.2 on page 26.
- Added a note in Table 2.3, “ADC0 Electrical Characteristics,” on page 28 with reference to Section “4.4. Selectable Gain” on page 60; also added note to indicate that additional tracking time may be necessary if VDD is less than the minimum specified VDD.
- Split off temperature sensor specifications from Table 2.3 into a separate table Table 2.4; Updated temperature sensor gain and added supply current values.
- Added temperature condition for Bias Current specification in Table 2.6 on page 30.
- Updated Comparator Input Offset Voltage values in Table 2.7 on page 31.
- Updated VDD Monitor (VDDMON0) Low Threshold ($V_{RST-LOW}$) minimum value for C8051F52xA/F52x-C/F53xA/F53x-C devices in Table 2.8 on page 32.
- Updated VDD Monitor (VDDMON0) supply current values in Table 2.8 on page 32.
- Added specifications for the new level-sensitive VDD monitor (VDDMON1) to Table 2.8, “Reset Electrical Characteristics,” on page 32 and also added notes to clarify the applicable $V_{RST}$ theshold level.
- Added note in Table 2.9, “Flash Electrical Characteristics,” on page 33 to describe the minimum flash programming temperature for –I (Industrial Grade) devices; Also added the same note and references to it in Section “12.1. Programming The Flash Memory” on page 113, Section “12.3. Non-volatile Data Storage” on page 117, and in SFR Definition 12.1 (PSCTL).