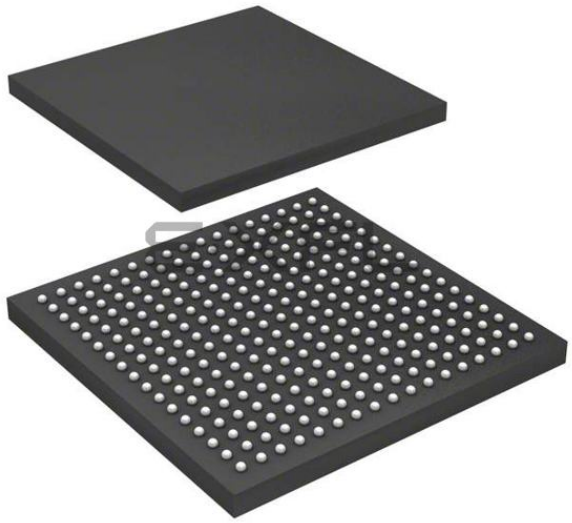

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A7
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	528MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	LCD, LVDS
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	ARM TZ, A-HAB, CAAM, CSU, SJC, SNVS
Package / Case	289-LFBGA
Supplier Device Package	289-MAPBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6g2dvm05ab

Table 3. i.MX 6UltraLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A7 Core Platform.
eCSPI1 eCSPI2 eCSPI3 eCSPI4	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
EIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The EIM NOR-FLASH / PSRAM provides: • Support 16-bit PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit NOR-Flash memories, at slow frequency • Multiple chip selects
EMV SIM1 EMV SIM2	Europay, Master and Visa Subscriber Identification Module	Connectivity peripherals	EMV SIM is designed to facilitate communication to Smart Cards compatible to the EMV version 4.3 standard (Book 1) and Smart Cards compatible with ISO/IEC 7816-3 standard.
ENET1 ENET2	Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10/100 Mbit/s Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the reference manual for details.
EPIT1 EPIT2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.
FLEXCAN1 FLEXCAN2	Flexible Controller Area Network	Connectivity Peripherals	The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames.
GPIO1 GPIO2 GPIO3 GPIO4 GPIO5	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O.

4.3.1 Digital regulators (LDO_ARM, LDO_SOC)

There are two digital LDO regulators (“Digital”, because of the logic loads that they drive, not because of their construction). The advantages of the regulators are to reduce the input supply variation because of their input supply ripple rejection and their on-die trimming. This translates into more stable voltage for the on-chip logics.

These regulators have two basic modes:

- Power Gate. The regulation FET is switched fully off limiting the current draw from the supply. The analog part of the regulator is powered down here limiting the power consumption.
- Analog regulation mode. The regulation FET is controlled such that the output voltage of the regulator equals the programmed target voltage. The target voltage is fully programmable in 25 mV steps.

For additional information, see the *i.MX 6UltraLite Reference Manual* (IMX6ULRM).

4.3.2 Regulators for analog modules

4.3.2.1 LDO_1P1

The LDO_1P1 regulator implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 11 for minimum and maximum input requirements). Typical Programming Operating Range is 1.0 V to 1.2 V with the nominal default setting as 1.1 V. The LDO_1P1 supplies the USB Phy, and PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for *i.MX 6UltraLite Applications Processors* (IMX6ULHDG).

For additional information, see the *i.MX 6UltraLite Reference Manual* (IMX6ULRM).

4.3.2.2 LDO_2P5

The LDO_2P5 module implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 11 for minimum and maximum input requirements). Typical Programming Operating Range is 2.25 V to 2.75 V with the nominal default setting as 2.5 V. LDO_2P5 supplies the DDR IOs, USB Phy, E-fuse module, and PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature. An alternate self-biased low-precision weak-regulator is included that can be enabled for applications needing to keep the output voltage alive during low-power modes where the main regulator driver and its associated global bandgap reference module are disabled. The output of the weak-regulator is not programmable and is a function of the input supply as well as the load current. Typically, with a 3 V input supply the weak-regulator output is 2.525 V and its output impedance is approximately 40 Ω.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for *i.MX 6UltraLite Applications Processors* (IMX6ULHDG).

For additional information, see the *i.MX 6UltraLite Reference Manual* (IMX6ULRM).

4.3.2.3 LDO_USB

The LDO_USB module implements a programmable linear-regulator function from the USB VUSB voltages (4.4 V–5.5 V) to produce a nominal 3.0 V output voltage. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. This regulator has a built in power-mux that allows the user to select to run the regulator from either USB VBUS supply, when both are present. If only one of the USB VBUS voltages is present, then, the regulator automatically selects this supply. Current limit is also included to help the system meet in-rush current targets.

For information on external capacitor requirements for this regulator, see the *Hardware Development Guide for i.MX 6UltraLite Applications Processors* (IMX6ULHDG).

For additional information, see the *i.MX 6UltraLite Reference Manual* (IMX6ULRM).

4.4 PLL's electrical characteristics

4.4.1 Audio/Video PLL's electrical parameters

Table 17. Audio/Video PLL's Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.2 528 MHz PLL

Table 18. 528 MHz PLL's Electrical Parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<11250 reference cycles

Table 24. Single Voltage GPIO DC Parameters (continued)

Parameter	Symbol	Test Conditions	Min	Max	Units
Input Hysteresis (OVDD= 1.8V)	VHYS_LowVDD	OVDD=1.8V	250	—	mV
Input Hysteresis (OVDD=3.3V)	VHYS_HighVDD	OVDD=3.3V	250	—	mV
Schmitt trigger VT+[2,3]	VTH+	—	0.5*OVDD	—	mV
Schmitt trigger VT-[2,3]	VTH-	—	—	0.5*OVDD	mV
Pull-up resistor (22_kΩ PU)	RPU_22K	Vin=0V	—	212	μA
Pull-up resistor (22_kΩ PU)	RPU_22K	Vin=OVDD	—	1	μA
Pull-up resistor (47_kΩ PU)	RPU_47K	Vin=0V	—	100	μA
Pull-up resistor (47_kΩ PU)	RPU_47K	Vin=OVDD	—	1	μA
Pull-up resistor (100_kΩ PU)	RPU_100K	Vin=0V	—	48	μA
Pull-up resistor (100_kΩ PU)	RPU_100K	Vin=OVDD	—	1	μA
Pull-down resistor (100_kΩ PD)	RPD_100K	Vin=OVDD	—	48	μA
Pull-down resistor (100_kΩ PD)	RPD_100K	Vin=0V	—	1	μA
Input current (no PU/PD)	IIN	VI = 0, VI = OVDD	-1	1	μA
Keeper Circuit Resistance	R_Keeper	VI =0.3*OVDD, VI = 0.7* OVDD	105	175	kΩ

1 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/ undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

2 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, Vil or Vih. Monotonic input transition time is from 0.1 ns to 1 s.

3 Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4.6.3 DDR I/O DC parameters

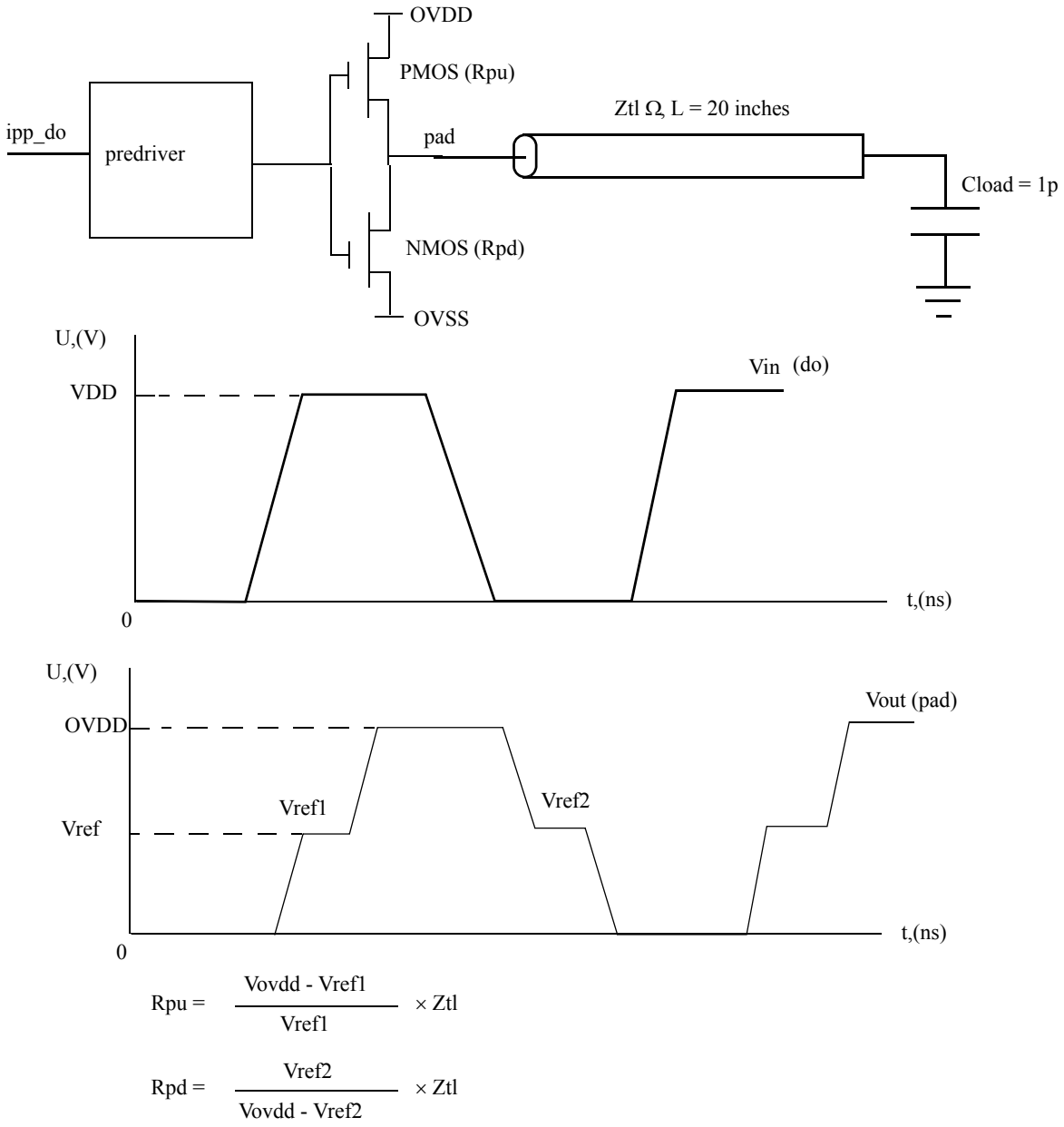
The DDR I/O pads support LPDDR2 and DDR3/DDR3L operational modes. For details on supported DDR memory configurations, see Section 4.10, “Multi-Mode DDR Controller (MMDC)".

MMDC operation with the standards stated above is contingent upon the board DDR design adherence to the DDR design and layout requirements stated in the *Hardware Development Guide for the i.MX 6UltraLite Applications Processor* (IMX6ULHDG).

4.6.3.1 LPDDR2 Mode I/O DC parameters

Table 25. LPDDR2 I/O DC Electrical Parameters[1]

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	VOH	Ioh= -0.1mA	0.9*OVDD	—	V
Low-level output voltage	VOL	Iol= 0.1mA	—	0.1*OVDD	V
Input Reference Voltage	Vref	—	0.49*OVDD	0.51*OVDD	V



$$Rpu = \frac{Vovdd - Vref1}{Vref1} \times Ztl$$

$$Rpd = \frac{Vref2}{Vovdd - Vref2} \times Ztl$$

Figure 6. Impedance Matching Load for Measurement

4.8.1 Single voltage GPIO output buffer impedance

Table 33 shows the GPIO output buffer impedance (OVDD 1.8 V).

Table 33. GPIO Output Buffer Average Impedance (OVDD 1.8 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	260 130 88 65 52 43 37	Ω

Table 34 shows the GPIO output buffer impedance (OVDD 3.3 V).

Table 34. GPIO Output Buffer Average Impedance (OVDD 3.3 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	157 78 53 39 32 26 23	Ω

4.8.2 DDR I/O output buffer impedance

Table 35 shows DDR I/O output buffer impedance of i.MX 6UltraLite processors.

Table 35. DDR I/O Output Buffer Impedance

Parameter	Symbol	Test Conditions DSE (Drive Strength)	Typical		Unit
			NVCC_DRAM=1.5 V (DDR3) DDR_SEL=11	NVCC_DRAM=1.2 V (LPDDR2) DDR_SEL=10	
Output Driver Impedance	Rdrv	000 001 010 011 100 101 110 111	Hi-Z 240 120 80 60 48 40 34	Hi-Z 240 120 80 60 48 40 34	Ω

Note:

1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.
2. Calibration is done against 240 Ω external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.
4. It is recommended to use a strong driver strength (<= 48 Ω) for all DDR pads and all DDR type (DDR3/DDR3L/LPDDR2).

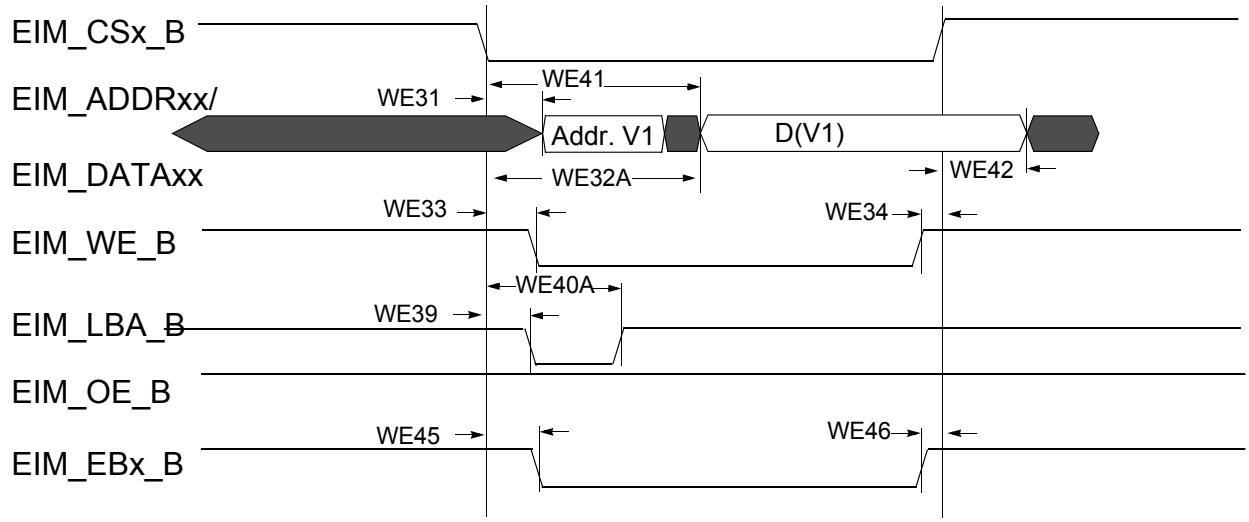


Figure 18. Asynchronous A/D Muxed Write Access

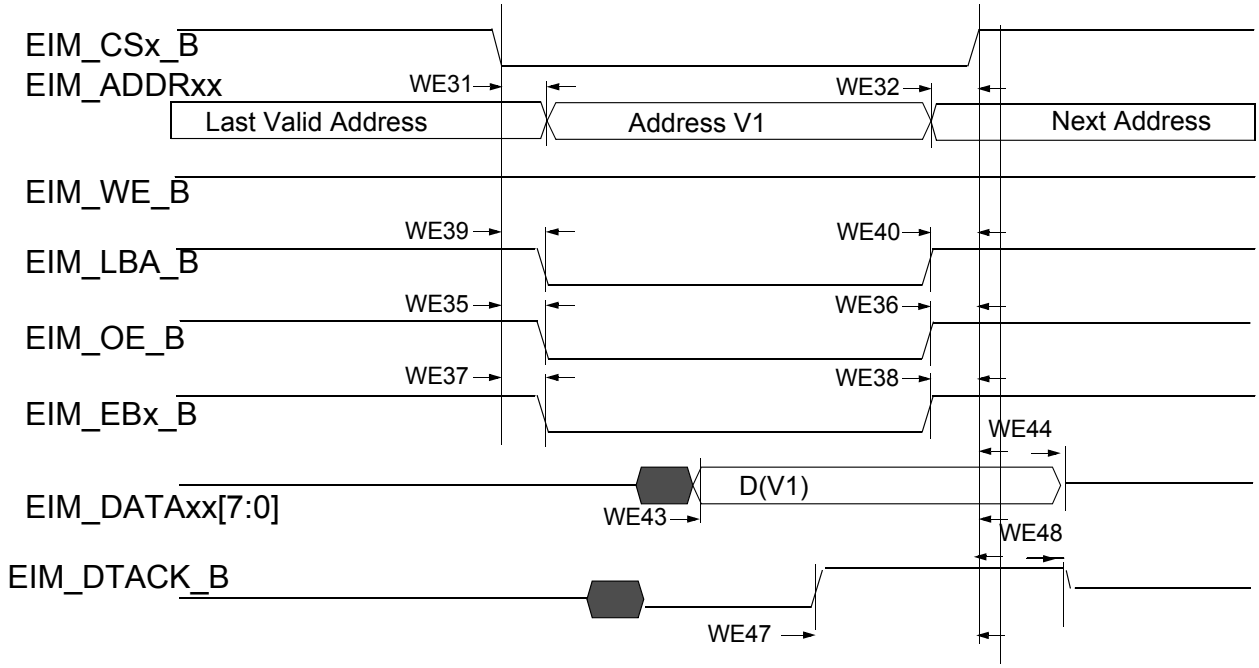


Figure 19. DTACK Mode Read Access (DAP=0)

(VSYNC), then CSI_HSYNC (HSYNC) is asserted and holds for the entire line. The pixel clock, CSI_PIXCLK (PIXCLK), is valid as long as HSYNC is asserted.

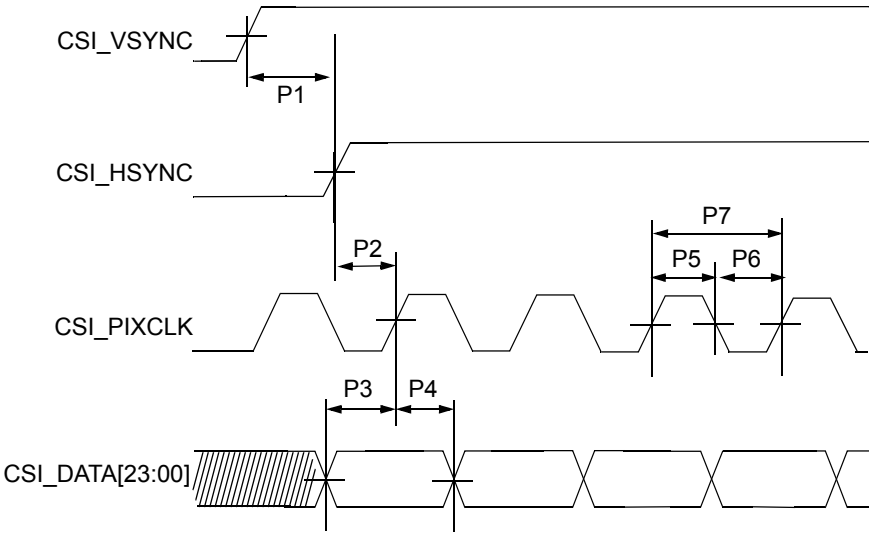


Figure 32. CSI Gated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

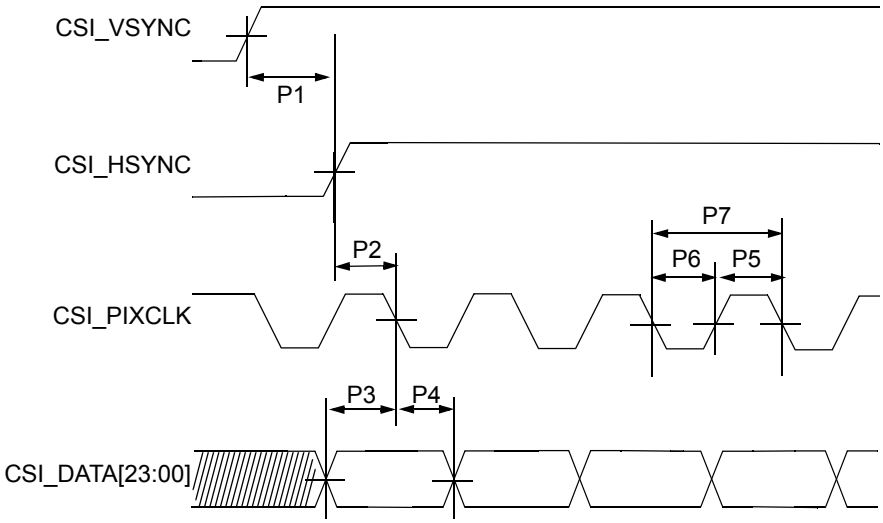


Figure 33. CSI Gated Clock Mode—Sensor Data at Rising Edge, Latch Data at Falling Edge

Table 45. CSI Gated Clock Mode Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
P1	CSI_VSYNC to CSI_HSYNC time	tV2H	33.5	—	ns
P2	CSI_HSYNC setup time	tHsu	1	—	ns
P3	CSI DATA setup time	tDsu	1	—	ns

Table 45. CSI Gated Clock Mode Timing Parameters (continued)

ID	Parameter	Symbol	Min.	Max.	Units
P4	CSI DATA hold time	tDh	1	—	ns
P5	CSI pixel clock high time	tCLKh	3.75	—	ns
P6	CSI pixel clock low time	tCLKl	3.75	—	ns
P7	CSI pixel clock frequency	fCLK	—	133	MHz

4.12.1.0.2 Ungated clock mode timing

Figure 34 shows the ungated clock mode timings of CSI, and Table 46 describes the timing parameters (P1–P6) that are shown in the figure. In ungated mode the CSI_VSYNC and CSI_PIXCLK signals are used, and the CSI_HSYNC signal is ignored.

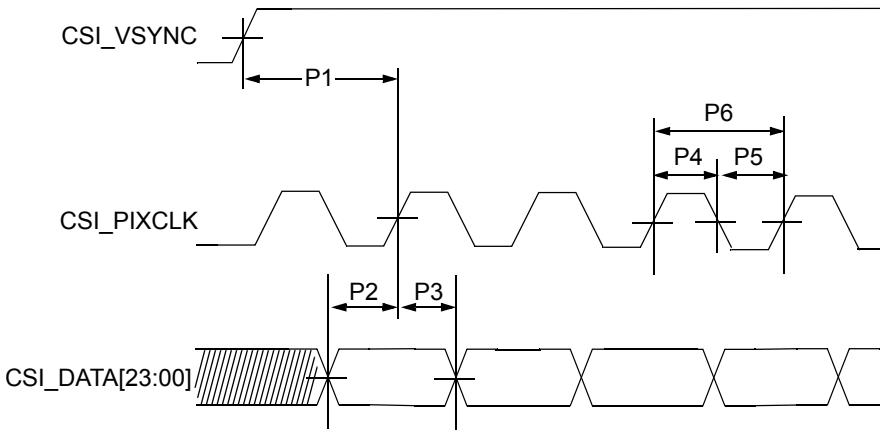


Figure 34. CSI Ungated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

Table 46. CSI Ungated Clock Mode Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
P1	CSI_VSYNC to pixel clock time	tVSYNC	33.5	—	ns
P2	CSI DATA setup time	tDsu	1	—	ns
P3	CSI DATA hold time	tDh	1	—	ns
P4	CSI pixel clock high time	tCLKh	3.75	—	ns
P5	CSI pixel clock low time	tCLKl	3.75	—	ns
P6	CSI pixel clock frequency	fCLK	—	133	MHz

The CSI enables the chip to connect directly to external CMOS image sensors, which are classified as dumb or smart as follows:

- Dumb sensors only support traditional sensor timing (vertical sync (VSYNC) and horizontal sync (HSYNC)) and output-only Bayer and statistics data.
- Smart sensors support CCIR656 video decoder formats and perform additional processing of the image (for example, image compression, image pre-filtering, and various data output formats).

[2] SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.12.2.2 ECSPI slave mode timing

Figure 36 depicts the timing of ECSPI in slave mode. Table 48 lists the ECSPI slave mode timing characteristics.

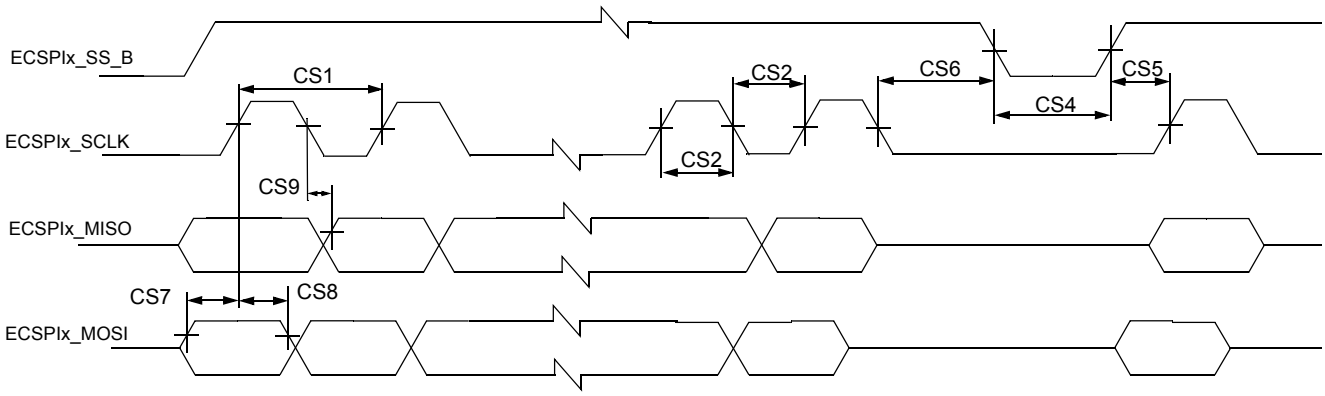


Figure 36. ECSPI Slave Mode Timing Diagram

Table 48. ECSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPI_SCLK Cycle Time–Write	t_{clk}	15 43	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read ECSPIx_SCLK High or Low Time–Write	t_{SW}	7 21.5	—	ns
CS4	ECSPIx_SS_B pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SS_B Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	ECSPIx_SS_B Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	ECSPIx_MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	ECSPIx_MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	ECSPIx_MISO Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmiso}	4	19	ns

Table 62. QuadSPI Input Timing (SDR mode with internal sampling)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{IS}	Setup time for incoming data	8.67	—	ns
T_{IH}	Hold time requirement for incoming data	0	—	ns

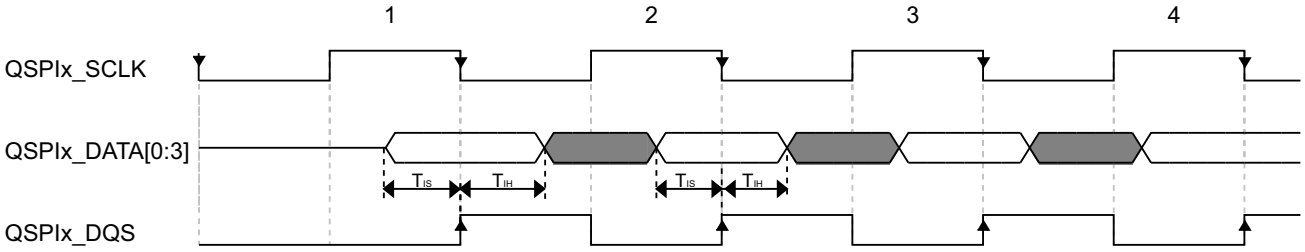


Figure 50. QuadSPI Input/Read Timing (SDR mode with loopback DQS sampling)

Table 63. QuadSPI Input/Read Timing (SDR mode with loopback DQS sampling)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{IS}	Setup time for incoming data	2	—	ns
T_{IH}	Hold time requirement for incoming data	1	—	ns

NOTE

- For internal sampling, the timing values assumes using sample point 0, that is QuadSPIx_SMPR[SDRSMP] = 0.
- For loopback DQS sampling, the data strobe is output to the DQS pad together with the serial clock. The data strobe is looped back from DQS pad and used to sample input data.

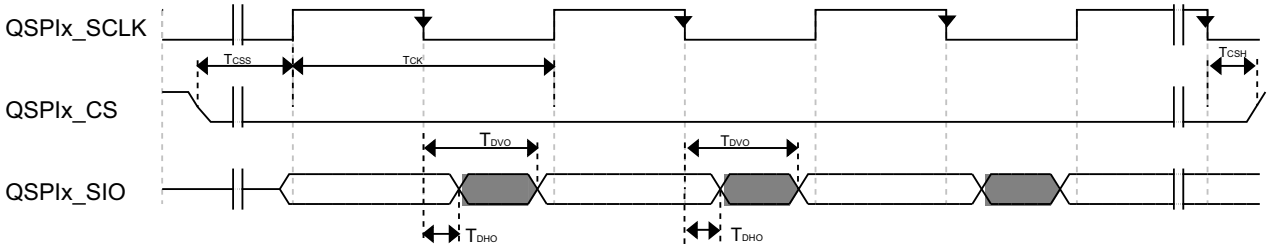


Figure 51. QuadSPI Output/Write Timing (SDR mode)

Table 64. QuadSPI Output/Write Timing (SDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{DVO}	Output data valid time	—	2	ns
T_{DHO}	Output data hold time	0	—	ns
T_{CK}	SCK clock period	10	—	ns
T_{CSS}	Chip select output setup time	3	—	SCK cycle(s)
T_{CSH}	Chip select output hold time	3	—	SCK cycle(s)

NOTE

T_{css} and T_{csh} are configured by the QuadSPIx_FLSHCR register, the default value of 3 are shown on the timing. Please refer to the *i.MX 6UltraLite Reference Manual (IMX6ULRM)* for more details.

4.12.9.2 DDR mode

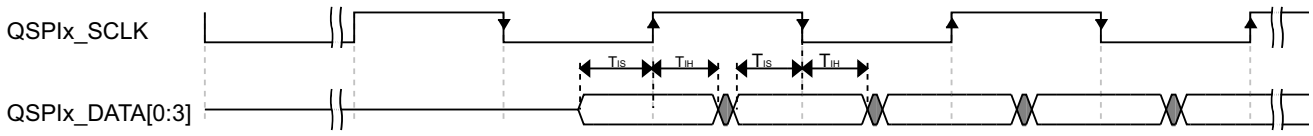


Figure 52. QuadSPI Input/Read Timing (DDR mode with internal sampling)

Table 65. QuadSPI Input/Read Timing (DDR mode with internal sampling)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{IS}	Setup time for incoming data	8.67	—	ns
T_{IH}	Hold time requirement for incoming data	0	—	ns

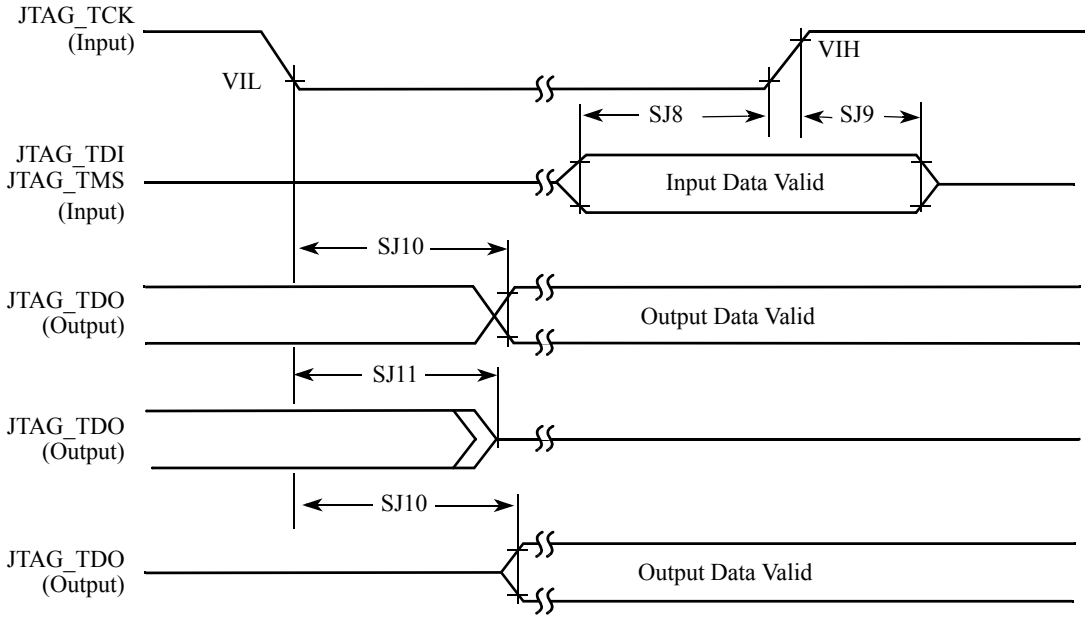


Figure 59. Test Access Port Timing Diagram

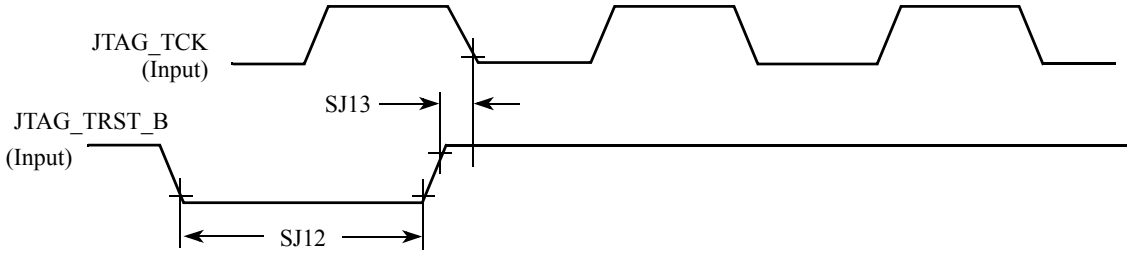


Figure 60. JTAG_TRST_B Timing Diagram

Table 70. JTAG Timing

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ0	JTAG_TCK frequency of operation $1/(3 \bullet T_{DC})$[1]	0.001	22	MHz
SJ1	JTAG_TCK cycle time in crystal mode	45	—	ns
SJ2	JTAG_TCK clock pulse width measured at V_M[2]	22.5	—	ns
SJ3	JTAG_TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	JTAG_TCK low to output data valid	—	40	ns
SJ7	JTAG_TCK low to output high impedance	—	40	ns
SJ8	JTAG_TMS, JTAG_TDI data set-up time	5	—	ns

5 Boot mode configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot mode configuration pins

Table 78 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX 6UltraLite Fuse Map document and the System Boot chapter in *i.MX 6UltraLite Reference Manual (IMX6ULRM)*.

Table 78. Fuses and Associated Pins Used for Boot

Pin	Direction at reset	eFuse name	Details
BOOT_MODE0	Input with 100 K pull-down	N/A	Boot mode selection
BOOT_MODE1	Input with 100 K pull-down	N/A	Boot mode selection

Table 91. 14x14 mm Functional Contact Assignments (continued)

DRAM_DATA09	U3	NVCC_DRAM	DDR	ALT0	DRAM_DATA09	Input	100 kΩ pull-up
DRAM_DATA10	U5	NVCC_DRAM	DDR	ALT0	DRAM_DATA10	Input	100 kΩ pull-up
DRAM_DATA11	R4	NVCC_DRAM	DDR	ALT0	DRAM_DATA11	Input	100 kΩ pull-up
DRAM_DATA12	P5	NVCC_DRAM	DDR	ALT0	DRAM_DATA12	Input	100 kΩ pull-up
DRAM_DATA13	P3	NVCC_DRAM	DDR	ALT0	DRAM_DATA13	Input	100 kΩ pull-up
DRAM_DATA14	R2	NVCC_DRAM	DDR	ALT0	DRAM_DATA14	Input	100 kΩ pull-up
DRAM_DATA15	R1	NVCC_DRAM	DDR	ALT0	DRAM_DATA15	Input	100 kΩ pull-up
DRAM_DQM0	T7	NVCC_DRAM	DDR	ALT0	DRAM_DQM0	Output	100 kΩ pull-up
DRAM_DQM1	T3	NVCC_DRAM	DDR	ALT0	DRAM_DQM1	Output	100 kΩ pull-up
DRAM_ODT0	N1	NVCC_DRAM	DDR	ALT0	DRAM_ODT0	Output	100 kΩ pull-down
DRAM_ODT1	F1	NVCC_DRAM	DDR	ALT0	DRAM_ODT1	Output	100 kΩ pull-down
DRAM_RAS_B	M5	NVCC_DRAM	DDR	ALT0	DRAM_RAS_B	Output	100 kΩ pull-up
DRAM_RESET	G4	NVCC_DRAM	DDR	ALT0	DRAM_RESET	Output	100 kΩ pull-down
DRAM_SDBA0	M1	NVCC_DRAM	DDR	ALT0	DRAM_SDBA0	Output	100 kΩ pull-up
DRAM_SDBA1	H1	NVCC_DRAM	DDR	ALT0	DRAM_SDBA1	Output	100 kΩ pull-up
DRAM_SDBA2	K2	NVCC_DRAM	DDR	ALT0	DRAM_SDBA2	Output	100 kΩ pull-up
DRAM_SDCKE0	M3	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE0	Output	100 kΩ pull-down
DRAM_SDCKE1	J3	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE1	Output	100 kΩ pull-down
DRAM_SDCLK0_N	P2	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK0_N	Input	100 kΩ pull-up
DRAM_SDCLK0_P	P1	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK0_P	Input	100 kΩ pull-up
DRAM_SDQS0_N	P7	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS0_N	Input	100 kΩ pull-down

Table 91. 14x14 mm Functional Contact Assignments (continued)

LCD_ENABLE	B8	NVCC_LCD	GPIO	ALT5	LCD_ENABLE	Input	Keeper
LCD_HSYNC	D9	NVCC_LCD	GPIO	ALT5	LCD_HSYNC	Input	Keeper
LCD_RESET	E9	NVCC_LCD	GPIO	ALT5	LCD_RESET	Input	Keeper
LCD_VSYNC	C9	NVCC_LCD	GPIO	ALT5	LCD_VSYNC	Input	Keeper
NAND_ALE	B4	NVCC_NAND	GPIO	ALT5	VDDSOC	Input	Keeper
NAND_CE0_B	C5	NVCC_NAND	GPIO	ALT5	NAND_CE0_B	Input	Keeper
NAND_CE1_B	B5	NVCC_NAND	GPIO	ALT5	NAND_CE1_B	Input	Keeper
NAND_CLE	A4	NVCC_NAND	GPIO	ALT5	NAND_CLE	Input	Keeper
NAND_DATA00	D7	NVCC_NAND	GPIO	ALT5	NAND_DATA00	Input	Keeper
NAND_DATA01	B7	NVCC_NAND	GPIO	ALT5	NAND_DATA01	Input	Keeper
NAND_DATA02	A7	NVCC_NAND	GPIO	ALT5	NAND_DATA02	Input	Keeper
NAND_DATA03	D6	NVCC_NAND	GPIO	ALT5	NAND_DATA03	Input	Keeper
NAND_DATA04	C6	NVCC_NAND	GPIO	ALT5	NAND_DATA04	Input	Keeper
NAND_DATA05	B6	NVCC_NAND	GPIO	ALT5	NAND_DATA05	Input	Keeper
NAND_DATA06	A6	NVCC_NAND	GPIO	ALT5	NAND_DATA06	Input	Keeper
NAND_DATA07	A5	NVCC_NAND	GPIO	ALT5	NAND_DATA07	Input	Keeper
NAND_DQS	E6	NVCC_NAND	GPIO	ALT5	NAND_DQS	Input	Keeper
NAND_RE_B	D8	NVCC_NAND	GPIO	ALT5	NAND_RE_B	Input	Keeper
NAND_READY_B	A3	NVCC_NAND	GPIO	ALT5	NAND_READY_B	Input	Keeper
NAND_WE_B	C8	NVCC_NAND	GPIO	ALT5	NAND_WE_B	Input	Keeper
NAND_WP_B	D5	NVCC_NAND	GPIO	ALT5	NAND_WP_B	Input	Keeper
ONOFF	R8	VDD_SNVS_IN	GPIO	ALT0	ONOFF	Input	100 kΩ pull-up
POR_B	P8	VDD_SNVS_IN	GPIO	ALT0	POR_B	Input	100 kΩ pull-up
RTC_XTALI	T11	VDD_SNVS_CAP	ANALOG	—	RTC_XTALI	—	—
RTC_XTALO	U11	VDD_SNVS_CAP	ANALOG	—	RTC_XTALO	—	—
SD1_CLK	C1	NVCC_SD1	GPIO	ALT5	SD1_CLK	Input	Keeper
SD1_CMD	C2	NVCC_SD1	GPIO	ALT5	SD1_CMD	Input	Keeper
SD1_DATA0	B3	NVCC_SD1	GPIO	ALT5	SD1_DATA0	Input	Keeper
SD1_DATA1	B2	NVCC_SD1	GPIO	ALT5	SD1_DATA1	Input	Keeper
SD1_DATA2	B1	NVCC_SD1	GPIO	ALT5	SD1_DATA2	Input	Keeper
SD1_DATA3	A2	NVCC_SD1	GPIO	ALT5	SD1_DATA3	Input	Keeper
SNVS_PMIC_ON_REQ	T9	VDD_SNVS_IN	GPIO	ALT0	SNVS_PMIC_ON_REQ	Output	100 kΩ pull-up

Table 92. 14x14 mm, 0.8 mm Pitch, Ball Map (continued)

	U	T	R	P
1	VSS	DRAM_SDQS1_P	DRAM_DATA15	DRAM_SDCLK0_P
2	DRAM_DATA08	DRAM_SDQS1_N	DRAM_DATA14	DRAM_SDCLK0_N
3	DRAM_DATA09	DRAM_DQM1	VSS	DRAM_DATA13
4	DRAM_DATA07	DRAM_DATA00	DRAM_DATA11	DRAM_VREF
5	DRAM_DATA10	DRAM_DATA06	VSS	DRAM_DATA12
6	DRAM_DATA01	DRAM_DATA02	SNVS_TAMPER9	DRAM_SDQS0_P
7	DRAM_DATA03	DRAM_DQM0	VSS	DRAM_SDQS0_N
8	DRAM_DATA04	DRAM_DATA05	ONOFF	POR_B
9	CCM_PMIC_STBY_REQ	SNVS_PMIC_ON_REQ	SNVS_TAMPER1	SNVS_TAMPER4
10	BOOT_MODE1	BOOT_MODE0	SNVS_TAMPER0	SNVS_TAMPER3
11	RTC_XTALO	RTC_XTALI	VSS	SNVS_TAMPER2
12	USB_OTG2_VBUS	USB_OTG1_VBUS	VDD_USB_CAP	VDD_SNVS_IN
13	USB_OTG2_DP	USB_OTG2_DN	GPANAIO	NVCC_PLL
14	VSS	VSS	VDD_HIGH_CAP	JTAG_TMS
15	USB_OTG1_DP	USB_OTG1_DN	VDD_HIGH_CAP	JTAG_MOD
16	USB_OTG1_CHD_B	XTALI	VSS	CCM_CLK1_N
17	VSS	XTALO	VSS	CCM_CLK1_P
	U	T	R	P

6.2 9x9 mm package information

6.2.1 9x9 mm, 0.5 mm pitch, ball matrix

Figure 69 shows the top, bottom, and side views of the 9x9 mm BGA package.

Table 95. 9x9 mm, 0.5 mm Pitch, Ball Map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
R	DRAM_DM1	DRAM_DATA11	VSS	DRAM_DATA06	DRAM_SDQS0_N	ONOFF	SNVS_TAMPER6	SNVS_TAMPER0	VSS	POR_B	USB_OTG1_DN	VSS	JTAG_MOD	JTAG_TMS	VSS	JTAG_TDO	JTAG_TCK	R
T	DRAM_VREF	DRAM_ZQPAD	DRAM_DATA00	DRAM_DATA02	DRAM_DATA03	DRAM_DATA05	SNVS_PMIC_ON_REQ	BOOT_MODE0	USB_OTG1_VBUS	USB_OTG2_DN	GPANAIO	RTC_XTALI	NVCC_PLL	XTALI	USB_OTG1_CHD_B	CCM_CLK1_P	VDDA_ADC_3P3	T
U	VSS	DRAM_DATA09	DRAM_DATA07	DRAM_DQM0	DRAM_DATA04	VSS	CCM_PMIC_STBY_REQ	BOOT_MODE1	USB_OTG2_VBUS	USB_OTG2_DP	VDD_HIGH_CAP	RTC_XTALO	VSS	XTALO	VDD_HIGH_IN	CCM_CLK1_N	VSS	U

6.3 GPIO reset behaviors during reset

Table 96 shows the GPIO behaviors during reset.

Table 96. GPIO Behaviors during Reset [1]

Ball Name	Mux Mode	Function	Input/Output	Value
GPIO01_IO03	ALT7	Reserved	Input	100 kΩ pull-down
UART3_TX_DATA	ALT7	SJC_JTAG_ACT	Output	0
LCD_DATA00	ALT6	SRC_BT_CFG[0]	Input	100 kΩ pull-down
LCD_DATA01	ALT6	SRC_BT_CFG[1]	Input	100 kΩ pull-down
LCD_DATA02	ALT6	SRC_BT_CFG[2]	Input	100 kΩ pull-down
LCD_DATA03	ALT6	SRC_BT_CFG[3]	Input	100 kΩ pull-down
LCD_DATA04	ALT6	SRC_BT_CFG[4]	Input	100 kΩ pull-down
LCD_DATA05	ALT6	SRC_BT_CFG[5]	Input	100 kΩ pull-down
LCD_DATA06	ALT6	SRC_BT_CFG[6]	Input	100 kΩ pull-down
LCD_DATA07	ALT6	SRC_BT_CFG[7]	Input	100 kΩ pull-down
LCD_DATA08	ALT6	SRC_BT_CFG[8]	Input	100 kΩ pull-down
LCD_DATA09	ALT6	SRC_BT_CFG[9]	Input	100 kΩ pull-down

Table 96. GPIO Behaviors during Reset (continued)[1]

Ball Name	Mux Mode	Function	Input/Output	Value
LCD_DATA10	ALT6	SRC_BT_CFG[10]	Input	100 kΩ pull-down
LCD_DATA11	ALT6	SRC_BT_CFG[11]	Input	100 kΩ pull-down
LCD_DATA12	ALT6	SRC_BT_CFG[12]	Input	100 kΩ pull-down
LCD_DATA13	ALT6	SRC_BT_CFG[13]	Input	100 kΩ pull-down
LCD_DATA14	ALT6	SRC_BT_CFG[14]	Input	100 kΩ pull-down
LCD_DATA15	ALT6	SRC_BT_CFG[15]	Input	100 kΩ pull-down
LCD_DATA16	ALT6	SRC_BT_CFG[16]	Input	100 kΩ pull-down
LCD_DATA17	ALT6	SRC_BT_CFG[17]	Input	100 kΩ pull-down
LCD_DATA18	ALT6	SRC_BT_CFG[18]	Input	100 kΩ pull-down
LCD_DATA19	ALT6	SRC_BT_CFG[19]	Input	100 kΩ pull-down
LCD_DATA20	ALT6	SRC_BT_CFG[20]	Input	100 kΩ pull-down
LCD_DATA21	ALT6	SRC_BT_CFG[21]	Input	100 kΩ pull-down
LCD_DATA22	ALT6	SRC_BT_CFG[22]	Input	100 kΩ pull-down
LCD_DATA23	ALT6	SRC_BT_CFG[23]	Input	100 kΩ pull-down

[1] Others are same as value in the column “Out of Reset Condition” of Table 91 and Table 94

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