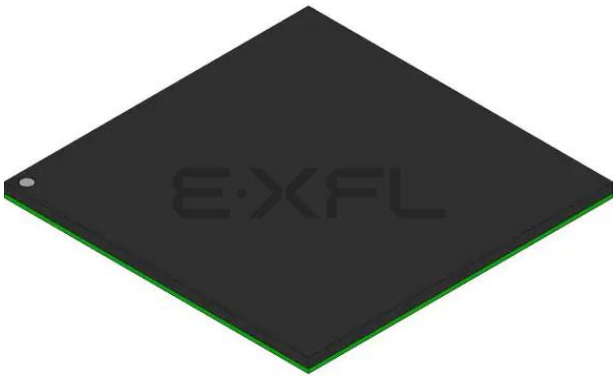

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Table 2. Detailed Peripherals Information (continued)[1,2,3]

Peripheral Name	Instance	G0	G1	G2	G3
Timer/PWM	EPIT1	Y	Y	Y	Y
	EPIT2	NA	Y	Y	Y
	GPT1	Y	Y	Y	Y
	GPT2	NA	Y	Y	Y
	PWM1	Y	Y	Y	Y
	PWM2	Y	Y	Y	Y
	PWM3	Y	Y	Y	Y
	PWM4	Y	Y	Y	Y
	PWM5	NA	Y	Y	Y
	PWM6	NA	Y	Y	Y
	PWM7	NA	Y	Y	Y
	PWM8	NA	Y	Y	Y
ADC	ADC1	Y	Y	Y	Y
	ADC2	NA	NA	Y	Y

[1]For detailed pin mux information, please refer to “Chapter 4 External Signals and Pin Multiplexing” of *i.MX 6UltraLite Reference Manual* (IMX6ULRM).
[2] Y stands for yes, NA stands for not available.
[3] G0 and G3 are not offered in automotive grade.

1.2 Features

The i.MX 6UltraLite processors are based on ARM Cortex-A7 MPCore™ Platform, which has the following features:

- Supports single ARM Cortex-A7 MPCore (with TrustZone) with:
  - 32 KBytes L1 Instruction Cache
  - 32 KBytes L1 Data Cache
  - Private Timer
  - Cortex-A7 NEON Media Processing Engine (MPE) Co-processor
- General Interrupt Controller (GIC) with 128 interrupts support
- Global Timer
- Snoop Control Unit (SCU)
- 128 KB unified I/D L2 cache (on G2 and G3 devices only)
- Single Master AXI bus interface output of L2 cache (for G2 and G3 devices only)
- Frequency of the core (including Neon and L1 cache), as per Table 11, "Operating Ranges," on page 23.

- Four I^2C
- Two 10/100 Ethernet Controller (IEEE1588 compliant)
- Eight Pulse Width Modulators (PWM)
- System JTAG Controller (SJC)
- GPIO with interrupt capabilities
- 8x8 Key Pad Port (KPP)
- One Quad SPI
- Two Flexible Controller Area Network (FlexCAN)
- Three Watchdog timers (WDOG)
- Two 12-bit Analog to Digital Converters (ADC) with up to 10 input channels in total
- Touch Screen Controller (TSC)

The i.MX 6UltraLite processors integrate advanced power management unit and controllers:

- Provide PMU, including LDO supplies, for on-chip resources
- Use Temperature Sensor for monitoring the die temperature
- Use Voltage Sensor for monitoring the die voltage
- Support DVFS techniques for low power modes
- Use SW State Retention and Power Gating for ARM and NEON
- Support various levels of system power modes
- Use flexible clock gating control scheme
- Two smart card interfaces compatible with EVM Standard 4.3

The i.MX 6UltraLite processors use dedicated hardware accelerators to meet the targeted multimedia performance. The use of hardware accelerators is a key factor in obtaining high performance at low power consumption, while having the CPU core relatively free for performing other tasks.

The i.MX 6UltraLite processors incorporate the following hardware accelerators:

- PXP—Pixel Processing Pipeline for imagine resize, rotation, overlay, and CSC[1]. Off loading key pixel processing operations are required to support the LCD display applications.
- ASRC—Asynchronous Sample Rate Converter

Security functions are enabled and accelerated by the following hardware:

- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, etc.)
- SJC—System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- CAAM—Cryptographic Acceleration and Assurance Module, containing cryptographic and hash engines, 32 KB secure RAM, and True and Pseudo Random Number Generator (NIST certified).
- SNVS—Secure Non-Volatile Storage, including Secure Real Time Clock.
- CSU—Central Security Unit. CSU is configured during boot and by eFUSEs and determine the security level operation mode as well as the TZ policy.

1. G2 and G3 only

Table 3. i.MX 6UltraLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
GPMI	General Purpose Memory Interface	Connectivity Peripherals	The GPMI module supports up to 8x NAND devices and 40-bit ECC for NAND Flash Controller (GPMI2). GPMI supports separate DMA channels for each NAND device.
GPT1 GPT2	General Purpose Timer	Timer peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
LCDIF	LCD interface	Connectivity peripherals	The LCDIF is a general purpose display controller used to drive a wide range of display devices varying in size and capability. The LCDIF is designed to support dumb (synchronous 24-bit Parallel RGB interface) and smart (asynchronous parallel MPU interface) LCD devices.
MQS	Medium Quality Sound	Multimedia Peripherals	MQS is used to generate 2-channel medium quality PWM-like audio via two standard digital GPIO pins.
PWM1 PWM2 PWM3 PWM4 PWM5 PWM6 PWM7 PWM8	Pulse Width Modulation	Connectivity peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
PXP	Pixel Processing Pipeline	Display peripherals	A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma-mapping, and rotation. The PXP is enhanced with features specifically for gray scale applications. In addition, the PXP supports traditional pixel/frame processing paths for still-image and video processing applications, allowing it to interface with the integrated EPD.

3.1 Special signal considerations

Table 4 lists special signal considerations for the i.MX 6UltraLite processors. The signal names are listed in alphabetical order.

The package contact assignments can be found in Section 6, "Package information and contact assignments"." Signal descriptions are provided in the *i.MX 6UltraLite Reference Manual* (IMX6ULRM).

Table 4. Special Signal Considerations

Signal Name	Remarks
CCM_CLK1_P/ CCM_CLK1_N	One general purpose differential high speed clock Input/output is provided. It can be used: • To feed external reference clock to the PLLs and further to the modules inside SoC. • To output internal SoC clock to be used outside the SoC as either reference clock or as a functional clock for peripherals. See the *i.MX 6UltraLite Reference Manual* (IMX6ULRM) for details on the respective clock trees. Alternatively one may use single ended signal to drive CLK1_P input. In this case corresponding CLK1_N input should be tied to the constant voltage level equal 1/2 of the input signal swing. Termination should be provided in case of high frequency signals. After initialization, the CLK1 input/output can be disabled (if not used). If unused either or both of the CLK1_N/P pairs may be remain unconnected.
RTC_XTALI/RTC_XTALO	If the user wishes to configure RTC_XTALI and RTC_XTALO as an RTC oscillator, a 32.768 kHz crystal, (≤100 kΩ ESR, 10 pF load) should be connected between RTC_XTALI and RTC_XTALO. Keep in mind the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from RTC_XTALI and RTC_XTALO to either power or ground (>100 MΩ). This will debias the amplifier and cause a reduction of startup margin. Typically RTC_XTALI and RTC_XTALO should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into RTC_XTALI, the RTC_XTALO pin must remain unconnected or driven with a complimentary signal. The logic level of this forcing clock should not exceed VDD_SNVS_CAP level and the frequency should be <100 kHz under typical conditions. In case when high accuracy real time clock are not required system may use internal low frequency ring oscillator. It is recommended to connect RTC_XTALI to GND and keep RTC_XTALO unconnected.
XTALI/XTALO	A 24.0 MHz crystal should be connected between XTALI and XTALO. The crystal must be rated for a maximum drive level of 250 μW. An ESR (equivalent series resistance) of typical 80 Ω is recommended. NXP BSP (board support package) software requires 24 MHz on XTALI/XTALO. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTALO must be directly driven by the external oscillator and XTALI mounted with 18 pF capacitor. Please refer to the EVK board reference design for details. The logic level of this forcing clock cannot exceed NVCC_PLL level. If this clock is used as a reference for USB, then there are strict frequency tolerance and jitter requirements. See OSC24M chapter and relevant interface specifications chapters for details.

The RTC_XTALI is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watch-dog counters. The clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier. Additionally, there is an internal ring oscillator, which can be used instead of the RTC_XTALI if accuracy is not important.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier.

Table 13 shows the interface frequency requirements.

Table 13. External Input Clock Frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
RTC_XTALI Oscillator[1,2]	f_{ckil}	—	32.768[3]/32.0	—	kHz
XTALI Oscillator[2,4]	f_{xtal}	—	24	—	MHz

1 External oscillator or a crystal with internal oscillator amplifier.

2 The required frequency stability of this clock source is application dependent. For recommendations, see the Hardware Development Guide for *i.MX 6UltraLite Applications Processors* (IMX6ULHDG).

3 Recommended nominal frequency 32.768 kHz.

4 External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 13 are required for use with NXP BSPs to ensure precise time keeping and USB operation. For RTC_XTALI operation, two clock sources are available.

- On-chip 40 kHz ring oscillator—this clock source has the following characteristics:
  - Approximately 25 µA more Idd than crystal oscillator
  - Approximately ±50% tolerance
  - No external component required
  - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit:
  - At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
  - Higher accuracy than ring oscillator
  - If no external crystal is present, then the ring oscillator is utilized

The decision of choosing a clock source should be taken based on real-time clock use and precision time-out.

4.1.5 Maximum supply currents

The data shown in Table 14 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

Table 25. LPDDR2 I/O DC Electrical Parameters[1] (continued)

Parameters	Symbol	Test Conditions	Min	Max	Unit
DC High-Level input voltage	Vih_DC	—	Vref+0.13	OVDD	V
DC Low-Level input voltage	Vil_DC	—	OVSS	Vref-0.13	V
Differential Input Logic High	Vih_diff	—	0.26	Note[2]	—
Differential Input Logic Low	Vil_diff	—	Note[2]	-0.26	—
Pull-up/Pull-down Impedance Mismatch	Mmpupd	—	-15	15	%
240 Ω unit calibration resolution	Rres	—	—	10	Ω
Keeper Circuit Resistance	Rkeep	—	110	175	kΩ
Input current (no pull-up/down)	Iin	VI = 0, VI = OVDD	-2.5	2.5	μA

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

4.6.3.2 DDR3/DDR3L mode I/O DC parameters

The parameters in Table 27 are guaranteed per the operating ranges in Table 11, unless otherwise noted.

Table 27. DDR3/DDR3L I/O DC Electrical Characteristics

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	VOH	Ioh= -0.1mA Voh (for ipp_dse=001)	0.8*OVDD[1]	—	V
Low-level output voltage	VOL	Iol= 0.1mA Vol (for ipp_dse=001)	0.2*OVDD	—	V
High-level output voltage	VOH	Ioh= -1mA Voh (for all except ipp_dse=001)	0.8*OVDD	—	V
Low-level output voltage	VOL	Iol= 1mA Vol (for all except ipp_dse=001)	0.2*OVDD	—	V
Input Reference Voltage	Vref	—	0.49*ovdd	0.51*ovdd	V
DC High-Level input voltage	Vih_DC	—	Vref[2]+0.1	OVDD	V
DC Low-Level input voltage	Vil_DC	—	OVSS	Vref-0.1	V
Differential Input Logic High	Vih_diff	—	0.2	—	V
Differential Input Logic Low	Vil_diff	—	—	-0.2	V
Termination Voltage	Vtt	Vtt tracking OVDD/2	0.49*OVDD	0.51*OVDD	V
Pull-up/Pull-down Impedance Mismatch	Mmpupd	—	-10	10	%
240 Ω unit calibration resolution	Rres	—	—	10	Ω
Keeper Circuit Resistance	Rkeep	—	105	165	kΩ
Input current (no pull-up/down)	Iin	VI = 0,VI = OVDD	-2.9	2.9	μA

1 OVDD – I/O power supply (1.425 V–1.575 V for DDR3 and 1.283 V–1.45 V for DDR3L)

4.9.3 External Interface Module (EIM)

The following subsections provide information on the EIM. Maximum operating frequency for EIM data transfer is 104 MHz. Timing parameters in this section that are given as a function of register settings or clock periods are valid for the entire range of allowed frequencies (0–104 MHz).

4.9.3.1 EIM interface pads allocation

EIM supports 16-bit and 8-bit devices operating in address/data separate or multiplexed modes. Table 38 provides EIM interface pads allocation in different modes.

Table 38. EIM Internal Module Multiplexing[1]

Setup	Non Multiplexed Address/Data Mode						Multiplexed Address/Data mode
	8 Bit				16 Bit		16 Bit
	MUM = 0, DSZ = 100	MUM = 0, DSZ = 101	MUM = 0, DSZ = 110	MUM = 0, DSZ = 111	MUM = 0, DSZ = 001	MUM = 0, DSZ = 010	MUM = 1, DSZ = 001
EIM_ADDR [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]
EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]
EIM_DATA [07:00], EIM_EB0_B	EIM_DATA [07:00]	—	Reserved	Reserved	EIM_DATA [07:00]	Reserved	EIM_AD [07:00]
EIM_DATA [15:08], EIM_EB1_B	—	EIM_DATA [15:08]	Reserved	Reserved	EIM_DATA [15:08]	Reserved	EIM_AD [15:08]

[1] For more information on configuration ports mentioned in this table, see the *i.MX 6UltraLite Reference Manual (IMX6ULRM)*.

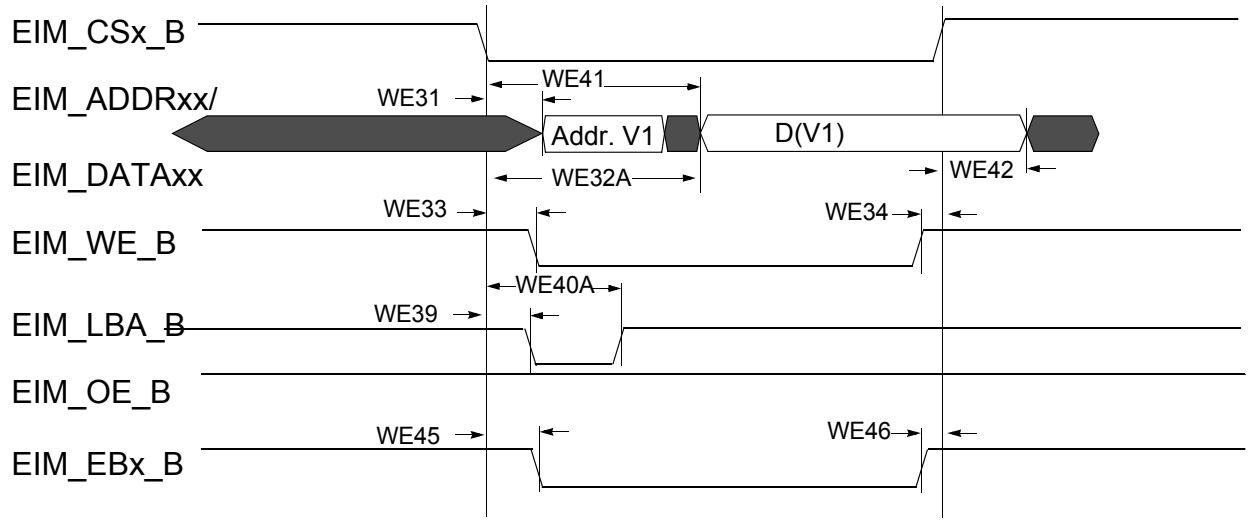

Figure 18. Asynchronous A/D Muxed Write Access

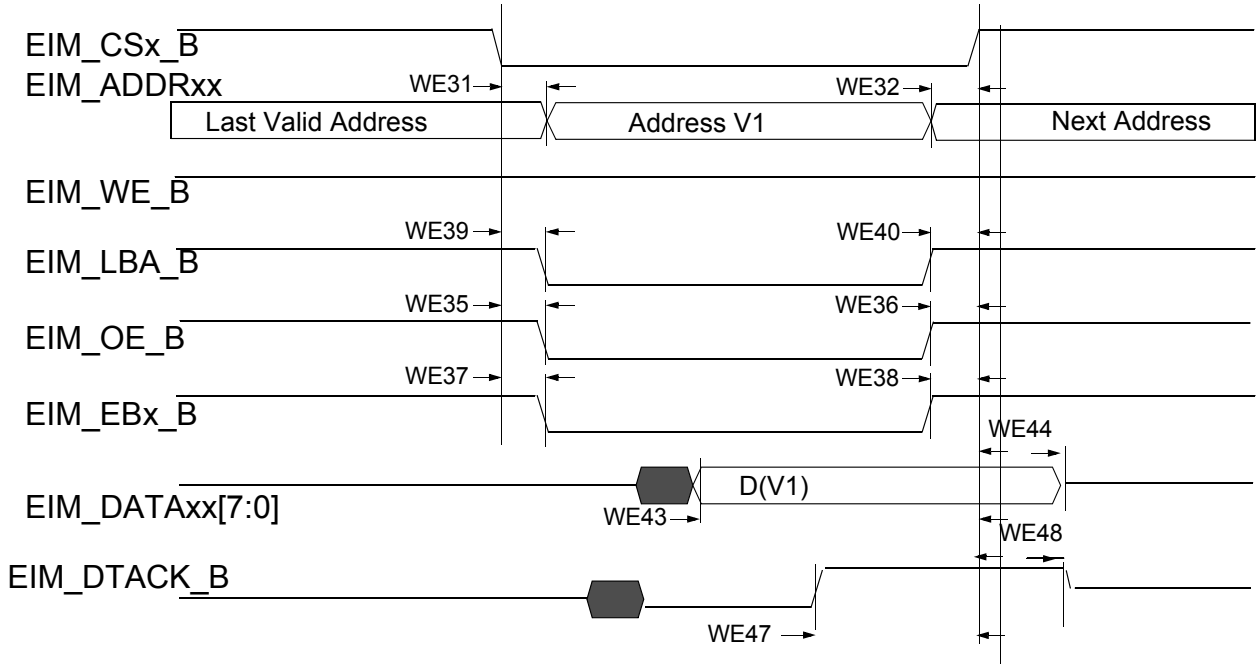

Figure 19. DTACK Mode Read Access (DAP=0)

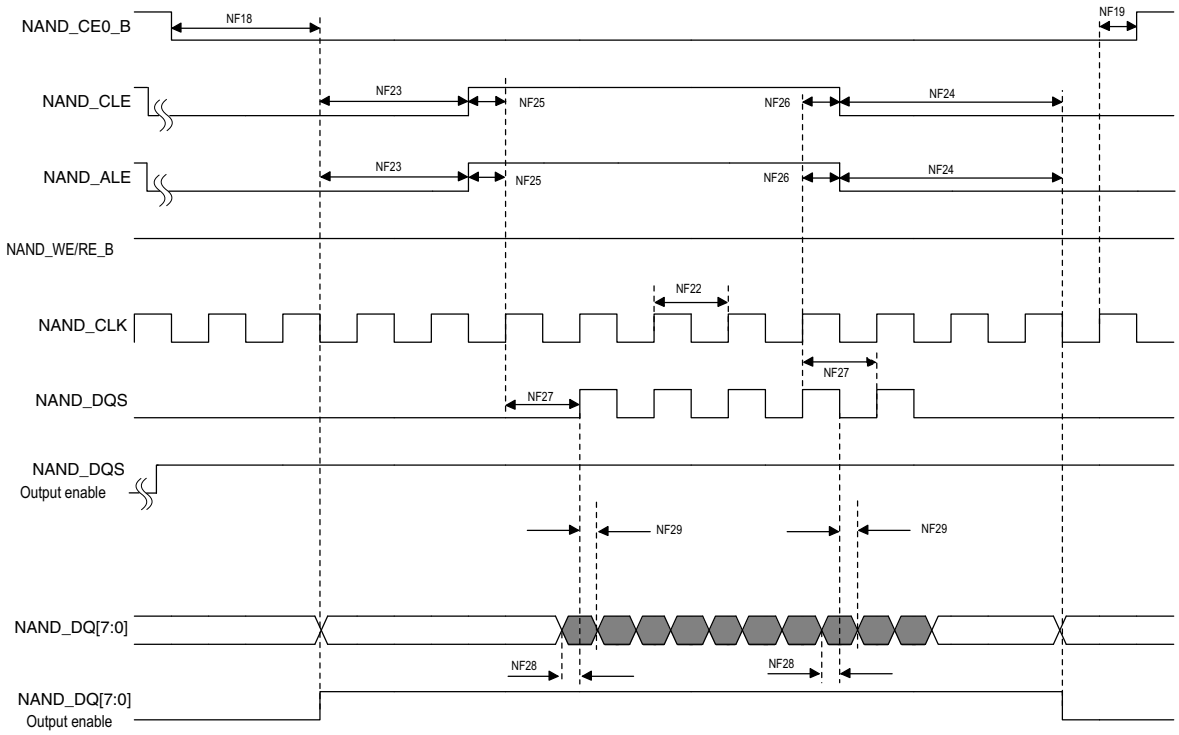

Figure 27. Source Synchronous Mode Data Write Timing Diagram

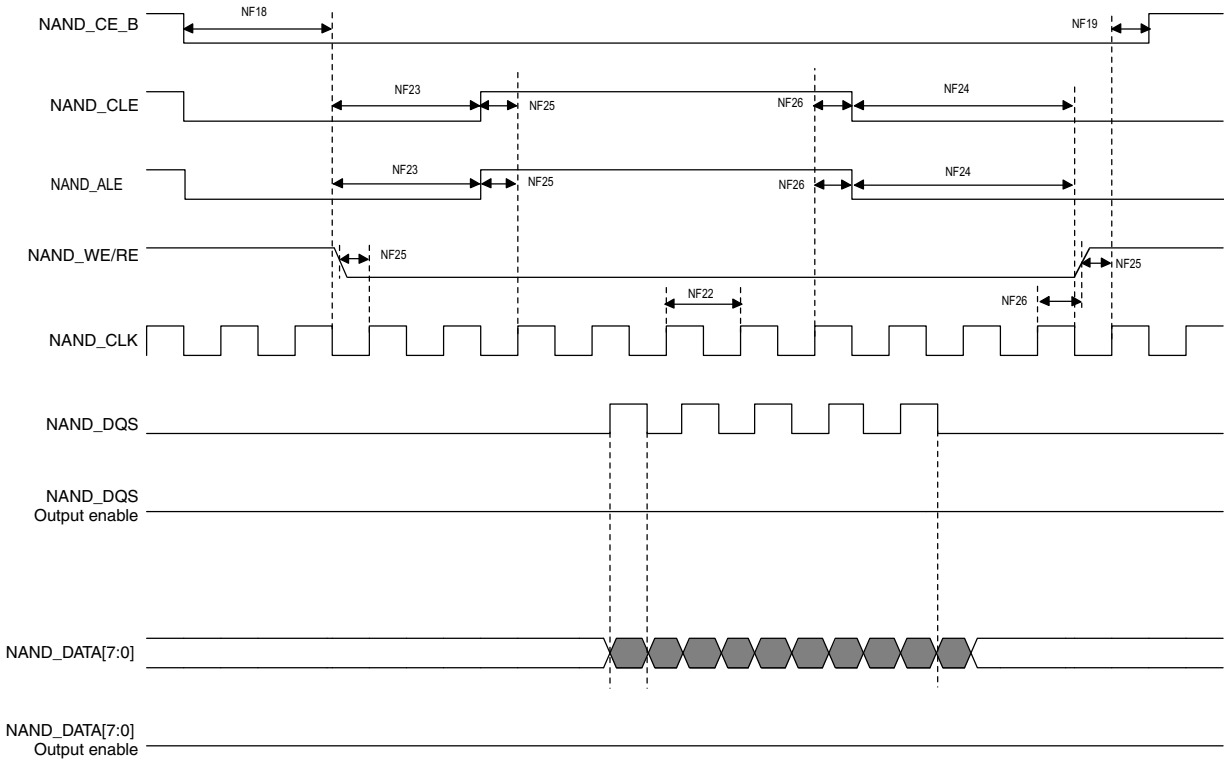

Figure 28. Source Synchronous Mode Data Read Timing Diagram

Table 61. LCD Signal Parameters (continued)

LCD_D12 / ENABLE**	—	R[1]	R[0]	G[4]	—
LCD_D11	—	R[0]	G[5]	G[3]	—
LCD_D10	—	G[5]	G[4]	G[2]	—
LCD_D9	—	G[4]	G[3]	G[1]	—
LCD_D8	—	G[3]	G[2]	G[0]	—
LCD_D8	—	G[3]	G[2]	G[0]	—
LCD_D7	R[2]	G[2]	G[1]	B[7]	Y/C[7]
LCD_D6	R[1]	G[1]	G[0]	B[6]	Y/C[6]
LCD_D5	R[0]	G[0]	B[5]	B[5]	Y/C[5]
LCD_D4	G[2]	B[4]	B[4]	B[4]	Y/C[4]
LCD_D3	G[1]	B[3]	B[3]	B[3]	Y/C[3]
LCD_D2	G[0]	B[2]	B[2]	B[2]	Y/C[2]
LCD_D1	B[1]	B[1]	B[1]	B[1]	Y/C[1]
LCD_D0	B[0]	B[0]	B[0]	B[0]	Y/C[0]
LCD_RESET	LCD_RESET	LCD_RESET	LCD_RESET	LCD_RESET	—
LCD_BUSY / LCD_VSYNC	LCD_BUSY (or optional LCD_VSYNC)	LCD_BUSY (or optional LCD_VSYNC)	LCD_BUSY (or optional LCD_VSYNC)	LCD_BUSY (or optional LCD_VSYNC)	—

4.12.9 QUAD SPI (QSPI) timing parameters

Measurement conditions are with 35 pF load on SCK and SIO pins and input slew rate of 1 V/ns.

4.12.9.1 SDR mode

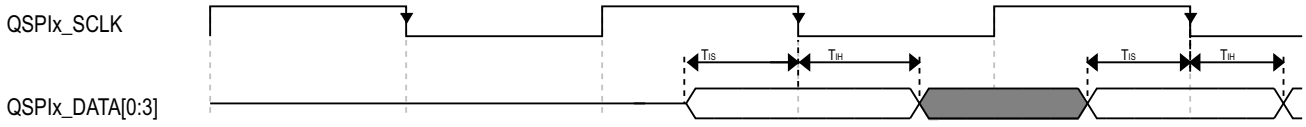

Figure 49. QuadSPI Input/Read Timing (SDR mode with internal sampling)

Table 64. QuadSPI Output/Write Timing (SDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{DVO}	Output data valid time	—	2	ns
T_{DHO}	Output data hold time	0	—	ns
T_{CK}	SCK clock period	10	—	ns
T_{CSS}	Chip select output setup time	3	—	SCK cycle(s)
T_{CSH}	Chip select output hold time	3	—	SCK cycle(s)

NOTE

T_{css} and T_{csh} are configured by the QuadSPIx_FLSHCR register, the default value of 3 are shown on the timing. Please refer to the *i.MX 6UltraLite Reference Manual (IMX6ULRM)* for more details.

4.12.9.2 DDR mode

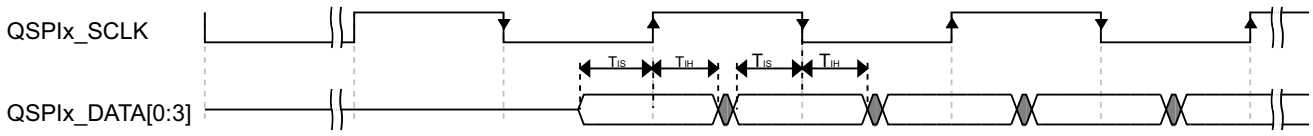

Figure 52. QuadSPI Input/Read Timing (DDR mode with internal sampling)

Table 65. QuadSPI Input/Read Timing (DDR mode with internal sampling)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{IS}	Setup time for incoming data	8.67	—	ns
T_{IH}	Hold time requirement for incoming data	0	—	ns

2 DC potential differences

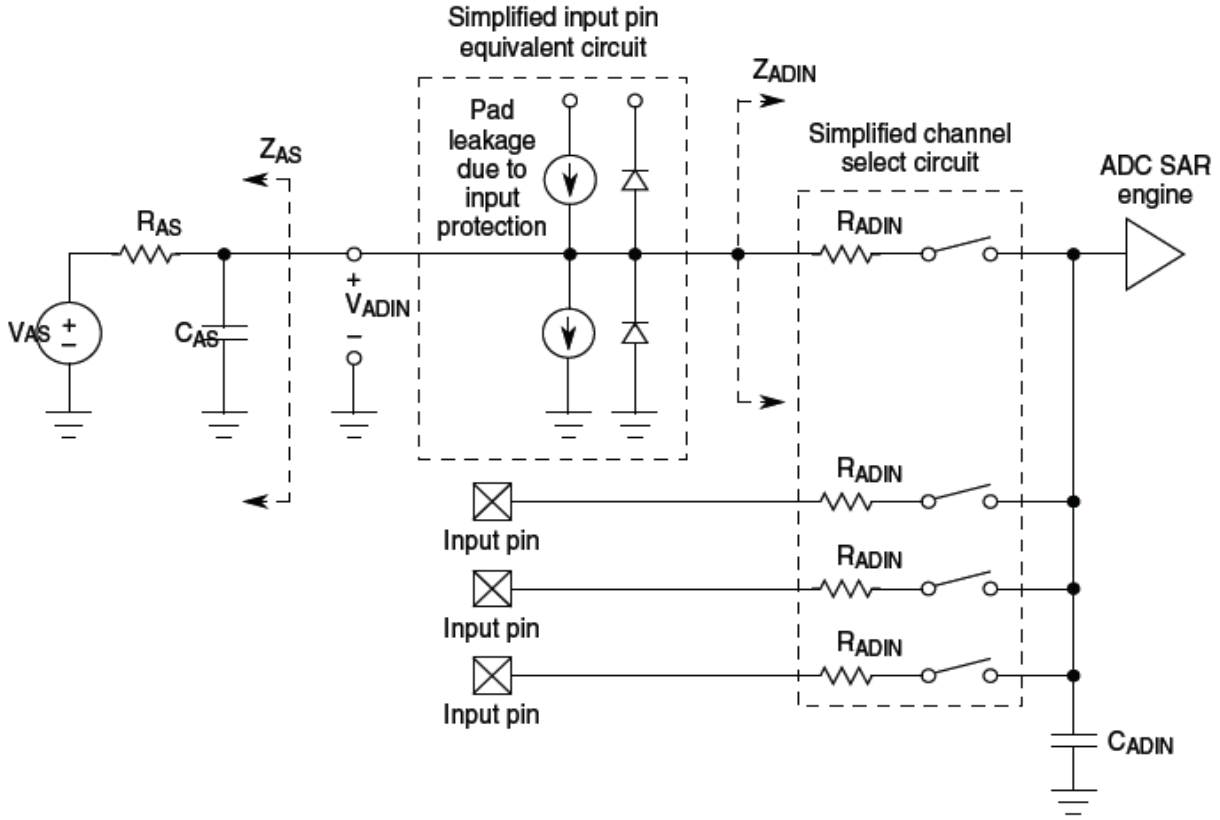

Figure 67. 12-bit ADC Input Impedance Equivalency Diagram

4.13.1.1.1 12-bit ADC characteristics

Table 77. 12-bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$)

Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	Comment
[L:] Supply Current	ADLPC=1, ADHSC=0	I_{DDAD}	—	250	—	μA	ADLSMP=0 ADSTS=10 ADCO=1
	ADLPC=0, ADHSC=0			350			
	ADLPC=0, ADHSC=1			400			
[L:] Supply Current	Stop, Reset, Module Off	I_{DDAD}	—	0.01	0.8	μA	—
ADC Asynchronous Clock Source	ADHSC=0	f_{ADACK}	—	10	—	MHz	$t_{ADACK} = 1/f_{ADACK}$
	ADHSC=1		—	20	—		

Table 84. NAND Boot through GPMI (continued)

Ball Name	Signal Name	Mux Mode	Common	BOOT_CFG1[3:2]= 01b	BOOT_CFG1[3:2]= 10b
NAND_DATA00	rawnand.DATA00	Alt 0	Yes		
NAND_DATA01	rawnand.DATA01	Alt 0	Yes		
NAND_DATA02	rawnand.DATA02	Alt 0	Yes		
NAND_DATA03	rawnand.DATA03	Alt 0	Yes		
NAND_DATA04	rawnand.DATA04	Alt 0	Yes		
NAND_DATA05	rawnand.DATA05	Alt 0	Yes		
NAND_DATA06	rawnand.DATA06	Alt 0	Yes		
NAND_DATA07	rawnand.DATA07	Alt 0	Yes		
NAND_DQS	rawnand.DQS	Alt 0	Yes		
CSI_MCLK	rawnand.CE2_B	Alt 2			Yes
CSI_PIXCLK	rawnand.CE3_B	Alt 2			Yes

Table 85. SD/MMC Boot through USDHC1

Ball Name	Signal Name	Mux Mode	Common	4-bit	8-bit	BOOT_CFG1[1]=1 (SD Power Cycle)	SDMMC MFG mode
UART1_RTS_B	usdhc1.CD_B	Alt 2					Yes
SD1_CLK	usdhc1.CLK	Alt 0	Yes				
SD1_CMD	usdhc1.CMD	Alt 0	Yes				
SD1_DATA0	usdhc1.DATA0	Alt 0	Yes				
SD1_DATA1	usdhc1.DATA1	Alt 0		Yes	Yes		
SD1_DATA2	usdhc1.DATA2	Alt 0		Yes	Yes		
SD1_DATA3	usdhc1.DATA3	Alt 0	Yes				
NAND_READY_B	usdhc1.DATA4	Alt 1			Yes		
NAND_CE0_B	usdhc1.DATA5	Alt 1			Yes		
NAND_CE1_B	usdhc1.DATA6	Alt 1			Yes		
NAND_CLE	usdhc1.DATA7	Alt 1			Yes		
GPIO1_IO09	usdhc1.RESET_B	Alt 5				Yes	
GPIO1_IO05	usdhc1.VSELECT	Alt 4				Yes	

6 Package information and contact assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 14x14 mm package information

6.1.1 14x14 mm, 0.8 mm pitch, ball matrix

Figure 68 shows the top, bottom, and side views of the 14x14 mm BGA package.

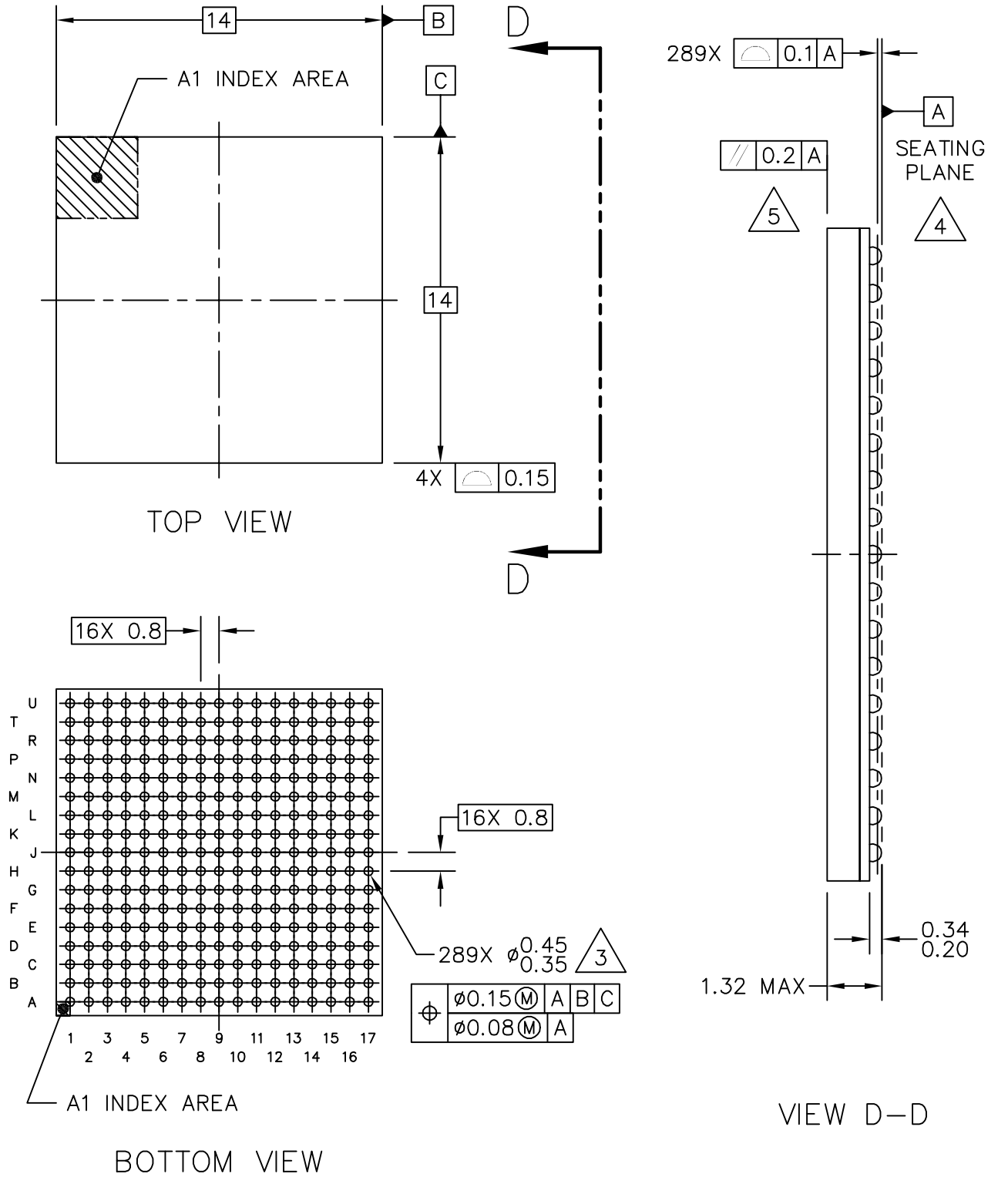

Figure 68. 14x14 mm BGA, Case x Package Top, Bottom, and Side Views

Table 91. 14x14 mm Functional Contact Assignments (continued)

DRAM_ADDR07	H4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR07	Output	100 kΩ pull-up
DRAM_ADDR08	J4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR08	Output	100 kΩ pull-up
DRAM_ADDR09	L2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR09	Output	100 kΩ pull-up
DRAM_ADDR10	M4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR10	Output	100 kΩ pull-up
DRAM_ADDR11	K3	NVCC_DRAM	DDR	ALT0	DRAM_ADDR11	Output	100 kΩ pull-up
DRAM_ADDR12	L4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR12	Output	100 kΩ pull-up
DRAM_ADDR13	H3	NVCC_DRAM	DDR	ALT0	DRAM_ADDR13	Output	100 kΩ pull-up
DRAM_ADDR14	G1	NVCC_DRAM	DDR	ALT0	DRAM_ADDR14	Output	100 kΩ pull-up
DRAM_ADDR15	K5	NVCC_DRAM	DDR	ALT0	DRAM_ADDR15	Output	100 kΩ pull-up
DRAM_CAS_B	J2	NVCC_DRAM	DDR	ALT0	DRAM_CAS_B	Output	100 kΩ pull-up
DRAM_CS0_B	N2	NVCC_DRAM	DDR	ALT0	DRAM_CS0_B	Output	100 kΩ pull-up
DRAM_CS1_B	H5	NVCC_DRAM	DDR	ALT0	DRAM_CS1_B	Output	100 kΩ pull-up
DRAM_DATA00	T4	NVCC_DRAM	DDR	ALT0	DRAM_DATA00	Input	100 kΩ pull-up
DRAM_DATA01	U6	NVCC_DRAM	DDR	ALT0	DRAM_DATA01	Input	100 kΩ pull-up
DRAM_DATA02	T6	NVCC_DRAM	DDR	ALT0	DRAM_DATA02	Input	100 kΩ pull-up
DRAM_DATA03	U7	NVCC_DRAM	DDR	ALT0	DRAM_DATA03	Input	100 kΩ pull-up
DRAM_DATA04	U8	NVCC_DRAM	DDR	ALT0	DRAM_DATA04	Input	100 kΩ pull-up
DRAM_DATA05	T8	NVCC_DRAM	DDR	ALT0	DRAM_DATA05	Input	100 kΩ pull-up
DRAM_DATA06	T5	NVCC_DRAM	DDR	ALT0	DRAM_DATA06	Input	100 kΩ pull-up
DRAM_DATA07	U4	NVCC_DRAM	DDR	ALT0	DRAM_DATA07	Input	100 kΩ pull-up
DRAM_DATA08	U2	NVCC_DRAM	DDR	ALT0	DRAM_DATA08	Input	100 kΩ pull-up

Table 91. 14x14 mm Functional Contact Assignments (continued)

USB_OTG1_CHD_B	U16	OPEN DRAIN	GPIO	—	USB_OTG1_CHD_B	—	—
USB_OTG1_DN	T15	VDD_USB_CAP	ANALOG	—	USB_OTG1_DN	—	—
USB_OTG1_DP	U15	VDD_USB_CAP	ANALOG	—	USB_OTG1_DP	—	—
USB_OTG1_VBUS	T12	USB_VBUS	VBUS POWER	—	USB_OTG1_VBUS	—	—
USB_OTG2_DN	T13	VDD_USB_CAP	ANALOG	—	USB_OTG2_DN	—	—
USB_OTG2_DP	U13	VDD_USB_CAP	ANALOG	—	USB_OTG2_DP	—	—
USB_OTG2_VBUS	U12	USB_VBUS	VBUS POWER	—	USB_OTG2_VBUS	—	—
XTALI	T16	NVCC_PLL	ANALOG	—	XTALI	—	—
XTALO	T17	NVCC_PLL	ANALOG	—	XTALO	—	—

[1] SNVS_TAMPER0 to SNVS_TAMPER9 can be configured as GPIO or tamper detection pin, it is depending on the fuse setting TAMPER_PIN_DISABLE[1:0].

Table 92. 14x14 mm, 0.8 mm Pitch, Ball Map (continued)

N	M	L	K	J	H	G
DRAM_ODT0	DRAM_SDBA0	DRAM_ADDR05	DRAM_ADDR02	DRAM_SDWE_B	DRAM_SDBA1	DRAM_ADDR14
DRAM_CS0_B	DRAM_ADDR03	DRAM_ADDR09	DRAM_SDBA2	DRAM_CAS_B	DRAM_ADDR01	DRAM_ADDR06
VSS	DRAM_SDCKE0	VSS	DRAM_ADDR11	DRAM_SDCKE1	DRAM_ADDR13	VSS
DRAM_ZQPAD	DRAM_ADDR10	DRAM_ADDR12	DRAM_ADDR04	DRAM_ADDR08	DRAM_ADDR07	DRAM_RESET
VSS	DRAM_RAS_B	DRAM_ADDR00	DRAM_ADDR15	VSS	DRAM_CS1_B	VSS
NVCC_DRAM_2P5	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM
TEST_MODE	VSS	VSS	VSS	VSS	VSS	VSS
SNVS_TAMPER5	VSS	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP
SNVS_TAMPER8	VSS	VDD_SOC_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_CAP
SNVS_TAMPER7	VSS	VDD_SOC_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_CAP
SNVS_TAMPER6	VSS	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_ARM_CAP	VDD_ARM_CAP
VDD_SNVS_CAP	NGND_KEL0	VSS	VSS	VSS	VSS	VSS
VDD_HIGH_IN	ADC_VREFH	VDDA_ADC_3P3	GPIO1_IO00	NVCC_GPIO	NVCC_UART	UART5_RX_DATA
JTAG_TRST_B	JTAG_TCK	GPIO1_IO02	UART1_TX_DATA	UART1_RTS_B	UART2_RTS_B	UART3_RTS_B
JTAG_TDO	GPIO1_IO09	GPIO1_IO01	UART1_CTS_B	UART2_CTS_B	UART3_CTS_B	VSS
JTAG_TDI	GPIO1_IO04	GPIO1_IO07	UART1_RX_DATA	UART2_RX_DATA	UART3_RX_DATA	UART4_RX_DATA
GPIO1_IO08	GPIO1_IO05	GPIO1_IO03	GPIO1_IO06	UART2_TX_DATA	UART3_TX_DATA	UART4_TX_DATA
N	M	L	K	J	H	G

Table 95. 9x9 mm, 0.5 mm Pitch, Ball Map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
R	DRAM_DM1	DRAM_DATA11	VSS	DRAM_DATA06	DRAM_SDQS0_N	ONOFF	SNVS_TAMPER6	SNVS_TAMPER0	VSS	POR_B	USB_OTG1_DN	VSS	JTAG_MOD	JTAG_TMS	VSS	JTAG_TDO	JTAG_TCK	R
T	DRAM_VREF	DRAM_ZQPAD	DRAM_DATA00	DRAM_DATA02	DRAM_DATA03	DRAM_DATA05	SNVS_PMIC_ON_REQ	BOOT_MODE0	USB_OTG1_VBUS	USB_OTG2_DN	GPANAIO	RTC_XTALI	NVCC_PLL	XTALI	USB_OTG1_CHD_B	CCM_CLK1_P	VDDA_ADC_3P3	T
U	VSS	DRAM_DATA09	DRAM_DATA07	DRAM_DQM0	DRAM_DATA04	VSS	CCM_PMIC_STBY_REQ	BOOT_MODE1	USB_OTG2_VBUS	USB_OTG2_DP	VDD_HIGH_CAP	RTC_XTALO	VSS	XTALO	VDD_HIGH_IN	CCM_CLK1_N	VSS	U

6.3 GPIO reset behaviors during reset

Table 96 shows the GPIO behaviors during reset.

Table 96. GPIO Behaviors during Reset [1]

Ball Name	Mux Mode	Function	Input/Output	Value
GPIO01_IO03	ALT7	Reserved	Input	100 kΩ pull-down
UART3_TX_DATA	ALT7	SJC_JTAG_ACT	Output	0
LCD_DATA00	ALT6	SRC_BT_CFG[0]	Input	100 kΩ pull-down
LCD_DATA01	ALT6	SRC_BT_CFG[1]	Input	100 kΩ pull-down
LCD_DATA02	ALT6	SRC_BT_CFG[2]	Input	100 kΩ pull-down
LCD_DATA03	ALT6	SRC_BT_CFG[3]	Input	100 kΩ pull-down
LCD_DATA04	ALT6	SRC_BT_CFG[4]	Input	100 kΩ pull-down
LCD_DATA05	ALT6	SRC_BT_CFG[5]	Input	100 kΩ pull-down
LCD_DATA06	ALT6	SRC_BT_CFG[6]	Input	100 kΩ pull-down
LCD_DATA07	ALT6	SRC_BT_CFG[7]	Input	100 kΩ pull-down
LCD_DATA08	ALT6	SRC_BT_CFG[8]	Input	100 kΩ pull-down
LCD_DATA09	ALT6	SRC_BT_CFG[9]	Input	100 kΩ pull-down

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