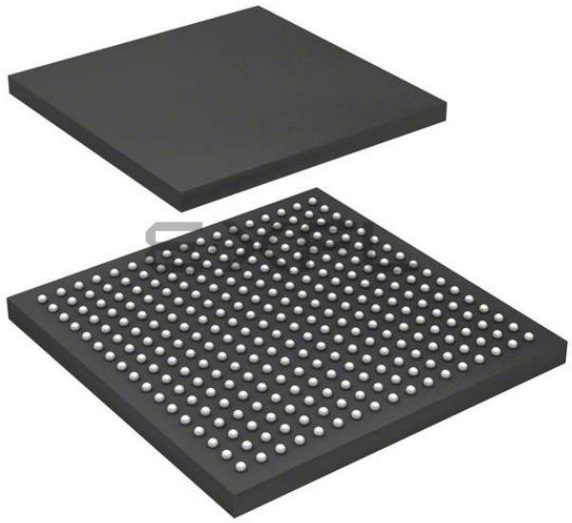

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A7
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	528MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	LCD, LVDS
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	ARM TZ, A-HAB, CAAM, CSU, SJC, SNVS
Package / Case	289-LFBGA
Supplier Device Package	289-MAPBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6g3dvm05ab

- IoT Gateway
- Access control panels
- Human Machine Interfaces (HMI)
- Smart appliances

The features of the i.MX 6UltraLite processor include[1]:

- Single-core ARM Cortex-A7—The single core A7 provides a cost-effective and power-efficient solution.
- Multilevel memory system—The multilevel memory system of each device is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The device supports many types of external memory devices, including DDR3, low voltage DDR3, LPDDR2, NOR Flash, NAND Flash (MLC and SLC), OneNAND™, Quad SPI, and managed NAND, including eMMC up to rev 4.4/4.41/4.5.
- Smart speed technology—Power management implemented throughout the IC that enables multimedia features and peripherals to consume minimum power in both active and various low power modes.
- Dynamic voltage and frequency scaling—The processor improves the power efficiency by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—Multimedia performance is enhanced by a multilevel cache system, NEON™ MPE (Media Processor Engine) co-processor, a programmable smart DMA (SDMA) controller, an asynchronous audio sample rate converter, and a Pixel processing pipeline (PXP) to support 2D image processing, including color-space conversion, scaling, alpha-blending, and rotation.
- Ethernet interfaces—10/100 Mbps Ethernet controllers.
- Human-machine interface—Support digital parallel display interface.
- Interface flexibility—Each processor supports connections to a variety of interfaces: High-speed USB on-the-go with PHY, multiple expansion card port (high-speed MMC/SDIO host and other), 12-bit ADC module, CAN port, smart card interface compatible with EMV Standard v4.3, and a variety of other popular interfaces (such as UART, I^2C, and I^2S serial audio).
- Advanced security—The processor delivers hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. The security features are discussed in detail in the *i.MX 6UltraLite Security Reference Manual* (IMX6ULSRM).
- Integrated power management—The processor integrates linear regulators and internally generate voltage levels for different domains. This significantly simplifies system power management structure.

For a comprehensive list of the i.MX 6UltraLite features, see Section 1.2, “Features"”.

1. The actual feature set depends on the part numbers as described in the Table 1 and Table 2.

1.1 Ordering information

Table 1 provides examples of orderable part numbers covered by this data sheet.

Table 1. Ordering Information

Part Number	Feature	Package	Junction Temperature T_j (°C)
MCIMX6G0DVM05AA	Single Core, 528 MHz	14 x 14 mm, 0.8 pitch, BGA	0 to +95
MCIMX6G0DVM05AB	Single Core, 528 MHz	14 x 14 mm, 0.8 pitch, BGA	0 to +95
MCIMX6G2DVM05AA	Single Core, 528 MHz	14 x 14 mm, 0.8 pitch, BGA	0 to +95
MCIMX6G2DVM05AB	Single Core, 528 MHz	14 x 14 mm, 0.8 pitch, BGA	0 to +95
MCIMX6G3DVM05AA	Single Core, 528 MHz	14 x 14 mm, 0.8 pitch, BGA	0 to +95
MCIMX6G3DVM05AB	Single Core, 528 MHz	14 x 14 mm, 0.8 pitch, BGA	0 to +95
MCIMX6G2DVK05AA	Single Core, 528 MHz	9 x 9 mm, 0.5 pitch, BGA	0 to +95
MCIMX6G2DVK05AB	Single Core, 528 MHz	9 x 9 mm, 0.5 pitch, BGA	0 to +95
MCIMX6G3DVK05AA	Single Core, 528 MHz	9 x 9 mm, 0.5 pitch, BGA	0 to +95
MCIMX6G3DVK05AB	Single Core, 528 MHz	9 x 9 mm, 0.5 pitch, BGA	0 to +95

Figure 1 describes the part number nomenclature so that characteristics of a specific part number can be identified (for example, cores, frequency, temperature grade, fuse options, and silicon revision). The primary characteristic which describes which data sheet applies to a specific part is the temperature grade (junction) field.

- The i.MX 6UltraLite Applications Processors for Consumer Products data sheet (IMX6ULCEC) covers parts listed with a “D (Consumer temp)”

Ensure to have the proper data sheet for specific part by verifying the temperature grade (junction) field and matching it to the proper data sheet. If there are any questions, visit the web page nxp.com/imx6series or contact an NXP representative for details.

- A-HAB—Advanced High Assurance Boot—HABv4 with the new embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization.

NOTE

The actual feature set depends on the part numbers as described in Table 1 and Table 2. Functions such as display and camera interfaces, connectivity interfaces, and security features are not offered on all derivatives.

Table 3. i.MX 6UltraLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
GPMI	General Purpose Memory Interface	Connectivity Peripherals	The GPMI module supports up to 8x NAND devices and 40-bit ECC for NAND Flash Controller (GPMI2). GPMI supports separate DMA channels for each NAND device.
GPT1 GPT2	General Purpose Timer	Timer peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
LCDIF	LCD interface	Connectivity peripherals	The LCDIF is a general purpose display controller used to drive a wide range of display devices varying in size and capability. The LCDIF is designed to support dumb (synchronous 24-bit Parallel RGB interface) and smart (asynchronous parallel MPU interface) LCD devices.
MQS	Medium Quality Sound	Multimedia Peripherals	MQS is used to generate 2-channel medium quality PWM-like audio via two standard digital GPIO pins.
PWM1 PWM2 PWM3 PWM4 PWM5 PWM6 PWM7 PWM8	Pulse Width Modulation	Connectivity peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
PXP	Pixel Processing Pipeline	Display peripherals	A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma-mapping, and rotation. The PXP is enhanced with features specifically for gray scale applications. In addition, the PXP supports traditional pixel/frame processing paths for still-image and video processing applications, allowing it to interface with the integrated EPD.

Table 11. Operating Ranges (continued)

DDR I/O supply	NVCC_DRAM	LPDDR2	1.14	1.2	1.3	V	—
		DDR3L	1.28	1.35	1.45	V	—
		DDR3	1.43	1.5	1.575	V	—
	NVCC_DRAM2P5	—	2.25	2.5	2.75	V	—
GPIO supplies	NVCC_CSI	—	1.65	1.8, 2.8, 3.3	3.6	V	All digital I/O supplies (NVCC_xxxx) must be powered (unless otherwise specified in this data sheet) under normal conditions whether the associated I/O pins are in use or not.
	NVCC_ENET						
	NVCC_GPIO						
	NVCC_UART						
	NVCC_LCD						
	NVCC_NAND						
	NVCC_SD1						
A/D converter	VDDA_ADC_3P3	—	3.0	3.15	3.6	V	VDDA_ADC_3P3 must be powered when chip is in RUN mode, IDLE mode, or SUSPEND mode. VDDA_ADC_3P3 should not be powered when chip is in SNVS mode.
Temperature Operating Ranges							
Junction temperature	Tj	Standard Commercial	0	—	95	°C	See the application note, i.MX 6UltraLite Product Lifetime Usage Estimates for information on product lifetime (power-on years) for this processor.

1 Applying the maximum voltage results in maximum power consumption and heat generation. NXP recommends a voltage set point = (V_{min} + the supply tolerance). This result in an optimized power/speed ratio.

2 In setting VDD_HIGH_IN voltage, refer to the Errata ERR010690 (SNVS_LP Registers Reset Issue).

3 In setting VDD_SNVS_IN voltage with regards to Charging Currents and RTC, refer to the *i.MX 6UltraLite Hardware Development Guide* (IMX6ULHDG).

Table 12 shows on-chip LDO regulators that can supply on-chip loads.

Table 12. On-Chip LDOs[1] and their On-Chip Loads

Voltage Source	Load	Comment
VDD_HIGH_CAP	NVCC_DRAM_2P5	Board-level connection to VDD_HIGH_CAP

1 On-chip LDOs are designed to supply i.MX6UltraLite loads and must not be used to supply external loads.

4.1.4 External clock sources

Each i.MX 6UltraLite processor has two external input system clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI).

NOTE

The POR_B input (if used) must be immediately asserted at power-up and remain asserted until after the last power rail reaches its working voltage. In the absence of an external reset feeding the POR_B input, the internal POR module takes control. See the *i.MX 6UltraLite Reference Manual* (IMX6ULRM) for further details and to ensure that all necessary requirements are being met.

NOTE

Need to ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

NOTE

USB_OTG1_VBUS and USB_OTG2_VBUS are not part of the power supply sequence and may be powered at any time.

4.2.2 Power-down sequence

The following restrictions must be followed:

- VDD_SNVS_IN supply must be turned off after any other power supply or be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is removed after any other supply is switched off.

CAUTION

For power sequence control on VDD_HIGH_IN and VDD_SOC_IN, refer to the ERR010690 (SNVS_LP Registers Reset Issue).

4.2.3 Power supplies usage

All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_xxx) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Rail” columns in pin list tables of Section 6, “Package information and contact assignments".”

4.3 Integrated LDO voltage regulator parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the *i.MX 6UltraLite Reference Manual* (IMX6ULRM) for details on the power tree scheme.

NOTE

The *_CAP signals should not be powered externally. These signals are intended for internal LDO operation only.

Table 25. LPDDR2 I/O DC Electrical Parameters[1] (continued)

Parameters	Symbol	Test Conditions	Min	Max	Unit
DC High-Level input voltage	Vih_DC	—	Vref+0.13	OVDD	V
DC Low-Level input voltage	Vil_DC	—	OVSS	Vref-0.13	V
Differential Input Logic High	Vih_diff	—	0.26	Note[2]	—
Differential Input Logic Low	Vil_diff	—	Note[2]	-0.26	—
Pull-up/Pull-down Impedance Mismatch	Mmpupd	—	-15	15	%
240 Ω unit calibration resolution	Rres	—	—	10	Ω
Keeper Circuit Resistance	Rkeep	—	110	175	kΩ
Input current (no pull-up/down)	Iin	VI = 0, VI = OVDD	-2.5	2.5	μA

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

4.6.3.2 DDR3/DDR3L mode I/O DC parameters

The parameters in Table 27 are guaranteed per the operating ranges in Table 11, unless otherwise noted.

Table 27. DDR3/DDR3L I/O DC Electrical Characteristics

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	VOH	Ioh= -0.1mA Voh (for ipp_dse=001)	0.8*OVDD[1]	—	V
Low-level output voltage	VOL	Iol= 0.1mA Vol (for ipp_dse=001)	0.2*OVDD	—	V
High-level output voltage	VOH	Ioh= -1mA Voh (for all except ipp_dse=001)	0.8*OVDD	—	V
Low-level output voltage	VOL	Iol= 1mA Vol (for all except ipp_dse=001)	0.2*OVDD	—	V
Input Reference Voltage	Vref	—	0.49*ovdd	0.51*ovdd	V
DC High-Level input voltage	Vih_DC	—	Vref[2]+0.1	OVDD	V
DC Low-Level input voltage	Vil_DC	—	OVSS	Vref-0.1	V
Differential Input Logic High	Vih_diff	—	0.2	—	V
Differential Input Logic Low	Vil_diff	—	—	-0.2	V
Termination Voltage	Vtt	Vtt tracking OVDD/2	0.49*OVDD	0.51*OVDD	V
Pull-up/Pull-down Impedance Mismatch	Mmpupd	—	-10	10	%
240 Ω unit calibration resolution	Rres	—	—	10	Ω
Keeper Circuit Resistance	Rkeep	—	105	165	kΩ
Input current (no pull-up/down)	Iin	VI = 0,VI = OVDD	-2.9	2.9	μA

1 OVDD – I/O power supply (1.425 V–1.575 V for DDR3 and 1.283 V–1.45 V for DDR3L)

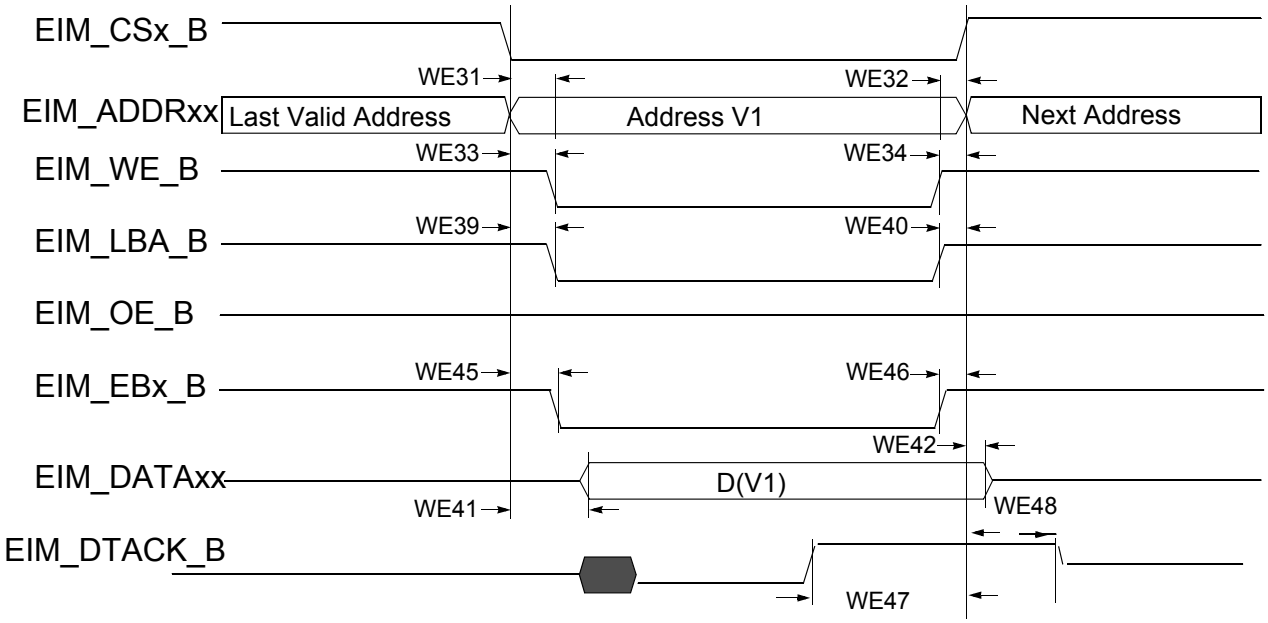

Figure 20. DTACK Mode Write Access (DAP=0)

Table 40. EIM Asynchronous Timing Parameters Table Relative Chip to Select[1,2]

Ref No.	Parameter	Determination by Synchronous measured parameters	Min	Max	Unit
WE31	EIM_CSx_B valid to Address Valid	WE4 - WE6 - CSA x t	-3.5 - CSA x t	3.5 - CSA x t	ns
WE32	Address Invalid to EIM_CSx_B Invalid	WE7 - WE5 - CSN x t	-3.5 - CSN x t	3.5 - CSN x t	ns
WE32A(muxed A/D	EIM_CSx_B valid to Address Invalid	t + WE4 - WE7 + (ADVN + ADVA + 1 - CSA) x t	t - 3.5 + (ADVN + ADVA + 1 - CSA) x t	t + 3.5 + (ADVN + ADVA + 1 - CSA) x t	ns
WE33	EIM_CSx_B Valid to EIM_WE_B Valid	WE8 - WE6 + (WEA - WCSA) x t	-3.5 + (WEA - WCSA) x t	3.5 + (WEA - WCSA) x t	ns
WE34	EIM_WE_B Invalid to EIM_CSx_B Invalid	WE7 - WE9 + (WEN - WCSN) x t	-3.5 + (WEN - WCSN) x t	3.5 + (WEN - WCSN) x t	ns
WE35	EIM_CSx_B Valid to EIM_OE_B Valid	WE10 - WE6 + (OEA - RCSA) x t	-3.5 + (OEA - RCSA) x t	3.5 + (OEA - RCSA) x t	ns
WE35A (muxed A/D)	EIM_CSx_B Valid to EIM_OE_B Valid	WE10 - WE6 + (OEA + RADVN + RADVA + ADH + 1 - RCSA) x t	-3.5 + (OEA + RADVN + RADVA + ADH + 1 - RCSA) x t	3.5 + (OEA + RADVN + RADVA + ADH + 1 - RCSA) x t	ns
WE36	EIM_OE_B Invalid to EIM_CSx_B Invalid	WE7 - WE11 + (OEN - RCSN) x t	-3.5 + (OEN - RCSN) x t	3.5 + (OEN - RCSN) x t	ns

Table 40. EIM Asynchronous Timing Parameters Table Relative Chip to Select[1,2]

Ref No.	Parameter	Determination by Synchronous measured parameters	Min	Max	Unit
WE37	EIM_CSx_B Valid to EIM_EBx_B Valid (Read access)	WE12 - WE6 + (RBEA - RCSA) x t	-3.5 + (RBEA - RCSA) x t	3.5 + (RBEA - RCSA) x t	ns
WE38	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Read access)	WE7 - WE13 + (RBEN - RCSN) x t	-3.5 + (RBEN - RCSN) x t	3.5 + (RBEN- RCSN) x t	ns
WE39	EIM_CSx_B Valid to EIM_LBA_B Valid	WE14 - WE6 + (ADVA - CSA) x t	-3.5 + (ADVA - CSA) x t	3.5 + (ADVA - CSA) x t	ns
WE40	EIM_LBA_B Invalid to EIM_CSx_B Invalid (ADVL is asserted)	WE7 - WE15 - CSN x t	-3.5 - CSN x t	3.5 - CSN x t	ns
WE40A (muxed A/D)	EIM_CSx_B Valid to EIM_LBA_B Invalid	WE14 - WE6 + (ADVN + ADVA + 1 - CSA) x t	-3.5 + (ADVN + ADVA + 1 - CSA) x t	3.5 + (ADVN + ADVA + 1 - CSA) x t	ns
WE41	EIM_CSx_B Valid to Output Data Valid	WE16 - WE6 - WCSA x t	-3.5 - WCSA x t	3.5 - WCSA x t	ns
WE41A (muxed A/D)	EIM_CSx_B Valid to Output Data Valid	WE16 - WE6 + (WADVN + WADVA + ADH + 1 - WCSA) x t	-3.5 + (WADVN + WADVA + ADH + 1 - WCSA) x t	3.5 + (WADVN + WADVA + ADH + 1 - WCSA) x t	ns
WE42	Output Data Invalid to EIM_CSx_B Invalid	WE17 - WE7 - CSN x t	-3.5 - CSN x t	3.5 - CSN x t	ns
MAXCO	Output maximum delay from internal driving EIM_ADDRxx/control flip-flops to chip outputs	10	—	10	ns
MAXCSO	Output maximum delay from internal chip selects driving flip-flops to EIM_CSx_B out	10	—	10	ns
MAXDI	EIM_DATAxx maximum delay from chip input data to its internal flip-flop	5	—	5	ns
WE43	Input Data Valid to EIM_CSx_B Invalid	MAXCO - MAXCSO + MAXDI	MAXCO - MAXCSO + MAXDI	—	ns
WE44	EIM_CSx_B Invalid to Input Data Invalid	0	0	—	ns

Table 40. EIM Asynchronous Timing Parameters Table Relative Chip to Select[1,2]

Ref No.	Parameter	Determination by Synchronous measured parameters	Min	Max	Unit
WE45	EIM_CSx_B Valid to EIM_EBx_B Valid (Write access)	WE12 - WE6 + (WBEA - WCSA) x t	-3.5 + (WBEA - WCSA) x t	3.5 + (WBEA - WCSA) x t	ns
WE46	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Write access)	WE7 - WE13 + (WBEN - WCSN) x t	-3.5 + (WBEN - WCSN) x t	3.5 + (WBEN - WCSN) x t	ns
MAXDTI	MAXIMUM delay from EIM_DTACK_B to its internal flip-flop + 2 cycles for synchronization	10	—	10	—
WE47	EIM_DTACK_B Active to EIM_CSx_B Invalid	MAXCO - MAXCSO + MAXDTI	MAXCO - MAXCSO + MAXDTI	—	ns
WE48	EIM_CSx_B Invalid to EIM_DTACK_B Invalid	0	0	—	ns

1 For more information on configuration parameters mentioned in this table, see the *i.MX 6UltraLite Reference Manual* (IMX6ULRM).

2 In this table, CSA means WCSA when write operation or RCSA when read operation

— t means clock period from axi_clk frequency.

—CSA means register setting for WCSA when in write operations or RCSA when in read operations.

—CSN means register setting for WCSN when in write operations or RCSN when in read operations.

—ADVN means register setting for WADVN when in write operations or RADVN when in read operations.

—ADVA means register setting for WADVA when in write operations or RADVA when in read operations.

4.10 Multi-Mode DDR Controller (MMDC)

The Multi-Mode DDR Controller is a dedicated interface to DDR3/DDR3L/LPDDR2 SDRAM.

4.10.1 MMDC compatibility with JEDEC-compliant SDRAMs

The i.MX 6UltraLite MMDC supports the following memory types:

- LPDDR2 SDRAM compliant with JESD209-2B LPDDR2 JEDEC standard release June, 2009
- DDR3/DDR3L SDRAM compliant with JESD79-3D DDR3 JEDEC standard release April, 2008

MMDC operation with the standards stated above is contingent upon the board DDR design adherence to the DDR design and layout requirements stated in the *Hardware Development Guide for the i.MX 6UltraLite Applications Processor (IMX6ULHDG)*.

4.10.2 MMDC supported DDR3/DDR3L/LPDDR2 configurations

Table 41 shows the MMDC supported DDR3/DDR3L/LPDDR2 configurations.

Table 41. i.MX 6UltraLite Supported DDR3/DDR3L/LPDDR2 Configurations

Parameter	DDR3	DDR3L	LDDDR2
Clock frequency	400 MHz	400 MHz	400 MHz
Bus width	16-bit	16-bit	16-bit
Channel	Single	Single	Single
Chip selects	2	2	2

4.11 General-Purpose Media Interface (GPMI) timing

The i.MX 6UltraLite GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select.

It supports Asynchronous timing mode, Source Synchronous timing mode and Samsung Toggle timing mode separately described in the following subsections.

4.11.1 Asynchronous mode AC timing (ONFI 1.0 compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The maximum I/O speed of GPMI in asynchronous mode is about 50 MB/s. Figure 21 through Figure 24 depicts the relative timing between GPMI signals at the module level for different operations under asynchronous mode. Table 42 describes the timing parameters (NF1–NF17) that are shown in the figures.

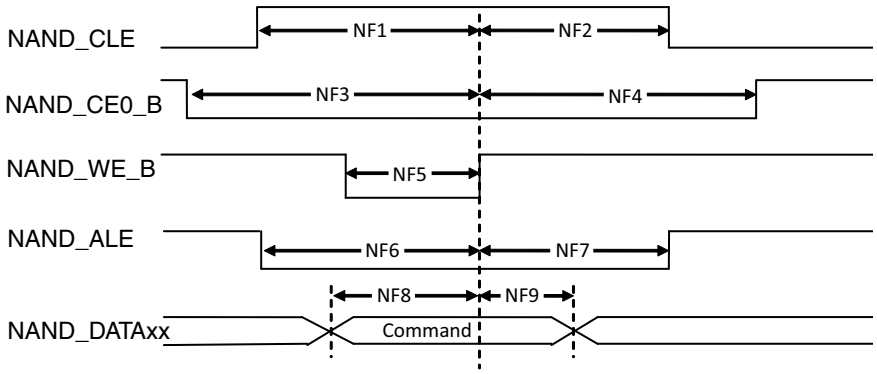

Figure 21. Command Latch Cycle Timing Diagram

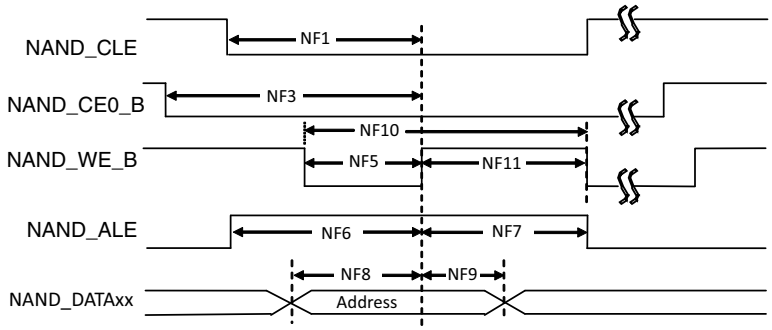

Figure 22. Address Latch Cycle Timing Diagram

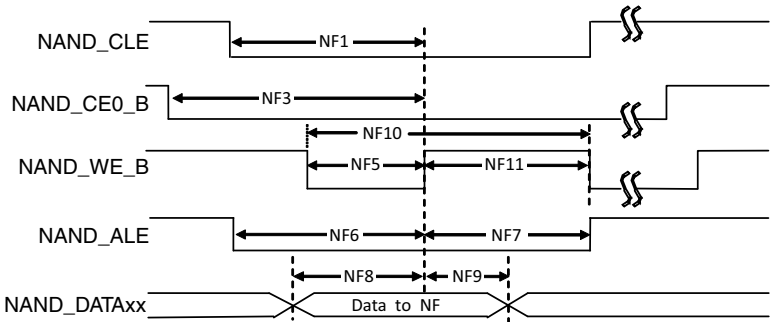

Figure 23. Write Data Latch Cycle Timing Diagram

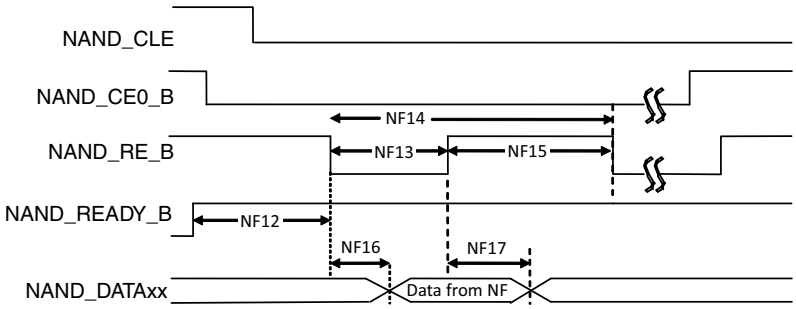

Figure 24. Read Data Latch Cycle Timing Diagram (Non-EDO Mode)

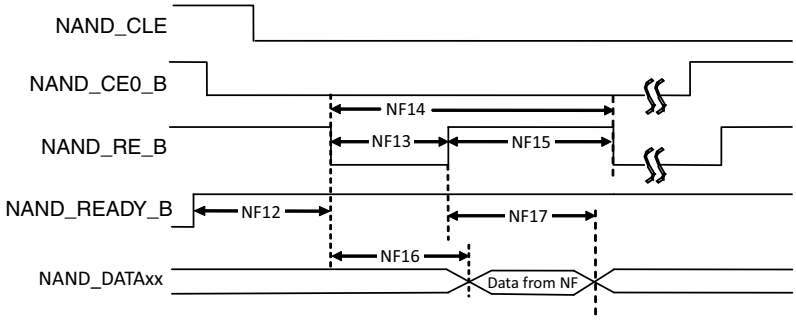

Figure 25. Read Data Latch Cycle Timing Diagram (EDO Mode)

4.11.2 Source synchronous mode AC timing (ONFI 2.x compatible)

Figure 26 to Figure 28 show the write and read timing of Source Synchronous Mode.

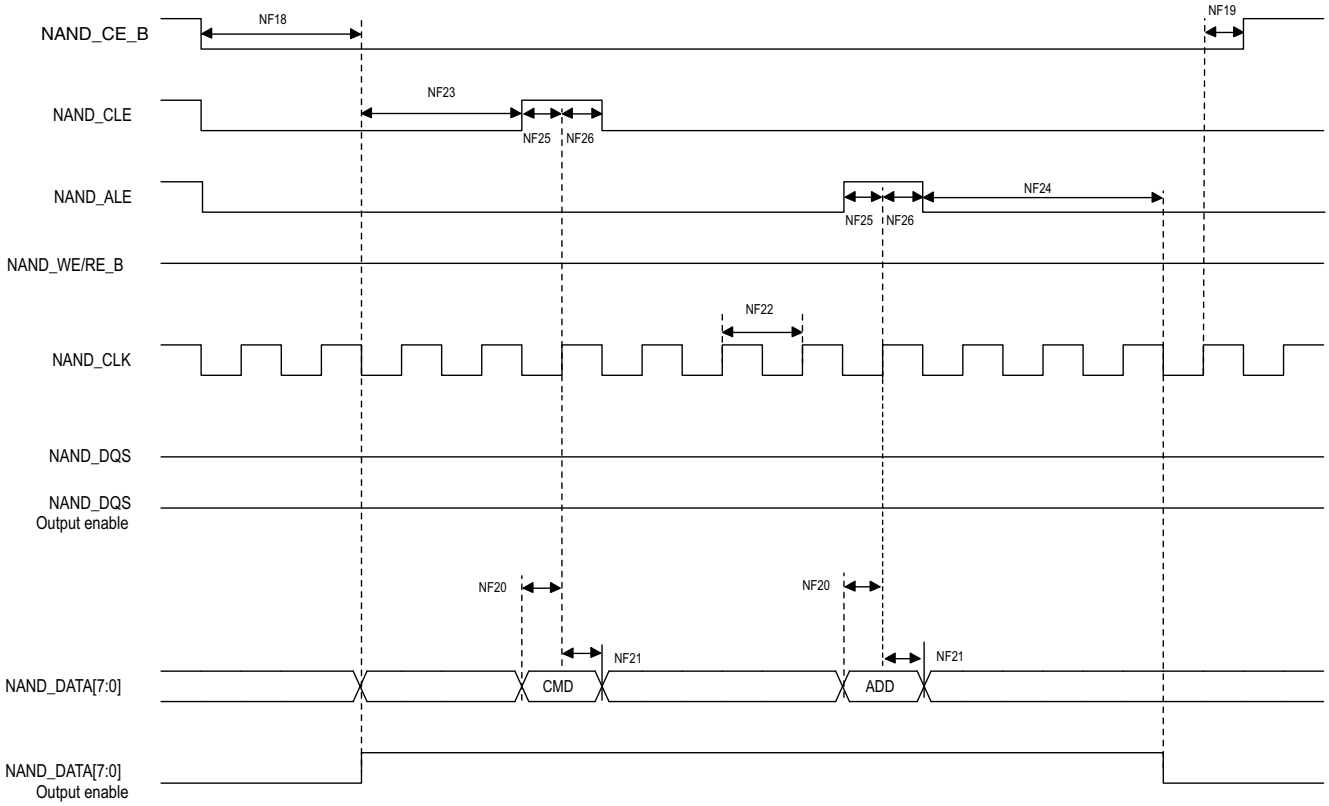

Figure 26. Source Synchronous Mode Command and Address Timing Diagram

4.12.3 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing, eMMC4.4/4.41/4.5 (Dual Date Rate) timing and SDR104/50(SD3.0) timing.

4.12.3.1 SD/eMMC4.3 (single data rate) AC timing

Figure 37 depicts the timing of SD/eMMC4.3, and Table 49 lists the SD/eMMC4.3 timing characteristics.

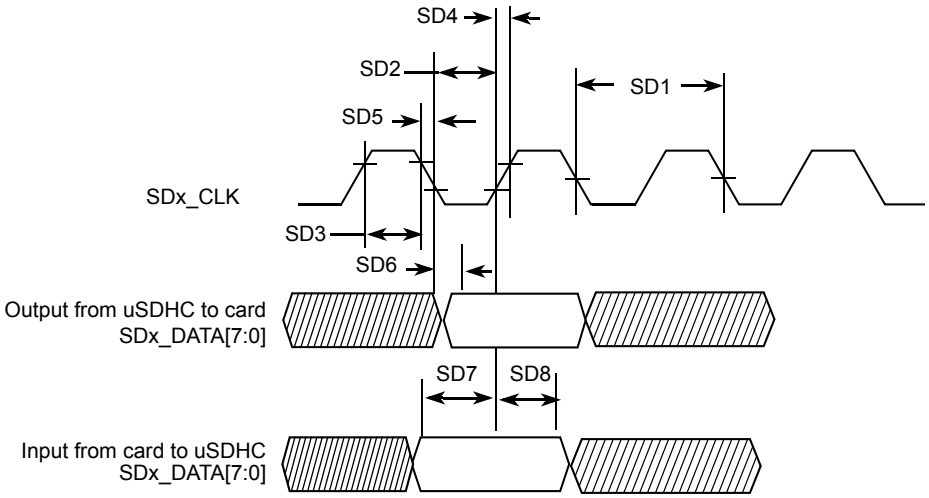

Figure 37. SD/eMMC4.3 Timing

Table 49. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD6	uSDHC Output Delay	t_{OD}	-6.6	3.6	ns

4.12.6 I²C module timing parameters

This section describes the timing parameters of the I²C module. Figure 46 depicts the timing of I²C module, and Table 58 lists the I²C module timing characteristics.

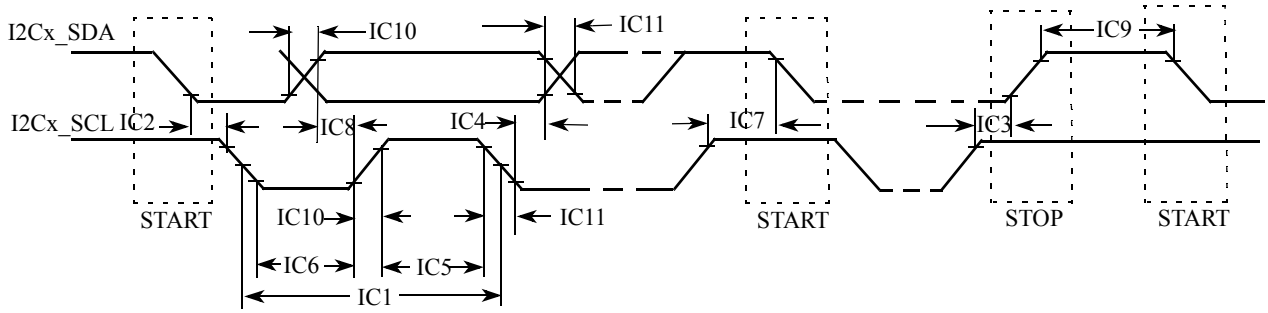

Figure 46. I²C Bus Timing

Table 58. I²C Module Timing Parameters

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC1	I2Cx_SCL cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2Cx_SCL Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2Cx_SCL Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2Cx_SDA and I2Cx_SCL signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11	Fall time of both I2Cx_SDA and I2Cx_SCL signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2Cx_SDA signal to bridge the undefined region of the falling edge of I2Cx_SCL.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2Cx_SCL signal.

3 A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2Cx_SCL signal. If such a device does stretch the LOW period of the I2Cx_SCL signal, it must output the next data bit to the I2Cx_SDA line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the I2Cx_SCL line is released.

4 C_b = total capacitance of one bus line in pF.

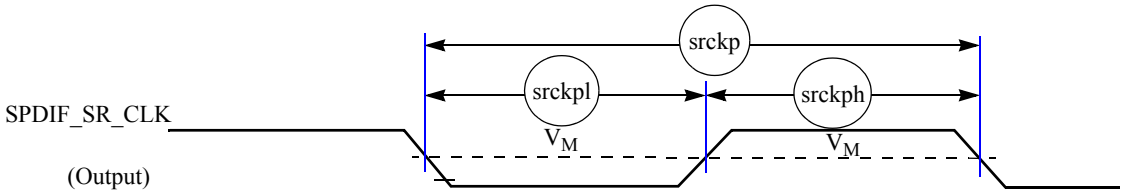

Figure 61. SPDIF_SR_CLK Timing Diagram

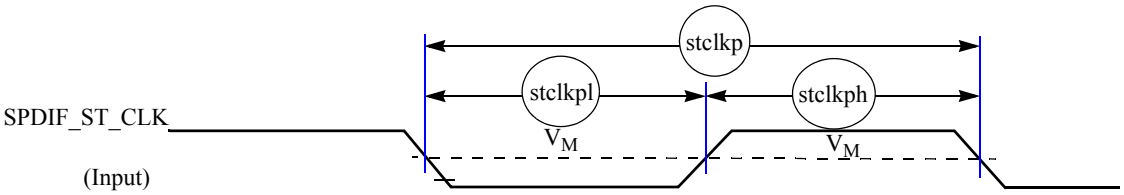

Figure 62. SPDIF_ST_CLK Timing Diagram

4.12.13 UART I/O configuration and timing parameters

4.12.13.1 UART RS-232 serial mode timing

The following sections describe the electrical information of the UART module in the RS-232 mode.

4.12.13.1.1 UART transmitter

Figure 63 depicts the transmit timing of UART in the RS-232 serial mode, with 8 data bit/1 stop bit format. Table 72 lists the UART RS-232 serial mode transmits timing characteristics.

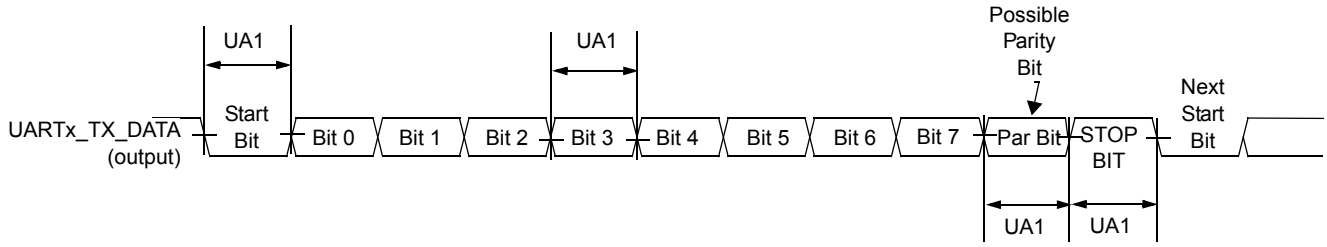

Figure 63. UART RS-232 Serial Mode Transmit Timing Diagram

Table 72. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$ [1] - T_{ref_clk} [2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

Table 77. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}) (continued)

Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	Comment
Conversion Time	ADLSMP=0 ADSTS=00	Tconv	—	0.7	—	µs	Fadc=40 MHz
	ADLSMP=0 ADSTS=01			0.75			
	ADLSMP=0 ADSTS=10			0.8			
	ADLSMP=0 ADSTS=11			0.85			
	ADLSMP=1 ADSTS=00			0.95			
	ADLSMP=1 ADSTS=01			1.05			
	ADLSMP=1 ADSTS=10			1.15			
	ADLSMP=1, ADSTS=11			1.25			
[P:][C:] Total Unadjusted Error	12 bit mode	TUE	—	4.5	—	LSB 1 LSB = $(V_{REFH} - V_{REFL})/2^N$	—
	10 bit mode		—	2	—		
	8 bit mode		—	1.5	—		
[P:][C:] Differential Non-Linearity	12 bit mode	DNL	—	1	—	LSB	—
	10bit mode		—	0.5	—		
	8 bit mode		—	0.2	—		
[P:][C:] Integral Non-Linearity	12 bit mode	INL	—	2.6	—	LSB	—
	10bit mode		—	0.8	—		
	8 bit mode		—	0.3	—		
Zero-Scale Error	12 bit mode	E_{ZS}	—	-0.3	—	LSB	—
	10bit mode		—	-0.15	—		
	8 bit mode		—	-0.15	—		
Full-Scale Error	12 bit mode	E_{FS}	—	-2.5	—	LSB	—
	10bit mode		—	-0.6	—		
	8 bit mode		—	-0.3	—		
[L:] Effective Number of Bits	12 bit mode	ENOB	10.1	10.7	—	Bits	—
[L:] Signal to Noise plus Distortion	See ENOB	SINAD	SINAD = 6.02 x ENOB + 1.76			dB	—

[1] All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDAD}

Table 91. 14x14 mm Functional Contact Assignments (continued)

LCD_ENABLE	B8	NVCC_LCD	GPIO	ALT5	LCD_ENABLE	Input	Keeper
LCD_HSYNC	D9	NVCC_LCD	GPIO	ALT5	LCD_HSYNC	Input	Keeper
LCD_RESET	E9	NVCC_LCD	GPIO	ALT5	LCD_RESET	Input	Keeper
LCD_VSYNC	C9	NVCC_LCD	GPIO	ALT5	LCD_VSYNC	Input	Keeper
NAND_ALE	B4	NVCC_NAND	GPIO	ALT5	VDDSOC	Input	Keeper
NAND_CE0_B	C5	NVCC_NAND	GPIO	ALT5	NAND_CE0_B	Input	Keeper
NAND_CE1_B	B5	NVCC_NAND	GPIO	ALT5	NAND_CE1_B	Input	Keeper
NAND_CLE	A4	NVCC_NAND	GPIO	ALT5	NAND_CLE	Input	Keeper
NAND_DATA00	D7	NVCC_NAND	GPIO	ALT5	NAND_DATA00	Input	Keeper
NAND_DATA01	B7	NVCC_NAND	GPIO	ALT5	NAND_DATA01	Input	Keeper
NAND_DATA02	A7	NVCC_NAND	GPIO	ALT5	NAND_DATA02	Input	Keeper
NAND_DATA03	D6	NVCC_NAND	GPIO	ALT5	NAND_DATA03	Input	Keeper
NAND_DATA04	C6	NVCC_NAND	GPIO	ALT5	NAND_DATA04	Input	Keeper
NAND_DATA05	B6	NVCC_NAND	GPIO	ALT5	NAND_DATA05	Input	Keeper
NAND_DATA06	A6	NVCC_NAND	GPIO	ALT5	NAND_DATA06	Input	Keeper
NAND_DATA07	A5	NVCC_NAND	GPIO	ALT5	NAND_DATA07	Input	Keeper
NAND_DQS	E6	NVCC_NAND	GPIO	ALT5	NAND_DQS	Input	Keeper
NAND_RE_B	D8	NVCC_NAND	GPIO	ALT5	NAND_RE_B	Input	Keeper
NAND_READY_B	A3	NVCC_NAND	GPIO	ALT5	NAND_READY_B	Input	Keeper
NAND_WE_B	C8	NVCC_NAND	GPIO	ALT5	NAND_WE_B	Input	Keeper
NAND_WP_B	D5	NVCC_NAND	GPIO	ALT5	NAND_WP_B	Input	Keeper
ONOFF	R8	VDD_SNVS_IN	GPIO	ALT0	ONOFF	Input	100 kΩ pull-up
POR_B	P8	VDD_SNVS_IN	GPIO	ALT0	POR_B	Input	100 kΩ pull-up
RTC_XTALI	T11	VDD_SNVS_CAP	ANALOG	—	RTC_XTALI	—	—
RTC_XTALO	U11	VDD_SNVS_CAP	ANALOG	—	RTC_XTALO	—	—
SD1_CLK	C1	NVCC_SD1	GPIO	ALT5	SD1_CLK	Input	Keeper
SD1_CMD	C2	NVCC_SD1	GPIO	ALT5	SD1_CMD	Input	Keeper
SD1_DATA0	B3	NVCC_SD1	GPIO	ALT5	SD1_DATA0	Input	Keeper
SD1_DATA1	B2	NVCC_SD1	GPIO	ALT5	SD1_DATA1	Input	Keeper
SD1_DATA2	B1	NVCC_SD1	GPIO	ALT5	SD1_DATA2	Input	Keeper
SD1_DATA3	A2	NVCC_SD1	GPIO	ALT5	SD1_DATA3	Input	Keeper
SNVS_PMIC_ON_REQ	T9	VDD_SNVS_IN	GPIO	ALT0	SNVS_PMIC_ON_REQ	Output	100 kΩ pull-up

Table 94. 9x9 mm Functional Contact Assignments (continued)

DRAM_ADDR07	J4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR07	Output	100 kΩ pull-up
DRAM_ADDR08	J5	NVCC_DRAM	DDR	ALT0	DRAM_ADDR08	Output	100 kΩ pull-up
DRAM_ADDR09	J1	NVCC_DRAM	DDR	ALT0	DRAM_ADDR09	Output	100 kΩ pull-up
DRAM_ADDR10	M2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR10	Output	100 kΩ pull-up
DRAM_ADDR11	K5	NVCC_DRAM	DDR	ALT0	DRAM_ADDR11	Output	100 kΩ pull-up
DRAM_ADDR12	L3	NVCC_DRAM	DDR	ALT0	DRAM_ADDR12	Output	100 kΩ pull-up
DRAM_ADDR13	H4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR13	Output	100 kΩ pull-up
DRAM_ADDR14	E3	NVCC_DRAM	DDR	ALT0	DRAM_ADDR14	Output	100 kΩ pull-up
DRAM_ADDR15	E2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR15	Output	100 kΩ pull-up
DRAM_CAS_B	G4	NVCC_DRAM	DDR	ALT0	DRAM_CAS_B	Output	100 kΩ pull-up
DRAM_CS0_B	L1	NVCC_DRAM	DDR	ALT0	DRAM_CS0_B	Output	100 kΩ pull-up
DRAM_CS1_B	H5	NVCC_DRAM	DDR	ALT0	DRAM_CS1_B	Output	100 kΩ pull-up
DRAM_DATA00	T3	NVCC_DRAM	DDR	ALT0	DRAM_DATA00	Input	100 kΩ pull-up
DRAM_DATA01	N5	NVCC_DRAM	DDR	ALT0	DRAM_DATA01	Input	100 kΩ pull-up
DRAM_DATA02	T4	NVCC_DRAM	DDR	ALT0	DRAM_DATA02	Input	100 kΩ pull-up
DRAM_DATA03	T5	NVCC_DRAM	DDR	ALT0	DRAM_DATA03	Input	100 kΩ pull-up
DRAM_DATA04	U5	NVCC_DRAM	DDR	ALT0	DRAM_DATA04	Input	100 kΩ pull-up
DRAM_DATA05	T6	NVCC_DRAM	DDR	ALT0	DRAM_DATA05	Input	100 kΩ pull-up
DRAM_DATA06	R4	NVCC_DRAM	DDR	ALT0	DRAM_DATA06	Input	100 kΩ pull-up
DRAM_DATA07	U3	NVCC_DRAM	DDR	ALT0	DRAM_DATA07	Input	100 kΩ pull-up
DRAM_DATA08	P1	NVCC_DRAM	DDR	ALT0	DRAM_DATA08	Input	100 kΩ pull-up

Table 96. GPIO Behaviors during Reset (continued)[1]

Ball Name	Mux Mode	Function	Input/Output	Value
LCD_DATA10	ALT6	SRC_BT_CFG[10]	Input	100 kΩ pull-down
LCD_DATA11	ALT6	SRC_BT_CFG[11]	Input	100 kΩ pull-down
LCD_DATA12	ALT6	SRC_BT_CFG[12]	Input	100 kΩ pull-down
LCD_DATA13	ALT6	SRC_BT_CFG[13]	Input	100 kΩ pull-down
LCD_DATA14	ALT6	SRC_BT_CFG[14]	Input	100 kΩ pull-down
LCD_DATA15	ALT6	SRC_BT_CFG[15]	Input	100 kΩ pull-down
LCD_DATA16	ALT6	SRC_BT_CFG[16]	Input	100 kΩ pull-down
LCD_DATA17	ALT6	SRC_BT_CFG[17]	Input	100 kΩ pull-down
LCD_DATA18	ALT6	SRC_BT_CFG[18]	Input	100 kΩ pull-down
LCD_DATA19	ALT6	SRC_BT_CFG[19]	Input	100 kΩ pull-down
LCD_DATA20	ALT6	SRC_BT_CFG[20]	Input	100 kΩ pull-down
LCD_DATA21	ALT6	SRC_BT_CFG[21]	Input	100 kΩ pull-down
LCD_DATA22	ALT6	SRC_BT_CFG[22]	Input	100 kΩ pull-down
LCD_DATA23	ALT6	SRC_BT_CFG[23]	Input	100 kΩ pull-down

[1] Others are same as value in the column “Out of Reset Condition” of Table 91 and Table 94