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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	AVR
Core Size	8-Bit
Speed	4MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	20
Program Memory Size	2KB (1K x 16)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	32-TQFP
Supplier Device Package	32-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at90ls2333-4ac

Description

The AT90S2333/4433 is a low-power CMOS 8-bit microcontroller based on the AVR RISC architecture. By executing powerful instructions in a single clock cycle, the AT90S2333/4433 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The AT90S2333/4433 provides the following features: 2K/4K bytes of In-System Programmable Flash, 128/256 bytes EEPROM, 128 bytes SRAM, 20 general purpose I/O lines, 32 general purpose working registers, two flexible timer/counters with compare modes, internal and external interrupts, a programmable serial UART, 6-channel, 10-bit ADC, programmable Watchdog Timer with internal oscillator, an SPI serial port and two software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, timer/counters, SPI port and interrupt system to continue functioning. The Power Down mode saves the register contents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset.

The device is manufactured using Atmel's high-density nonvolatile memory technology. The on-chip Flash program memory can be reprogrammed in-system through an SPI serial interface or by a conventional nonvolatile memory programmer. By combining a RISC 8-bit CPU with In-System Programmable Flash on a monolithic chip, the Atmel AT90S2333/4433 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The AT90S2333/4433 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

Table 1. Comparison Table

Device	Flash	EEPROM	SRAM	Voltage Range	Frequency
AT90S2333	2K	128B	128B	4.0V - 6.0V	0 - 8 MHz
AT90LS2333	2K	128B	128B	2.7V - 6.0V	0 - 4 MHz
AT90S4433	4K	256B	128B	4.0V - 6.0V	0 - 8 MHz
AT90LS4433	4K	256B	128B	2.7V - 6.0V	0 - 4 MHz

The I/O memory space contains 64 addresses for CPU peripheral functions as Control Registers, Timer/Counters, A/D-converters, and other I/O functions. The I/O Memory can be accessed directly, or as the Data Space locations following those of the register file, $20 - $5F.

The AVR uses a Harvard architecture concept - with separate memories and buses for program and data. The program memory is executed with a two stage pipeline. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This concept enables instructions to be executed in every clock cycle.

The program memory is In-System Programmable Flash memory.

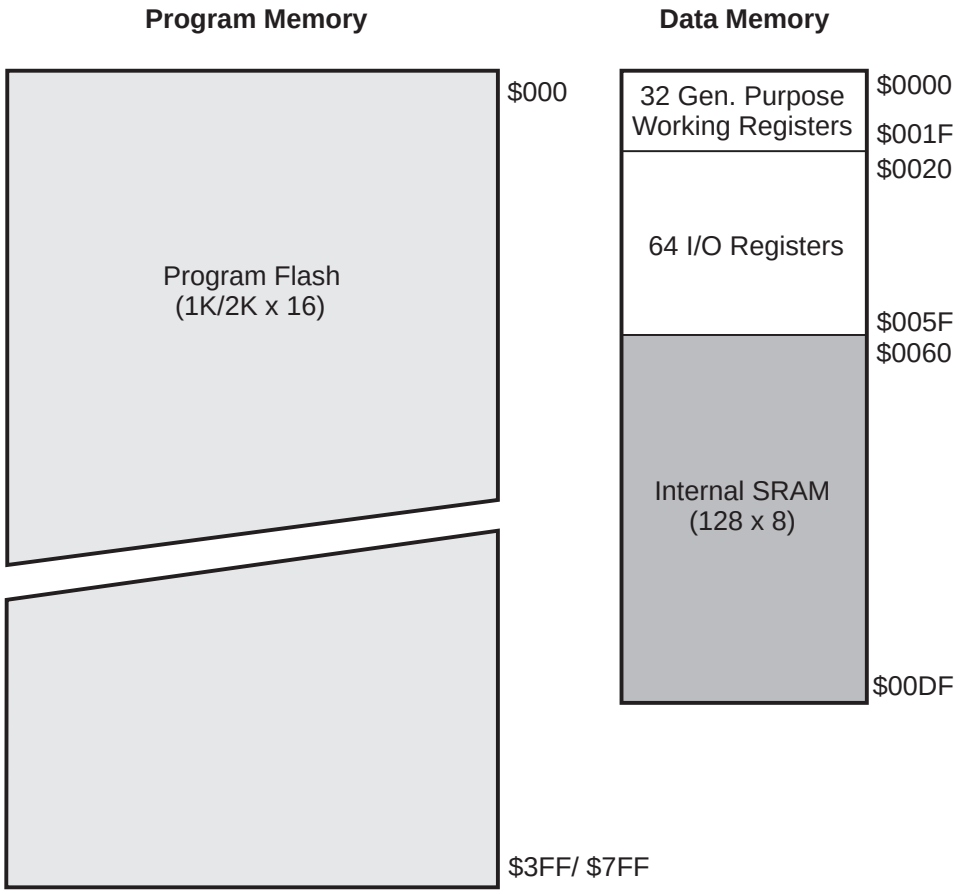
With the relative jump and call instructions, the whole 1K/2K word address space is directly accessed. Most AVR instructions have a single 16-bit word format. Every program memory address contains a 16- or 32-bit instruction.

During interrupts and subroutine calls, the return address program counter (PC) is stored on the stack. The stack is effectively allocated in the general data SRAM, and consequently the stack size is only limited by the total SRAM size and the usage of the SRAM. All user programs must initialize the SP in the reset routine (before subroutines or interrupts are executed). The 8-bit stack pointer SP is read/write accessible in the I/O space.

The 128 bytes data SRAM can be easily accessed through the five different addressing modes supported in the AVR architecture.

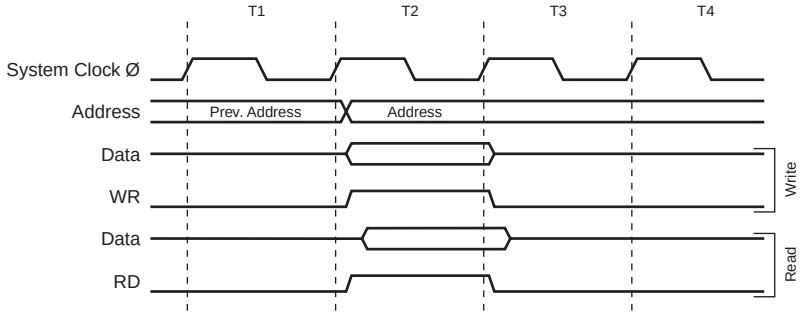
The memory spaces in the AVR architecture are all linear and regular memory maps.

Figure 6. AT90S2333/4433 Memory Maps



A flexible interrupt module has its control registers in the I/O space with an additional global interrupt enable bit in the status register. All the different interrupts have a separate interrupt vector in the interrupt vector table at the beginning of the program memory. The different interrupts have priority in accordance with their interrupt vector position. The lower the interrupt vector address, the higher the priority.

Figure 23. On-Chip Data SRAM Access Cycles



I/O Memory

The I/O space definition of the AT90S2333/4433 is shown in the following table:

Table 2. AT90S2333/4433 I/O Space

I/O Address (SRAM Address)	Name	Function
$3F ($5F)	SREG	Status REGister
$3D ($5D)	SP	Stack Pointer
$3B ($5B)	GIMSK	General Interrupt MaSK register
$3A ($5A)	GIFR	General Interrupt Flag Register
$39 ($59)	TIMSK	Timer/Counter Interrupt MaSK register
$38 ($58)	TIFR	Timer/Counter Interrupt Flag register
$35 ($55)	MCUCR	MCU general Control Register
$34 ($54)	MCUSR	MCU general Status Register
$33 ($53)	TCCR0	Timer/Counter0 Control Register
$32 ($52)	TCNT0	Timer/Counter0 (8-bit)
$2F ($4F)	TCCR1A	Timer/Counter1 Control Register A
$2E ($4E)	TCCR1B	Timer/Counter1 Control Register B
$2D ($4D)	TCNT1H	Timer/Counter1 High Byte
$2C ($4C)	TCNT1L	Timer/Counter1 Low Byte
$2B ($4B)	OCR1H	Timer/Counter1 Output Compare Register High Byte
$2A ($4A)	OCR1L	Timer/Counter1 Output Compare Register Low Byte
$27 ($47)	ICR1H	Timer/Counter1 Input Capture Register High Byte
$26 ($46)	ICR1L	Timer/Counter 1 Input Capture Register Low Byte
$21 ($41)	WDTCR	Watchdog Timer Control Register
$1E ($3E)	EEAR	EEPROM Address Register
$1D ($3D)	EEDR	EEPROM Data Register
$1C ($3C)	EECR	EEPROM Control Register
$18 ($38)	PORTB	Data Register, Port B
$17 ($37)	DDRB	Data Direction Register, Port B
$16 ($36)	PINB	Input Pins, Port B

```
$00e                MAIN:       ldi     r16,low(RAMEND); Main program start
$00f                            out     SP,r16;
$010                            <instr>  xxx       ;
  …                 …             …       …
```

Reset Sources

The AT90S2333/4433 has four sources of reset:

- Power-On Reset. The MCU is reset when the supply voltage is below the power-on reset threshold (V_{POT}).
- External Reset. The MCU is reset when a low level is present on the $\overline{\text{RESET}}$ pin for more than 50 ns.
- Watchdog Reset. The MCU is reset when the Watchdog timer period expires and the Watchdog is enabled.
- Brown-Out Reset. The MCU is reset when the supply voltage V_{CC} falls below a certain voltage.

During reset, all I/O registers are then set to their initial values, and the program starts execution from address $000. The instruction placed in address $000 must be an RJMP - relative jump - instruction to the reset handling routine. If the program never enables an interrupt source, the interrupt vectors are not used, and regular program code can be placed at these locations. The circuit diagram in Figure 24 shows the reset logic. Table 4 and Table 5 define the timing and electrical parameters of the reset circuitry.

Figure 24. Reset Logic

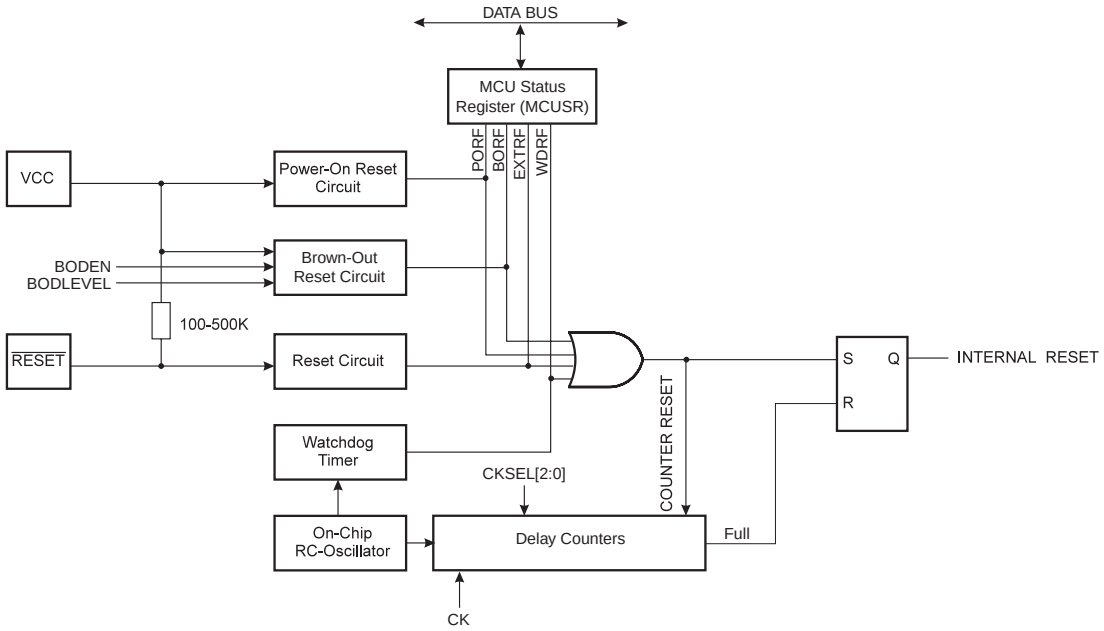
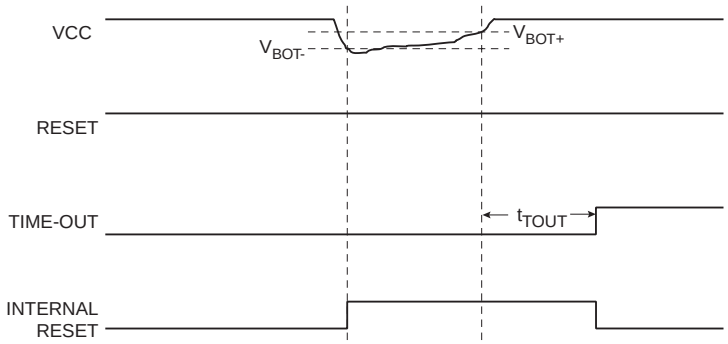


Table 4. Reset Characteristics (V_{CC} = 5.0V)

Symbol	Parameter	Min	Typ	Max	Units
V_{POT}	Power-On Reset Threshold Voltage, rising	1.0	1.4	1.8	V
	Power-On Reset Threshold Voltage, falling	0.4	0.6	0.8	V
V_{RST}	$\overline{\text{RESET}}$ Pin Threshold Voltage		$0.6V_{CC}$		V
V_{BOT}	Brown-Out Reset Threshold Voltage	2.6 (BODLEVEL = 1)	2.7 (BODLEVEL = 1)	2.8 (BODLEVEL = 1)	V
		3.8 (BODLEVEL = 0)	4.0 (BODLEVEL = 0)	4.2 (BODLEVEL = 0)	

Note: The Power-On Reset will not work unless the supply voltage has been below Vpot (falling).

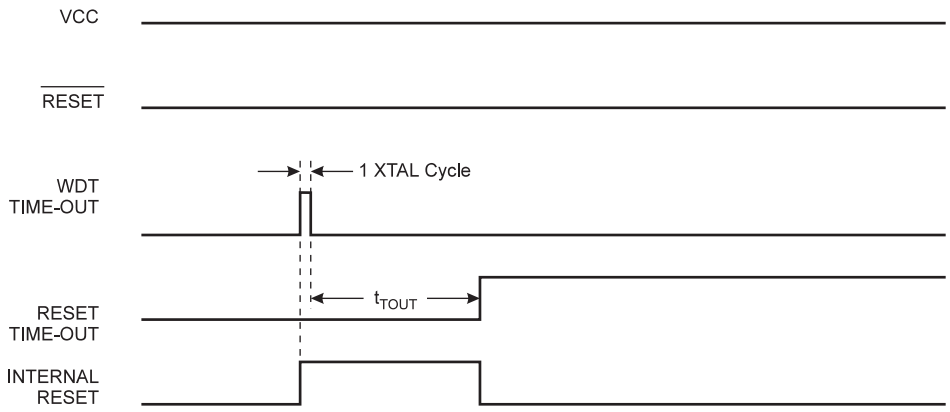
Figure 28. Brown-Out Reset During Operation



Watchdog Reset

When the Watchdog times out, it will generate a short reset pulse of 1 XTAL cycle duration. On the falling edge of this pulse, the delay timer starts counting the Time-out period t_{TOUT}. Refer to Page page 36 for details on operation of the Watchdog.

Figure 29. Watchdog Reset During Operation



MCU Status Register - MCUSR

The MCU Status Register provides information on which reset source caused an MCU reset.

Bit	7	6	5	4	3	2	1	0	
$34 ($54)	-	-	-	-	**WDRF**	**BORF**	**EXTRF**	**PORF**	**MCUSR**
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	See bit description				

- **Bits 7..4 - Res: Reserved Bits**

These bits are reserved bits in the AT90S2333 and always read as zero.

- **Bit 3 - WDRF: Watchdog Reset Flag**

This bit is set if a watchdog reset occurs. The bit is cleared by a power-on reset, or by writing a logic zero to the flag.

- **Bit 2 - BORF: Brown-Out Reset Flag**

This bit is set if a brown-out reset occurs. The bit is cleared by a power-on reset, or by writing a logic zero to the flag.

- **Bit 1 - EXTRF: External Reset Flag**

This bit is set if an external reset occurs. The bit is cleared by a power-on reset, or by writing a logic zero to the flag.

- **Bit 0 - PORF: Power-on Reset Flag**

This bit is set if a power-on reset occurs. The bit is cleared only by writing a logic zero to the flag.

To make use of the reset flags to identify a reset condition, the user should read and then clear the MCUSR as early as possible in the program. If the register is cleared before another reset occurs, the source of the reset can be found by examining the reset flags.

Interrupt Handling

The AT90S2333/4433 has two 8-bit Interrupt Mask control registers; GIMSK - General Interrupt Mask register and TIMSK - Timer/Counter Interrupt Mask register.

When an interrupt occurs, the Global Interrupt Enable I-bit is cleared (zero) and all interrupts are disabled. The user software can set (one) the I-bit to enable nested interrupts. The I-bit is set (one) when a Return from Interrupt instruction - RETI - is executed.

When the Program Counter is vectored to the actual interrupt vector in order to execute the interrupt handling routine, hardware clears the corresponding flag that generated the interrupt. Some of the interrupt flags can also be cleared by writing a logic one to the flag bit position(s) to be cleared.

If an interrupt condition occurs when the corresponding interrupt enable bit is cleared (zero), the interrupt flag will be set and remembered until the interrupt is enabled, or the flag is cleared by software.

If one or more interrupt conditions occur when the global interrupt enable bit is cleared (zero), the corresponding interrupt flag(s) will be set and remembered until the global interrupt enable bit is set (one), and will be executed by order of priority.

Note that external level interrupt does not have a flag, and will only be remembered for as long as the interrupt condition is active.

Note that the status register is not automatically stored when entering an interrupt routine and restored when returning from an interrupt routine. This must be handled by software.

General Interrupt Mask Register - GIMSK

Bit	7	6	5	4	3	2	1	0	
$3B ($5B)	**INT1**	**INT0**	**-**	**-**	**-**	**-**	**-**	**-**	**GIMSK**
Read/Write	R/W	R/W	R	R	R	R	R	R	
Initial value	0	0	0	0	0	0	0	0	

- **Bit 7 - INT1: External Interrupt Request 1 Enable**

When the INT1 bit is set (one) and the I-bit in the Status Register (SREG) is set (one), the external pin interrupt is enabled. The Interrupt Sense Control1 bits 1/0 (ISC11 and ISC10) in the MCU general Control Register (MCUCR) defines whether the external interrupt is activated on rising or falling edge of the INT1 pin or level sensed. Please note that INTF1 flag is not set when level sensitive interrupt condition is met. However, INT1 interrupt is generated, provided that INT1 mask bit is set in GIMSK register. Activity on the pin will cause an interrupt request even if INT1 is configured as an output. The corresponding interrupt of External Interrupt Request 1 is executed from program memory address $002. See also “External Interrupts”.

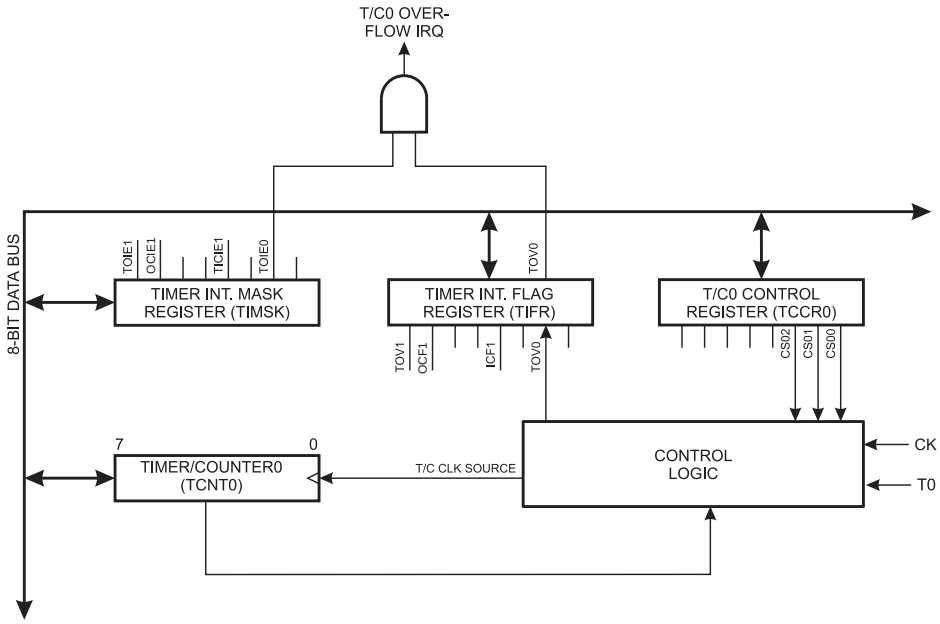
- **Bit 6 - INT0: External Interrupt Request 0 Enable**

When the INT0 bit is set (one) and the I-bit in the Status Register (SREG) is set (one), the external pin interrupt is enabled. The Interrupt Sense Control0 bits 1/0 (ISC01 and ISC00) in the MCU general Control Register (MCUCR) defines whether the external interrupt is activated on rising or falling edge of the INT0 pin or level sensed. Please note that INTF0 flag is not set when level sensitive interrupt condition is met. However, INT0 interrupt is generated, provided that INT0 mask bit is set in GIMSK register. Activity on the pin will cause an interrupt request even if INT0 is configured as an output. The corresponding interrupt of External Interrupt Request 0 is executed from program memory address $001. See also “External Interrupts.”

- **Bits 5..0 - Res: Reserved bits**

These bits are reserved bits in the AT90S2333/4433 and always read as zero.

Figure 31. Timer/Counter0 Block Diagram



Timer/Counter0 Control Register - TCCR0

Bit	7	6	5	4	3	2	1	0	
$33 ($53)	-	-	-	-	-	**CS02**	**CS01**	**CS00**	**TCCR0**
Read/Write	R	R	R	R	R	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

- **Bits 7-3 - Res: Reserved bits**

These bits are reserved bits in the AT90S2333/4433 and always read as zero.

- **Bits 2,1,0 - CS02, CS01, CS00: Clock Select0, bit 2,1 and 0**

The Clock Select0 bits 2,1, and 0 define the prescaling source of Timer0.

Table 9. Clock 0 Prescale Select

CS02	CS01	CS00	Description
0	0	0	Stop, Timer/Counter0 is stopped.
0	0	1	CK
0	1	0	CK / 8
0	1	1	CK / 64
1	0	0	CK / 256
1	0	1	CK / 1024
1	1	0	External Pin T0, falling edge
1	1	1	External Pin T0, rising edge

The Stop condition provides a Timer Enable/Disable function. The prescaled CK modes are scaled directly from the CK oscillator clock. If the external pin modes are used, for Timer/Counter0, transitions on PD4/(T0) will clock the counter even if the pin is configured as an output. This feature can give the user SW control of the counting.

Timer Counter 0 - TCNT0

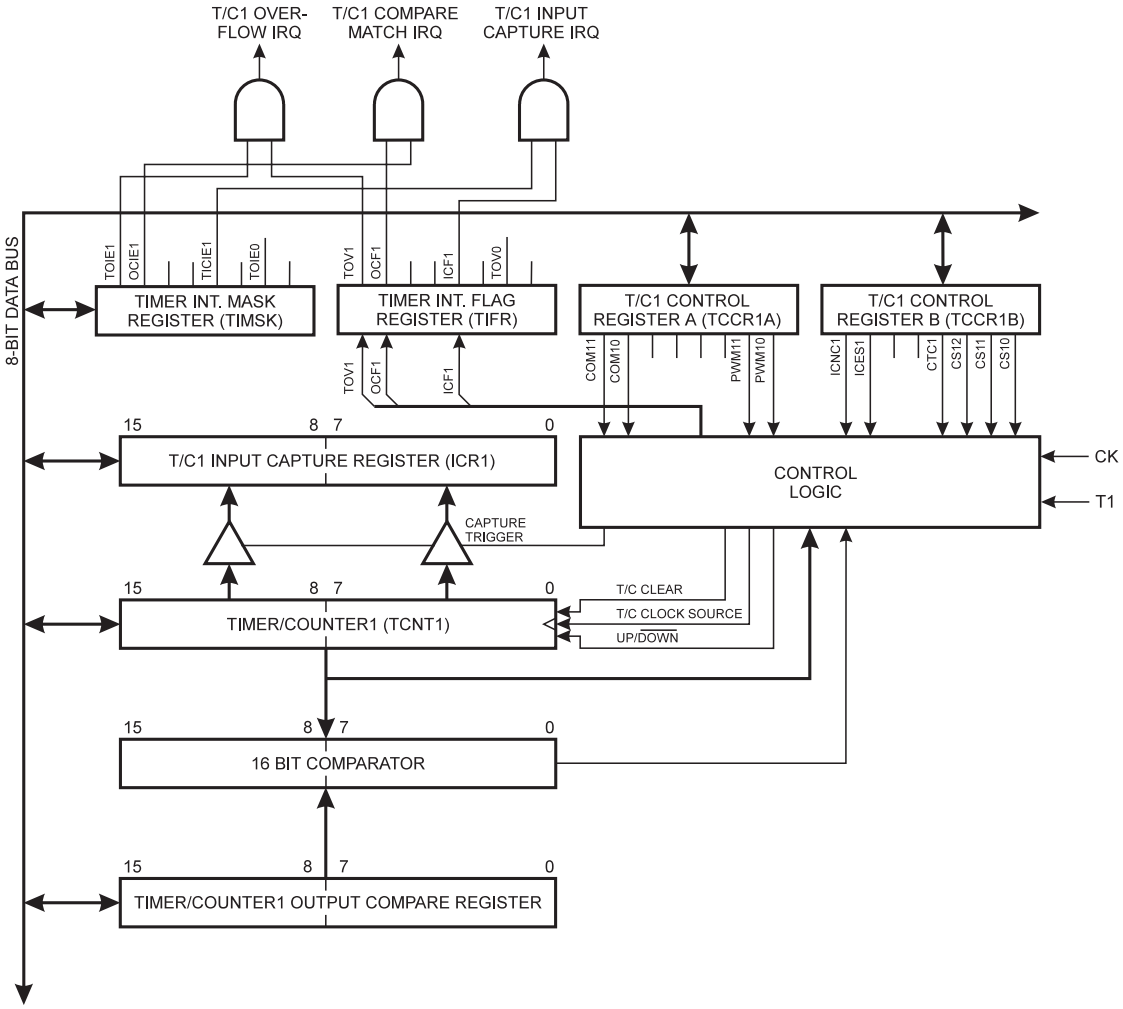
Bit	7	6	5	4	3	2	1	0	
$32 ($52)	MSB							LSB	TCNT0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

The Timer/Counter0 is realized as an up-counter with read and write access. If the Timer/Counter0 is written and a clock source is present, the Timer/Counter0 continues counting in the clock cycle following the write operation.

16-bit Timer/Counter1

Figure 32 shows the block diagram for Timer/Counter1.

Figure 32. Timer/Counter1 Block Diagram



The 16-bit Timer/Counter1 can select clock source from CK, prescaled CK, or an external pin. In addition it can be stopped as described in the specification for the Timer/Counter1 Control Register - TCCR1A. The different status flags (overflow, compare match and capture event) and control signals are found in the Timer/Counter Interrupt Flag Register - TIFR. The interrupt enable/disable settings for Timer/Counter1 are found in the Timer/Counter Interrupt Mask Register - TIMSK.

- **Bits 1,0 - SPR1, SPR0: SPI Clock Rate Select 1 and 0**

These two bits control the SCK rate of the device configured as a master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the Oscillator Clock frequency f_{cl} is shown in the following table:

Table 18. Relationship Between SCK and the Oscillator Frequency

SPR1	SPR0	SCK Frequency
0	0	f_{cl} / 4
0	1	f_{cl} / 16
1	0	f_{cl} / 64
1	1	f_{cl} / 128

SPI Status Register - SPSR

Bit	7	6	5	4	3	2	1	0	
$0E ($2E)	**SPIF**	**WCOL**	**-**	**-**	**-**	**-**	**-**	**-**	**SPSR**
Read/Write	R	R	R	R	R	R	R	R	
Initial value	0	0	0	0	0	0	0	0	

- **Bit 7 - SPIF: SPI Interrupt Flag**

When a serial transfer is complete, the SPIF bit is set (one) and an interrupt is generated if SPIE in SPCR is set (one) and global interrupts are enabled. If $\overline{SS}$ is an input and is driven low when the SPI is in master mode, this will also set the SPIF flag. SPIF is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, the SPIF bit is cleared by first reading the SPI status register with SPIF set (one), then accessing the SPI Data Register (SPDR).

- **Bit 6 - WCOL: Write COLlision flag**

The WCOL bit is set if the SPI data register (SPDR) is written during a data transfer. The WCOL bit (and the SPIF bit) are cleared (zero) by first reading the SPI Status Register with WCOL set (one), and then accessing the SPI Data Register.

- **Bit 5..0 - Res: Reserved bits**

These bits are reserved bits in the AT90S2333/4433 and will always read as zero.

The SPI interface on the AT90S2333/4433 is also used for program memory and EEPROM downloading or uploading. See page 78 for serial programming and verification.

SPI Data Register - SPDR

Bit	7	6	5	4	3	2	1	0	
$0F ($2F)	**MSB**							**LSB**	**SPDR**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	X	X	X	X	X	X	X	X	Undefined

The SPI Data Register is a read/write register used for data transfer between the register file and the SPI Shift register. Writing to the register initiates data transmission. Reading the register causes the Shift Register Receive buffer to be read.

- **Bit 3 - OR: OverRun**

This bit is set if an Overrun condition is detected, i.e. when a character already present in the UDR register is not read before the next character has been shifted into the Receiver Shift register. The OR bit is buffered, which means that it will be set once the valid data still in UDRE is read.

The OR bit is cleared (zero) when data is received and transferred to UDR.

- **Bits 2..1 - Res: Reserved bits**

These bits are reserved bits in the AT90S2333/4433 and will always read as zero.

- **Bit 0 - MPCM: Multi-Processor Communication Mode**

This bit is used to enter Multi-Processor Communication Mode. The bit is set when the slave MCU waits for an address byte to be received. When the MCU has been addressed, the MCU switches off the MPCM bit, and starts data reception.

For a detailed description, see “Multi-Processor Communication Mode”.

UART Control and Status Registers - UCSRB

Bit	7	6	5	4	3	2	1	0	
$0A ($2A)	**RXCIE**	**TXCIE**	**UDRIE**	**RXEN**	**TXEN**	**CHR9**	**RXB8**	**TXB8**	**UCSRB**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	W	
Initial value	0	0	0	0	0	0	1	0	

- **Bit 7 - RXCIE: RX Complete Interrupt Enable**

When this bit is set (one), a setting of the RXC bit in USR will cause the Receive Complete interrupt routine to be executed provided that global interrupts are enabled.

- **Bit 6 - TXCIE: TX Complete Interrupt Enable**

When this bit is set (one), a setting of the TXC bit in USR will cause the Transmit Complete interrupt routine to be executed provided that global interrupts are enabled.

- **Bit 5 - UDRIE: UART Data Register Empty Interrupt Enable**

When this bit is set (one), a setting of the UDRE bit in USR will cause the UART Data Register Empty interrupt routine to be executed provided that global interrupts are enabled.

- **Bit 4 - RXEN: Receiver Enable**

This bit enables the UART receiver when set (one). When the receiver is disabled, the TXC, OR and FE status flags cannot become set. If these flags are set, turning off RXEN does not cause them to be cleared.

- **Bit 3 - TXEN: Transmitter Enable**

This bit enables the UART transmitter when set (one). When disabling the transmitter while transmitting a character, the transmitter is not disabled before the character in the shift register plus any following character in UDR has been completely transmitted.

- **Bit 2 - CHR9: 9 Bit Characters**

When this bit is set (one) transmitted and received characters are 9 bit long plus start and stop bits. The 9th bit is read and written by using the RXB8 and TXB8 bits in UCR, respectively. The 9th data bit can be used as an extra stop bit or a parity bit.

- **Bit 1 - RXB8: Receive Data Bit 8**

When CHR9 is set (one), RXB8 is the 9th data bit of the received character.

- **Bit 0 - TXB8: Transmit Data Bit 8**

When CHR9 is set (one), TXB8 is the 9th data bit in the character to be transmitted.

Baud Rate Generator

The baud rate generator is a frequency divider which generates baud-rates according to the following equation:

$$BAUD = \frac{f_{CK}}{16(UBR + 1)}$$

- BAUD = Baud-Rate
- f_{CK}= Crystal Clock frequency
- UBR = Contents of the UBRRH and UBRR registers, (0-4095)

For standard crystal frequencies, the most commonly used baud rates can be generated by using the UBR settings in Table 19. UBR values which yield an actual baud rate differing less than 2% from the target baud rate, are bold in the table. However, using baud rates that have more than 1% error is not recommended. High error ratings give less noise resistanse.

Table 19. UBR Settings at Various Crystal Frequencies

Baud Rate	1 MHz		% Error	1.8432 MHz		% Error	2 MHz		% Error
2400	UBR=	**25**	**0.2**	UBR=	**47**	**0.0**	UBR=	**51**	**0.2**
4800	UBR=	**12**	**0.2**	UBR=	**23**	**0.0**	UBR=	**25**	**0.2**
9600	UBR=	6	7.5	UBR=	**11**	**0.0**	UBR=	**12**	**0.2**
14400	UBR=	3	7.8	UBR=	**7**	**0.0**	UBR=	8	3.7
19200	UBR=	2	7.8	UBR=	**5**	**0.0**	UBR=	6	7.5
28800	UBR=	1	7.8	UBR=	**3**	**0.0**	UBR=	3	7.8
38400	UBR=	1	22.9	UBR=	**2**	**0.0**	UBR=	2	7.8
57600	UBR=	0	7.8	UBR=	**1**	**0.0**	UBR=	1	7.8
76800	UBR=	0	22.9	UBR=	1	33.3	UBR=	1	22.9
115200	UBR=	0	84.3	UBR=	**0**	**0.0**	UBR=	0	7.8

Baud Rate	3.2768 MHz		% Error	3.6864 MHz		% Error	4 MHz		% Error
2400	UBR=	**84**	**0.4**	UBR=	**95**	**0.0**	UBR=	**103**	**0.2**
4800	UBR=	**42**	**0.8**	UBR=	**47**	**0.0**	UBR=	**51**	**0.2**
9600	UBR=	**20**	**1.6**	UBR=	**23**	**0.0**	UBR=	**25**	**0.2**
14400	UBR=	**13**	**1.6**	UBR=	**15**	**0.0**	UBR=	16	2.1
19200	UBR=	10	3.1	UBR=	**11**	**0.0**	UBR=	**12**	**0.2**
28800	UBR=	**6**	**1.6**	UBR=	**7**	**0.0**	UBR=	8	3.7
38400	UBR=	4	6.3	UBR=	**5**	**0.0**	UBR=	6	7.5
57600	UBR=	3	12.5	UBR=	**3**	**0.0**	UBR=	3	7.8
76800	UBR=	2	12.5	UBR=	**2**	**0.0**	UBR=	2	7.8
115200	UBR=	1	12.5	UBR=	**1**	**0.0**	UBR=	1	7.8

Baud Rate	7.3728 MHz		% Error	8 MHz		% Error	9.216 MHz		% Error
2400	UBR=	**191**	**0.0**	UBR=	**207**	**0.2**	UBR=	**239**	**0.0**
4800	UBR=	**95**	**0.0**	UBR=	**103**	**0.2**	UBR=	**119**	**0.0**
9600	UBR=	**47**	**0.0**	UBR=	**51**	**0.2**	UBR=	**59**	**0.0**
14400	UBR=	**31**	**0.0**	UBR=	**34**	**0.8**	UBR=	**39**	**0.0**
19200	UBR=	**23**	**0.0**	UBR=	**25**	**0.2**	UBR=	**29**	**0.0**
28800	UBR=	**15**	**0.0**	UBR=	16	2.1	UBR=	**19**	**0.0**
38400	UBR=	**11**	**0.0**	UBR=	**12**	**0.2**	UBR=	**14**	**0.0**
57600	UBR=	**7**	**0.0**	UBR=	8	3.7	UBR=	**9**	**0.0**
76800	UBR=	**5**	**0.0**	UBR=	6	7.5	UBR=	7	6.7
115200	UBR=	**3**	**0.0**	UBR=	3	7.8	UBR=	**4**	**0.0**

UART Baud Rate Register - UBRR

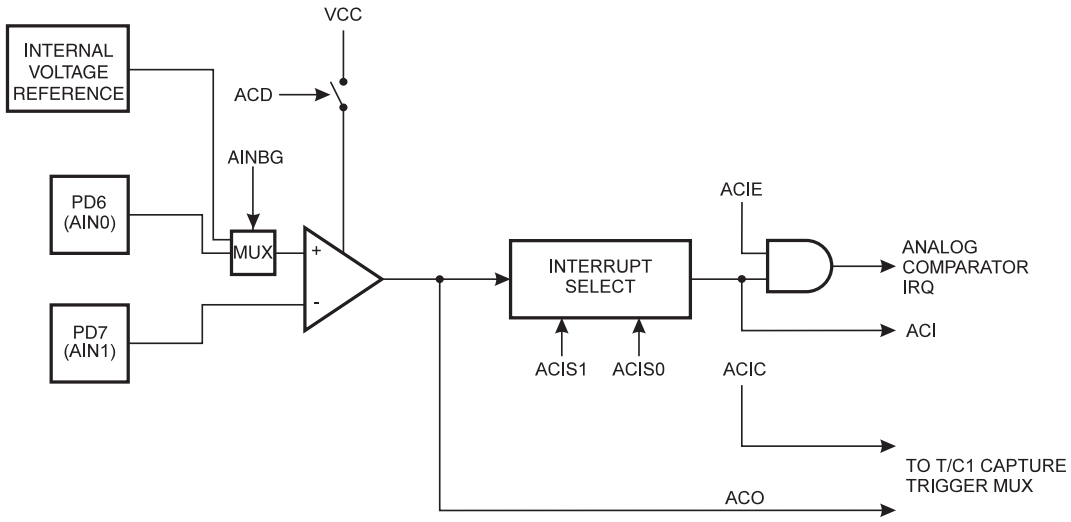
Bit	15	14	13	12	11	10	9	8	
$03 ($23)	-	-	-	-	MSB			LSB	UBRRHI
$09 ($29)	MSB							LSB	UBRR
	7	6	5	4	3	2	1	0	
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

This is a 12-bit register which contains the UART Baud Rate according to the equation on the previous page. The UBRRHI contains the 4 most significant bits, and the UBRR contains the 8 least significant bits of the UART Baud Rate.

Analog Comparator

The analog comparator compares the input values on the positive input PD6 (AIN0) and negative input PD7 (AIN1). When the voltage on the positive input PD6 (AIN0) is higher than the voltage on the negative input PD7 (AIN1), the Analog Comparator Output, ACO is set (one). The comparator's output can be set to trigger the Timer/Counter1 Input Capture function. In addition, the comparator can trigger a separate interrupt, exclusive to the Analog Comparator. The user can select Interrupt triggering on comparator output rise, fall or toggle. A block diagram of the comparator and its surrounding logic is shown in Figure 43.

Figure 43. Analog Comparator Block Diagram



Analog Comparator Control And Status Register - ACSR

Bit	7	6	5	4	3	2	1	0	
$08 ($28)	ACD	AINBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	ACSR
Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

- **Bit 7 - ACD: Analog Comparator Disable**

When this bit is set(one), the power to the analog comparator is switched off. This bit can be set at any time to turn off the analog comparator. When changing the ACD bit, the Analog Comparator Interrupt must be disabled by clearing the ACIE bit in ACSR. Otherwise an interrupt can occur when the bit is changed.

Figure 46. ADC Timing Diagram, First Conversion (Single Conversion Mode)

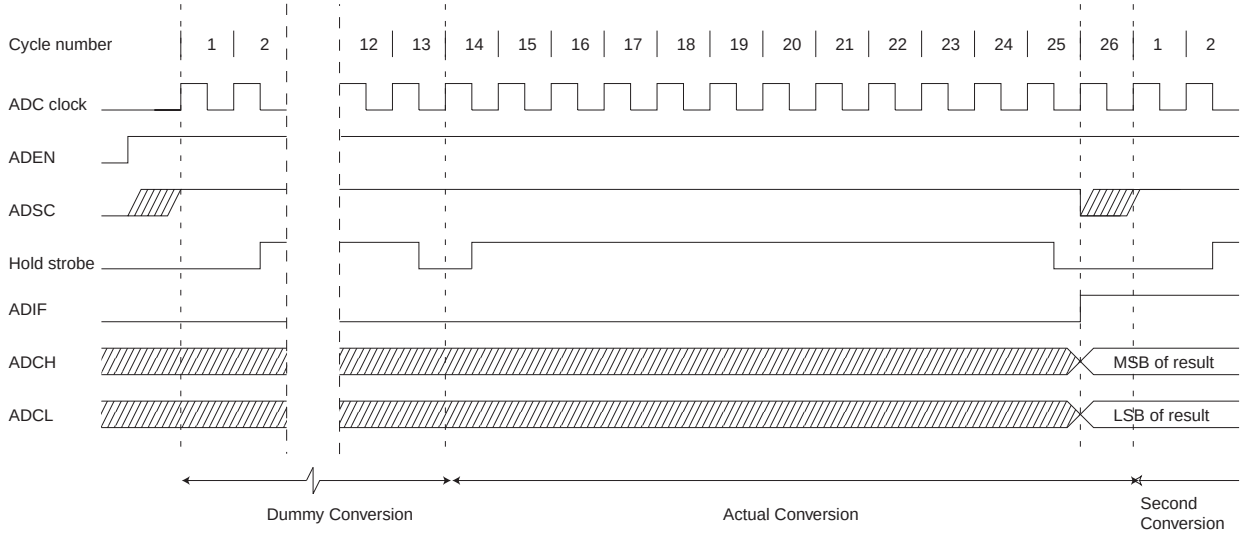
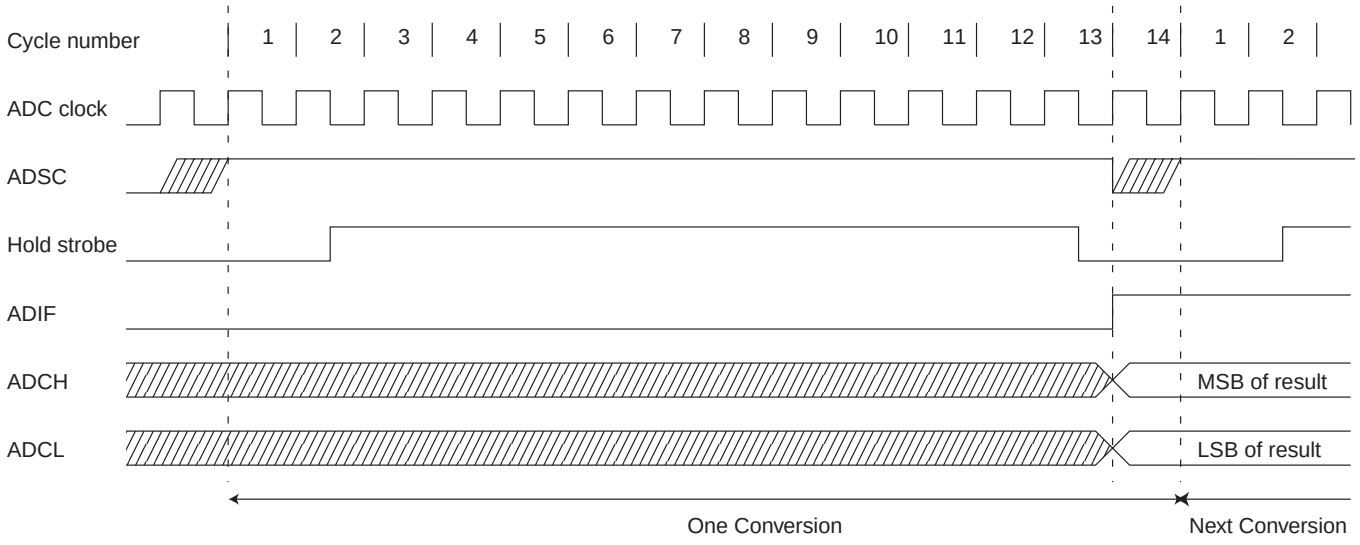


Table 21. ADC Conversion Time

Condition	Sample Cycle Number	Result Ready (cycle number)	Total Conversion Time (cycles)	Total Conversion Time (µs)
1st Conversion, Free Run	14	25	25	125 - 500
1st Conversion, Single	14	25	26	130 - 520
Free Run Conversion	2	13	13	65 - 260
Single Conversion	2	13	14	70 - 280

Figure 47. ADC Timing Diagram, Single Conversion



Port C

Port C is a 6-bit bi-directional I/O port.

Three I/O memory address locations are allocated for the Port C, one each for the Data Register - PORTC, $15($35), Data Direction Register - DDRC, $14($34) and the Port C Input Pins - PINC, $13($33). The Port C Input Pins address is read only, while the Data Register and the Data Direction Register are read/write.

All port pins have individually selectable pull-up resistors. The Port C output buffers can sink 20mA and thus drive LED displays directly. When pins PC0 to PC5 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated.

Port C has an alternate function as analog inputs for the ADC. If some Port C pins are configured as outputs, it is essential that these do not switch when a conversion is in progress. This might corrupt the result of the conversion.

During Power Down Mode, the schmitt triggers of the digital inputs are disconnected. This allows an analog voltage close to $V_{CC}/2$ to be present during power down without causing excessive power consumption.

Port C Data Register - PORTC

Bit	7	6	5	4	3	2	1	0	
$15 ($35)	-	-	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	PORTC
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

Port C Data Direction Register - DDRC

Bit	7	6	5	4	3	2	1	0	
$14 ($34)	-	-	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	DDRC
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

Port C Input Pins Address - PINC

Bit	7	6	5	4	3	2	1	0	
$13 ($33)	-	-	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	PINC
Read/Write	R	R	R	R	R	R	R	R	
Initial value	Q	Q	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	

The Port C Input Pins address - PINC - is not a register, and this address enables access to the physical value on each Port C pin. When reading PORTC, the Port C Data Latch is read, and when reading PINC, the logical values present on the pins are read.

Port C As General Digital I/O

All 6 pins in Port C have equal functionality when used as digital I/O pins.

PCn, General I/O pin: The DDCn bit in the DDRC register selects the direction of this pin, if DDCn is set (one), PCn is configured as an output pin. If DDCn is cleared (zero), PCn is configured as an input pin. If PORTCn is set (one) when the pin configured as an input pin, the MOS pull up resistor is activated. To switch the pull up resistor off, PORTCn has to be cleared (zero) or the pin has to be configured as an output pin.The port pins are tristated when a reset condition becomes active, even if the clock is not running

Table 30. Pin Name Mapping

Signal Name in Programming Mode	Pin Name	I/O	Function
RDY/$\overline{\text{BSY}}$	PD1	O	0: Device is busy programming, 1: Device is ready for new command
$\overline{\text{OE}}$	PD2	I	Output Enable (Active low)
$\overline{\text{WR}}$	PD3	I	Write Pulse (Active low)
BS	PD4	I	Byte Select (‘0’ selects low byte, ‘1’ selects high byte)
XA0	PD5	I	XTAL Action Bit 0
XA1	PD6	I	XTAL Action Bit 1
DATA	PC1-0, PB5-0	I/O	Bidirectional Databus (Output when $\overline{\text{OE}}$ is low)

Table 31. XA1 and XA0 Coding

XA1	XA0	Action when XTAL1 is Pulsed
0	0	Load Flash or EEPROM Address (High or low address byte determined by BS)
0	1	Load Data (High or Low data byte for Flash determined by BS)
1	0	Load Command
1	1	No Action, Idle

Table 32. Command Byte Bit Coding

Command Byte	Command Executed
1000 0000	Chip Erase
0100 0000	Write Fuse Bits
0010 0000	Write Lock Bits
0001 0000	Write Flash
0001 0001	Write EEPROM
0000 1000	Read Signature Bytes
0000 0100	Read Fuse and Lock Bits
0000 0010	Read Flash
0000 0011	Read EEPROM

Enter Programming Mode

The following algorithm puts the device in parallel programming mode:

1. Apply supply voltage according to Table 29, between V_{CC} and GND.
2. Set the $\overline{\text{RESET}}$ and BS pin to ‘0’ and wait at least 100 ns.
3. Apply 11.5 - 12.5V to $\overline{\text{RESET}}$. Any activity on BS within 100 ns after +12V has been applied to $\overline{\text{RESET}}$, will cause the device to fail entering programming mode.

Chip Erase

The Chip Erase command will erase the Flash and EEPROM memories, and the Lock bits. The Lock bits are not reset until the Flash and EEPROM have been completely erased. The Fuse bits are not changed. Chip Erase must be performed before the Flash or EEPROM is reprogrammed.

Load Command “Chip Erase”

Bit 5 = SPIEN Fuse bit
Bit 4 = BODLEVEL Fuse bit
Bit 3 = BODEN Fuse bit
Bit 2 = CKSEL2 Fuse bit
Bit 1 = CKSEL1 Fuse bit
Bit 0 = CKSEL0 Fuse bit

3. Set BS to ‘1’. The status of the Lock bits can now be read at DATA (‘0’ means programmed).
   Bit 2 = Lock Bit2
   Bit 1= Lock Bit1
4. Set $\overline{OE}$ to ‘1’.

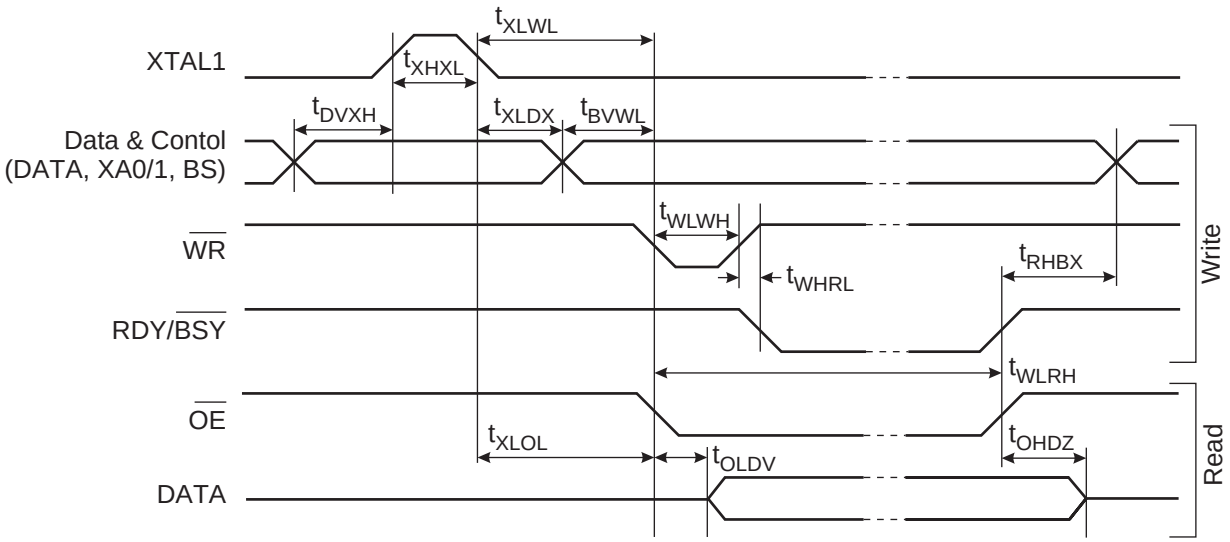
Reading the Signature Bytes

The algorithm for reading the Signature bytes is as follows (refer to Programming the Flash for details on Command and Address loading):

1. A: Load Command ‘0000 1000’.
2. C: Load Address Low Byte ($00 - $02).
   Set $\overline{OE}$ to ‘0’, and BS to ‘0’. The selected Signature byte can now be read at DATA.
3. Set $\overline{OE}$ to ‘1’.

Parallel Programming Characteristics

Figure 65. Parallel Programming Timing



For the EEPROM, an auto-erase cycle is provided within the self-timed write instruction and there is no need to first execute the Chip Erase instruction. The Chip Erase instruction turns the content of every memory location in both the Program and EEPROM arrays into $FF.

The Program and EEPROM memory arrays have separate address spaces:

0000 to $03FF/$07FF (AT90S2333/AT90S4433) for Program memory and $0000 to $007F/$00FF (AT90S2333/AT90S4433) for EEPROM memory.

Either an external system clock is supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2.The minimum low and high periods for the serial clock (SCK) input are defined as follows:

Low:> 2 XTAL1 clock cycles

High:> 2 XTAL1 clock cycles

Serial Programming Algorithm

When writing serial data to the AT90S2333/AT90S4433, data is clocked on the rising edge of CLK.

When reading data from the AT90S2333/AT90S4433, data is clocked on the falling edge of CLK. See Figure 67, Figure 68 and Table 36 for details.

To program and verify the AT90S2333/AT90S4433 in the serial programming mode, the following sequence is recommended (See four byte instruction formats in Table 35):

1. Power-up sequence:

   Apply power between V_{CC} and GND while $\overline{\text{RESET}}$ and SCK are set to ‘0’. If a crystal is not connected across pins XTAL1 and XTAL2, apply a clock signal to the XTAL1 pin. In some systems, the programmer can not guarantee that SCK is held low during power-up. In this case, $\overline{\text{RESET}}$ must be given a positive pulse of at least two XTAL1 cycles duration after SCK has been set to ‘0’.
2. Wait for at least 20 ms and enable serial programming by sending the Programming Enable serial instruction to pin MOSI/PB3.
3. The serial programming instructions will not work if the communication is out of syncronization. When in sync, the second byte ($53) will echo back when issuing the third byte of the Programming Enable instruction. Wheter the echo is correct or not, all 4 bytes of the instruction must be transmitted. If the $53 did not echo back, give SCK a positive pulse and issue a new Programming Enable instruction. If the $53 is not seen within 32 attempts, there is no functional device connected.
4. If a Chip Erase is performed (must be done to erase the Flash), wait t_{WD_ERASE} after the instruction, give $\overline{\text{RESET}}$ a positive pulse, and start over from Step 2. See Table 37 on page 82 for t_{WD_ERASE} value.
5. The Flash or EEPROM array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. An EEPROM memory location is first automatically erased before new data is written. Use Data Polling to detect when the next byte in the Flash or EEPROM can be written. If polling is not used, wait t_{WD_PROG} before transmitting the next instruction. In an erased device, no $FFs in the data file(s) needs to be programmed. See Table 38 on page 82 for t_{WD_PROG} value.
6. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/PB4.
7. At the end of the programming session, $\overline{\text{RESET}}$ can be set high to commence normal operation.
8. Power-off sequence (if needed):

   Set XTAL1 to ‘0’ (if a crystal is not used).

   Set $\overline{\text{RESET}}$ to ‘1’.

   Turn V_{CC} power off

Serial Programming Characteristics

Figure 68. Serial Programming Timing

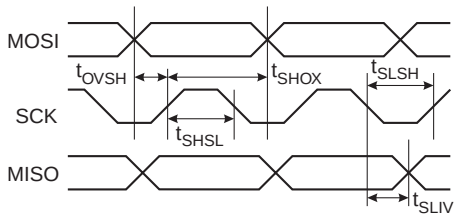


Table 36. Serial Programming Characteristics

T_A = -40°C to 85°C, V_{CC} = 2.7 - 6.0V (Unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency (V_{CC} = 2.7 - 6.0V)	0		4	MHz
t_{CLCL}	Oscillator Period (V_{CC} = 2.7 - 6.0V)	250			ns
$1/t_{CLCL}$	Oscillator Frequency (V_{CC} = 4.0 - 6.0V)	0		8	MHz
t_{CLCL}	Oscillator Period (V_{CC} = 4.0 - 6.0V)	125			ns
t_{SHSL}	SCK Pulse Width High	2 t_{CLCL}			ns
t_{SLSH}	SCK Pulse Width Low	2 t_{CLCL}			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	2 t_{CLCL}			ns
t_{SLIV}	SCK Low to MISO Valid	10	16	32	ns

Table 37. Minimum wait delay after the Chip Erase instruction

Symbol	3.2V	3.6V	4.0V	5.0V
t_{WD_ERASE}	18ms	14ms	12ms	8ms

Table 38. Minimum wait delay after writing a Flash or EEPROM location

Symbol	3.2V	3.6V	4.0V	5.0V
t_{WD_PROG}	9ms	7ms	6ms	4ms

Figure 73. Idle Supply Current vs. V_{CC}

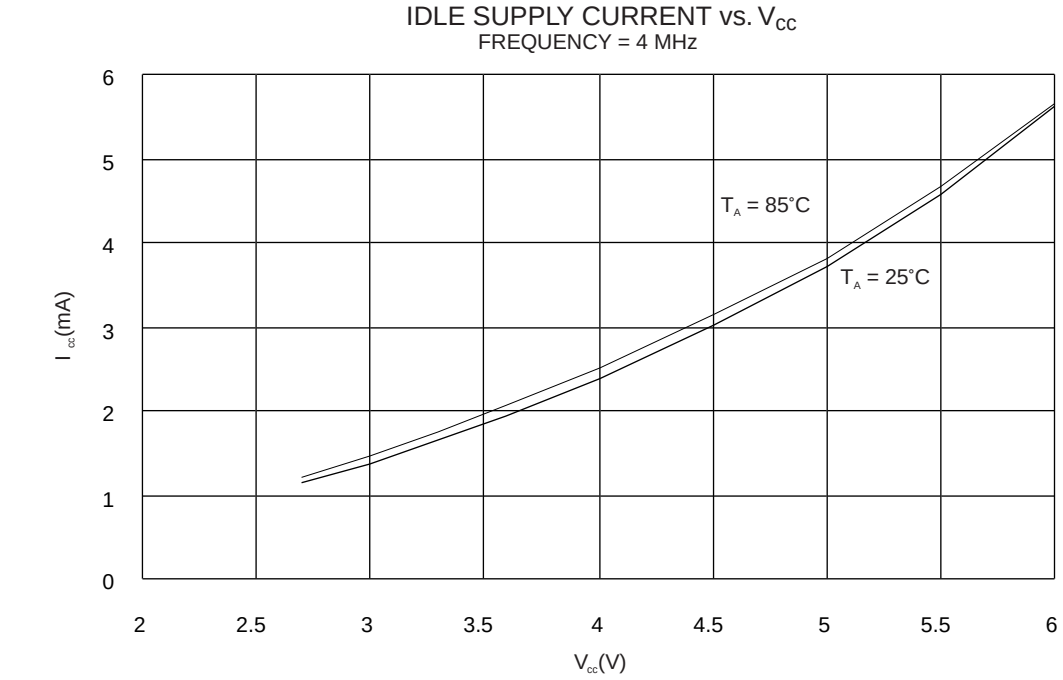
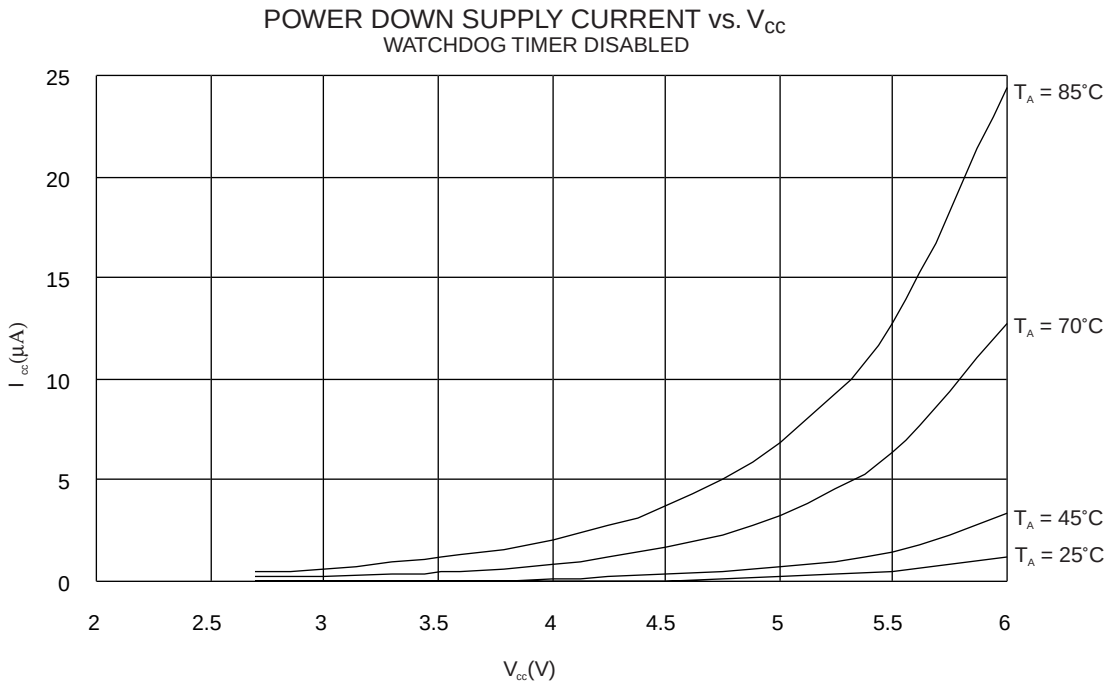


Figure 74. Power Down Supply Current vs. V_{CC}



Ordering Information

Power Supply	Speed (MHz)	Ordering Code	Package	Operation Range
2.7 - 6.0V	4	AT90LS2333-4AC AT90LS2333-4PC	32A 28P3	Commercial (0°C to 70°C)
		AT90LS2333-4AI AT90LS2333-4PI	32A 28P3	Industrial (-40°C to 85°C)
4.0 - 6.0V	8	AT90S2333-8AC AT90S2333-8PC	32A 28P3	Commercial (0°C to 70°C)
		AT90S2333-8AI AT90S2333-8PI	32A 28P3	Industrial (-40°C to 85°C)
2.7 - 6.0V	4	AT90LS4433-4AC AT90LS4433-4PC	32A 28P3	Commercial (0°C to 70°C)
		AT90LS4433-4AI AT90LS4433-4PI	32A 28P3	Industrial (-40°C to 85°C)
4.0 - 6.0V	8	AT90S4433-8AC AT90S4433-8PC	32A 28P3	Commercial (0°C to 70°C)
		AT90S4433-8AI AT90S4433-8PI	32A 28P3	Industrial (-40°C to 85°C)

Package Type	
28P3	28-lead, 0.300” Wide, Plastic Dual in Line Package (PDIP)
32A	32-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP)