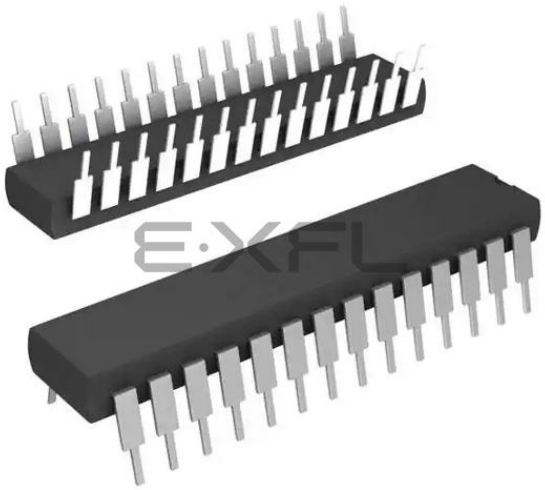

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	AVR
Core Size	8-Bit
Speed	4MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	20
Program Memory Size	2KB (1K x 16)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at90ls2333-4pi

Pin Descriptions

VCC

Supply voltage

GND

Ground

Port B (PB5..PB0)

Port B is a 6-bit bi-directional I/O port with internal pullup resistors. The Port B output buffers can sink 20 mA. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated.

Port B also serves the functions of various special features of the AT90S2333/4433 as listed on page 60.

The port B pins are tristated when a reset condition becomes active, even if the clock is not running.

Port C (PC5..PC0)

Port C is a 6-bit bi-directional I/O port with internal pullup resistors. The Port C output buffers can sink 20 mA. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. Port C also serves as the analog inputs to the A/D Converter.

The port C pins are tristated when a reset condition becomes active, even if the clock is not running.

Port D (PD7..PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors. The Port D output buffers can sink 20 mA. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated.

Port D also serves the functions of various special features of the AT90S2333/4433 as listed on page 67.

The port D pins are tristated when a reset condition becomes active, even if the clock is not running.

$\overline{\text{RESET}}$

Reset input. An external reset is generated by a low level on the $\overline{\text{RESET}}$ pin. Reset pulses longer than 50 ns will generate a reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a reset.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier

AVCC

This is the supply voltage pin for the A/D Converter. It should be externally connected to V_{CC} via a low-pass filter. See page 52 for details on operation of the ADC.

AREF

This is the analog reference input for the A/D Converter. For ADC operations, a voltage in the range 2.7V to AVCC must be applied to this pin.

AGND

If the board has a separate analog ground plane, this pin should be connected to this ground plane. Otherwise, connect to GND.

The 32 general purpose working registers, 64 I/O registers and the 128 bytes of internal data SRAM in the AT90S2333/4433 are all accessible through all these addressing modes.

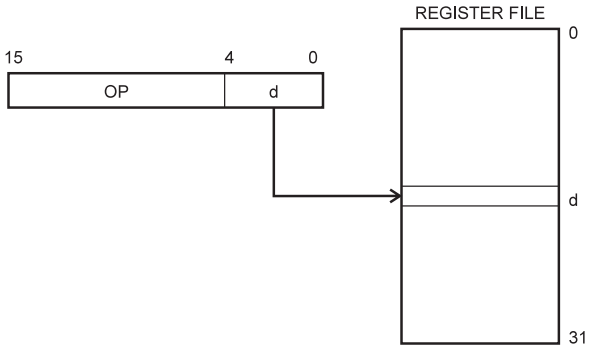
See the next section for a detailed description of the different addressing modes.

Program and Data Addressing Modes

The AT90S2333/4433 AVR RISC microcontroller supports powerful and efficient addressing modes for access to the Flash program memory, SRAM, Register File, and I/O data memory. This section describes the different addressing modes supported by the AVR architecture. In the figures, OP means the operation code part of the instruction word. To simplify, not all figures show the exact location of the addressing bits.

Register Direct, Single Register Rd

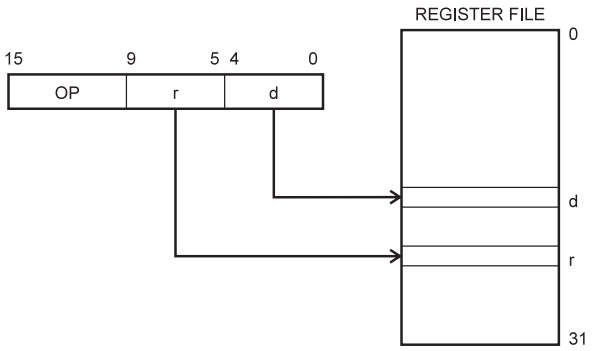
Figure 10. Direct Single Register Addressing



The operand is contained in register d (Rd).

Register Direct, Two Registers Rd and Rr

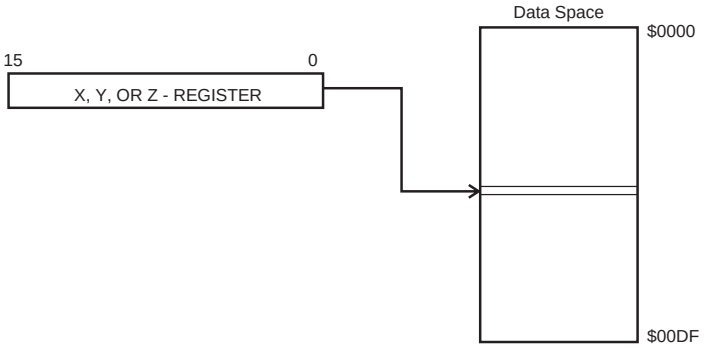
Figure 11. Direct Register Addressing, Two Registers



Operands are contained in register r (Rr) and d (Rd). The result is stored in register d (Rd).

Data Indirect

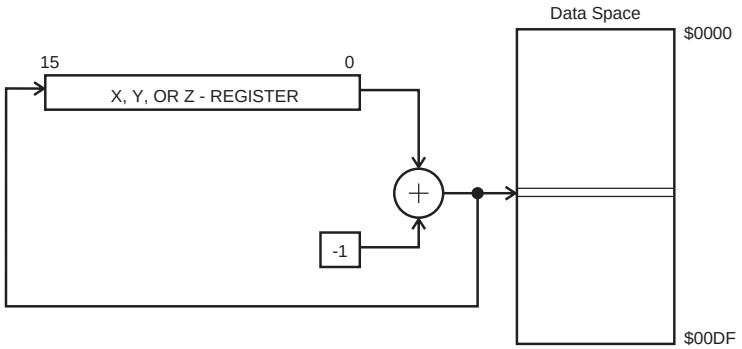
Figure 15. Data Indirect Addressing



Operand address is the contents of the X, Y, or the Z-register.

Data Indirect with Pre-Decrement

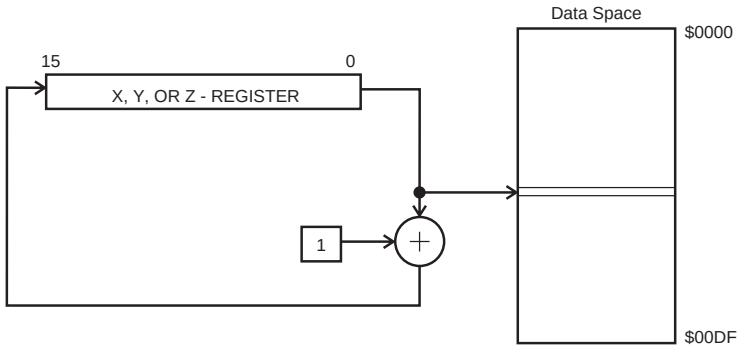
Figure 16. Data Indirect Addressing with Pre-Decrement



The X, Y, or the Z-register is decremented before the operation. Operand address is the decremented contents of the X, Y, or the Z-register.

Data Indirect with Post-Increment

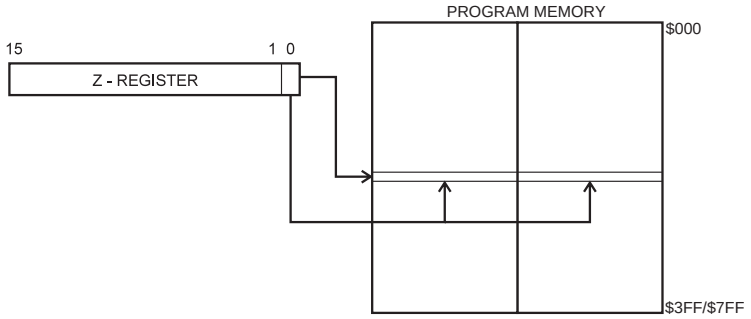
Figure 17. Data Indirect Addressing with Post-Increment



The X, Y, or the Z-register is incremented after the operation. Operand address is the content of the X, Y, or the Z-register prior to incrementing.

Constant Addressing Using the LPM Instruction

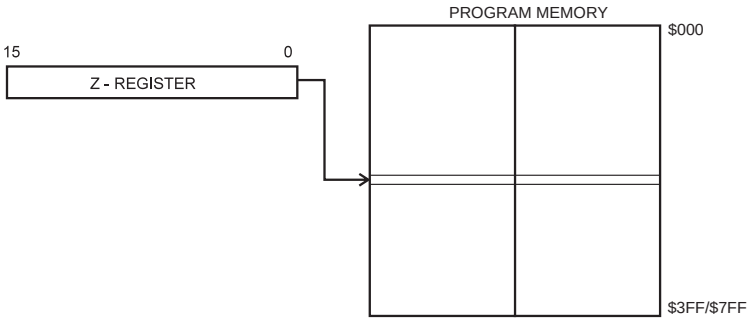
Figure 18. Code Memory Constant Addressing



Constant byte address is specified by the Z-register contents. The 15 MSBs select word address (0 - 1K/2K), the LSB selects low byte if cleared (LSB = 0) or high byte if set (LSB = 1).

Indirect Program Addressing, IJMP and ICALL

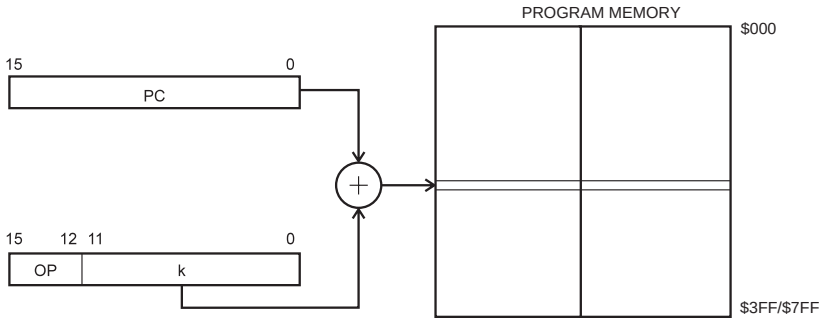
Figure 19. Indirect Program Memory Addressing



Program execution continues at address contained by the Z-register (i.e. the PC is loaded with the contents of the Z-register).

Relative Program Addressing, RJMP and RCALL

Figure 20. Relative Program Memory Addressing



Program execution continues at address PC + k + 1. The relative address k is from -2048 to 2047.

instruction, and it is incremented by two when an address is popped from the Stack with return from subroutine RET or return from interrupt RETI.

Reset and Interrupt Handling

The AT90S2333/4433 provides 13 different interrupt sources. These interrupts and the separate reset vector, each have a separate program vector in the program memory space. All interrupts are assigned individual enable bits which must be set (one) together with the I-bit in the status register in order to enable the interrupt.

The lowest addresses in the program memory space are automatically defined as the Reset and Interrupt vectors. The complete list of vectors is shown in Table 3. The list also determines the priority levels of the different interrupts. The lower the address the higher is the priority level. RESET has the highest priority, and next is INT0 - the External Interrupt Request 0, etc.

Table 3. Reset and Interrupt Vectors

Vector No.	Program Address	Source	Interrupt Definition
1	$000	RESET	External Pin, Power-On Reset, Brown-Out Reset and Watchdog Reset.
2	$001	INT0	External Interrupt Request 0
3	$002	INT1	External Interrupt Request 1
4	$003	TIMER1 CAPT	Timer/Counter1 Capture Event
5	$004	TIMER1 COMP	Timer/Counter1 Compare Match
6	$005	TIMER1 OVF	Timer/Counter1 Overflow
7	$006	TIMER0 OVF	Timer/Counter0 Overflow
8	$007	SPI, STC	Serial Transfer Complete
9	$008	UART, RX	UART, Rx Complete
10	$009	UART, UDRE	UART Data Register Empty
11	$00A	UART, TX	UART, Tx Complete
12	$00B	ADC	ADC Conversion Complete
13	$00C	EE_RDY	EEPROM Ready
14	$00D	ANA_COMP	Analog Comparator

The most typical program setup for the Reset and Interrupt Vector Addresses are:

```
Address             Labels     Code              Comments
$000                           rjmp    RESET     ; Reset Handler
$001                           rjmp    EXT_INT0  ; IRQ0 Handler
$002                           rjmp    EXT_INT1  ; IRQ1 Handler
$003                           rjmp    TIM1_CAPT ; Timer1 Capture Handler
$004                           rjmp    TIM1_COMP ; Timer1 compare Handler
$005                           rjmp    TIM1_OVF  ; Timer1 Overflow Handler
$006                           rjmp    TIM0_OVF  ; Timer0 Overflow Handler
$007                           rjmp    SPI_STC;  ; SPI Transfer Complete Handler
$008                           rjmp    UART_RXC  ; UART RX Complete Handler
$009                           rjmp    UART_DRE  ; UDR Empty Handler
$00a                           rjmp    UART_TXC  ; UART TX Complete Handler
$00b                           rjmp    ADC       ; ADC Conversion Complete Interrupt Handler
$00c                           rjmp    EE_RDY    ; EEPROM Ready Handler
$00d                           rjmp    ANA_COMP  ; Analog Comparator Handler
;
```

- **Bits 5..2 - Res: Reserved bits**

These bits are reserved bits in the AT90S2333/4433 and always read zero.

- **Bits 1,0 - PWM11, PWM10: Pulse Width Modulator Select Bits**

These bits select PWM operation of Timer/Counter1 as specified in Table 11. This mode is described on page 34.

Table 11. PWM Mode Select

PWM11	PWM10	Description
0	0	PWM operation of Timer/Counter1 is disabled
0	1	Timer/Counter1 is an 8-bit PWM
1	0	Timer/Counter1 is a 9-bit PWM
1	1	Timer/Counter1 is a 10-bit PWM

Timer/Counter1 Control Register B - TCCR1B

Bit	7	6	5	4	3	2	1	0	
$2E ($4E)	**ICNC1**	**ICES1**	**-**	**-**	**CTC1**	**CS12**	**CS11**	**CS10**	**TCCR1B**
Read/Write	R/W	R/W	R	R	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

- **Bit 7 - ICNC1: Input Capture1 Noise Canceler (4 CKs)**

When the ICNC1 bit is cleared (zero), the input capture trigger noise canceler function is disabled. The input capture is triggered at the first rising/falling edge sampled on the ICP - input capture pin - as specified. When the ICNC1 bit is set (one), four successive samples are measured on the ICP - input capture pin, and all samples must be high/low according to the input capture trigger specification in the ICES1 bit. The actual sampling frequency is the XTAL clock frequency.

- **Bit 6 - ICES1: Input Capture1 Edge Select**

While the ICES1 bit is cleared (zero), the Timer/Counter1 contents are transferred to the Input Capture Register - ICR1 - on the falling edge of the input capture pin - ICP. While the ICES1 bit is set (one), the Timer/Counter1 contents are transferred to the Input Capture Register - ICR1 - on the rising edge of the input capture pin - ICP.

- **Bits 5, 4 - Res: Reserved bits**

These bits are reserved bits in the AT90S2333/4433 and always read zero.

- **Bit 3 - CTC1: Clear Timer/Counter1 on Compare match**

When the CTC1 control bit is set (one), the Timer/Counter1 is reset to $0000 in the clock cycle after a compare match. If the CTC1 control bit is cleared, Timer/Counter1 continues counting and is unaffected by a compare match. Since the compare match is detected in the CPU clock cycle following the match, this function will behave differently when a prescaling higher than 1 is used for the timer. When a prescaling of 1 is used, and the compare register is set to C, the timer will count as follows if CTC1 is set:

... | C-2 | C-1 | C | 0 | 1 | ...

When the prescaler is set to divide by 8, the timer will count like this:

... | C-2, C-2, C-2, C-2, C-2, C-2, C-2, C-2 | C-1, C-1, C-1, C-1, C-1, C-1, C-1, C-1 | C, 0, 0, 0, 0, 0, 0, 0, 0 | ...

In PWM mode, this bit has no effect.

- **Bits 2,1,0 - CS12, CS11, CS10: Clock Select1, bit 2,1 and 0**

The Clock Select1 bits 2,1 and 0 define the prescaling source of Timer/Counter1.

3. Each slave MCU reads the UDR register and determines if it has been selected. If so, it clears the MPCM bit in UCSRA, otherwise it waits for the next address byte.
4. For each received data byte, the receiving MCU will set the receive complete flag (RXC in UCSRA). In 8-bit mode, the receiving MCU will also generate a framing error (FE in UCSRA set), since the stop bit is zero. The other slave MCUs, which still have the MPCM bit set, will ignore the data byte. In this case, the UDR register and the RXC or FE flags will not be affected.
5. After the last byte has been transferred, the process repeats from step 2.

UART Control

UART I/O Data Register - UDR

Bit	7	6	5	4	3	2	1	0	
$0C ($2C)	**MSB**							**LSB**	**UDR**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

The UDR register is actually two physically separate registers sharing the same I/O address. When writing to the register, the UART Transmit Data register is written. When reading from UDR, the UART Receive Data register is read.

UART Control and Status Registers - UCSRA

Bit	7	6	5	4	3	2	1	0	
$0B ($2B)	**RXC**	**TXC**	**UDRE**	**FE**	**OR**	**-**	**-**	**MPCM**	**UCSRA**
Read/Write	R	R/W	R	R	R	R	R	R/W	
Initial value	0	0	1	0	0	0	0	0	

- **Bit 7 - RXC: UART Receive Complete**

This bit is set (one) when a received character is transferred from the Receiver Shift register to UDR. The bit is set regardless of any detected framing errors. When the RXCIE bit in UCR is set, the UART Receive Complete interrupt will be executed when RXC is set(one). RXC is cleared by reading UDR. When interrupt-driven data reception is used, the UART Receive Complete Interrupt routine must read UDR in order to clear RXC, otherwise a new interrupt will occur once the interrupt routine terminates.

- **Bit 6 - TXC: UART Transmit Complete**

This bit is set (one) when the entire character (including the stop bit) in the Transmit Shift register has been shifted out and no new data has been written to UDR. This flag is especially useful in half-duplex communications interfaces, where a transmitting application must enter receive mode and free the communications bus immediately after completing the transmission.

When the TXCIE bit in UCR is set, setting of TXC causes the UART Transmit Complete interrupt to be executed. TXC is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, the TXC bit is cleared (zero) by writing a logical one to the bit.

- **Bit 5 - UDRE: UART Data Register Empty**

This bit is set (one) when a character written to UDR is transferred to the Transmit shift register. Setting of this bit indicates that the transmitter is ready to receive a new character for transmission.

When the UDRIE bit in UCR is set, the UART Transmit Complete interrupt to be executed as long as UDRE is set. UDRE is cleared by writing UDR. When interrupt-driven data transmittal is used, the UART Data Register Empty Interrupt routine must write UDR in order to clear UDRE, otherwise a new interrupt will occur once the interrupt routine terminates.

UDRE is set (one) during reset to indicate that the transmitter is ready.

- **Bit 4 - FE: Framing Error**

This bit is set if a Framing Error condition is detected, i.e. when the stop bit of an incoming character is zero.

The FE bit is cleared when the stop bit of received data is one.

- **Bit 3 - OR: OverRun**

This bit is set if an Overrun condition is detected, i.e. when a character already present in the UDR register is not read before the next character has been shifted into the Receiver Shift register. The OR bit is buffered, which means that it will be set once the valid data still in UDRE is read.

The OR bit is cleared (zero) when data is received and transferred to UDR.

- **Bits 2..1 - Res: Reserved bits**

These bits are reserved bits in the AT90S2333/4433 and will always read as zero.

- **Bit 0 - MPCM: Multi-Processor Communication Mode**

This bit is used to enter Multi-Processor Communication Mode. The bit is set when the slave MCU waits for an address byte to be received. When the MCU has been addressed, the MCU switches off the MPCM bit, and starts data reception.

For a detailed description, see “Multi-Processor Communication Mode”.

UART Control and Status Registers - UCSRB

Bit	7	6	5	4	3	2	1	0	
$0A ($2A)	**RXCIE**	**TXCIE**	**UDRIE**	**RXEN**	**TXEN**	**CHR9**	**RXB8**	**TXB8**	**UCSRB**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	W	
Initial value	0	0	0	0	0	0	1	0	

- **Bit 7 - RXCIE: RX Complete Interrupt Enable**

When this bit is set (one), a setting of the RXC bit in USR will cause the Receive Complete interrupt routine to be executed provided that global interrupts are enabled.

- **Bit 6 - TXCIE: TX Complete Interrupt Enable**

When this bit is set (one), a setting of the TXC bit in USR will cause the Transmit Complete interrupt routine to be executed provided that global interrupts are enabled.

- **Bit 5 - UDRIE: UART Data Register Empty Interrupt Enable**

When this bit is set (one), a setting of the UDRE bit in USR will cause the UART Data Register Empty interrupt routine to be executed provided that global interrupts are enabled.

- **Bit 4 - RXEN: Receiver Enable**

This bit enables the UART receiver when set (one). When the receiver is disabled, the TXC, OR and FE status flags cannot become set. If these flags are set, turning off RXEN does not cause them to be cleared.

- **Bit 3 - TXEN: Transmitter Enable**

This bit enables the UART transmitter when set (one). When disabling the transmitter while transmitting a character, the transmitter is not disabled before the character in the shift register plus any following character in UDR has been completely transmitted.

- **Bit 2 - CHR9: 9 Bit Characters**

When this bit is set (one) transmitted and received characters are 9 bit long plus start and stop bits. The 9th bit is read and written by using the RXB8 and TXB8 bits in UCR, respectively. The 9th data bit can be used as an extra stop bit or a parity bit.

- **Bit 1 - RXB8: Receive Data Bit 8**

When CHR9 is set (one), RXB8 is the 9th data bit of the received character.

- **Bit 0 - TXB8: Transmit Data Bit 8**

When CHR9 is set (one), TXB8 is the 9th data bit in the character to be transmitted.

Baud Rate Generator

The baud rate generator is a frequency divider which generates baud-rates according to the following equation:

$$BAUD = \frac{f_{CK}}{16(UBR + 1)}$$

- BAUD = Baud-Rate
- f_{CK}= Crystal Clock frequency
- UBR = Contents of the UBRRH and UBRR registers, (0-4095)

Figure 46. ADC Timing Diagram, First Conversion (Single Conversion Mode)

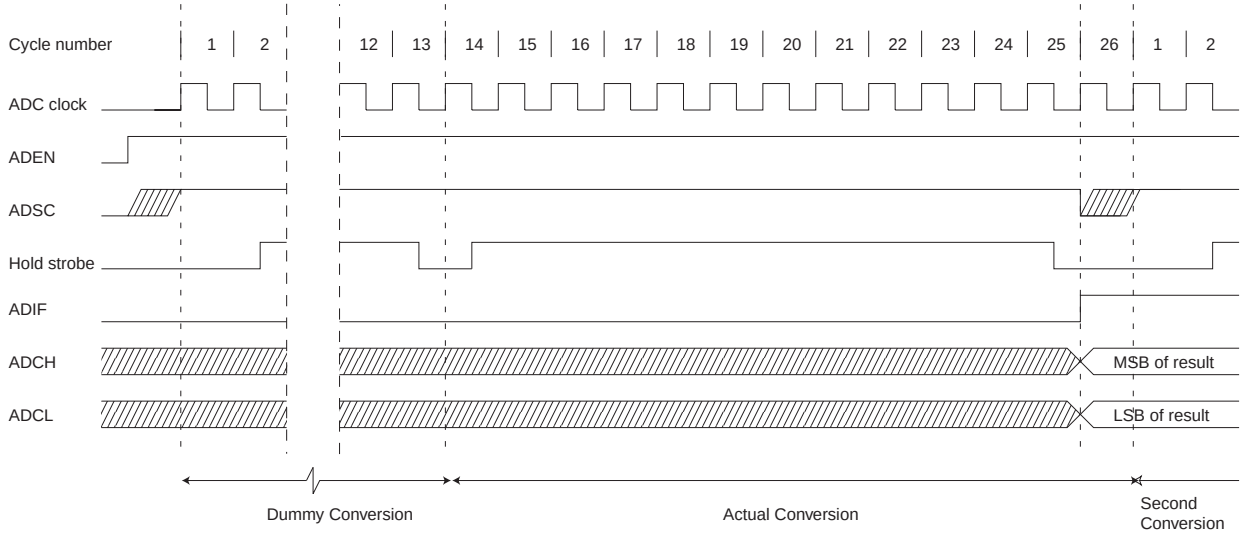


Table 21. ADC Conversion Time

Condition	Sample Cycle Number	Result Ready (cycle number)	Total Conversion Time (cycles)	Total Conversion Time (µs)
1st Conversion, Free Run	14	25	25	125 - 500
1st Conversion, Single	14	25	26	130 - 520
Free Run Conversion	2	13	13	65 - 260
Single Conversion	2	13	14	70 - 280

Figure 47. ADC Timing Diagram, Single Conversion

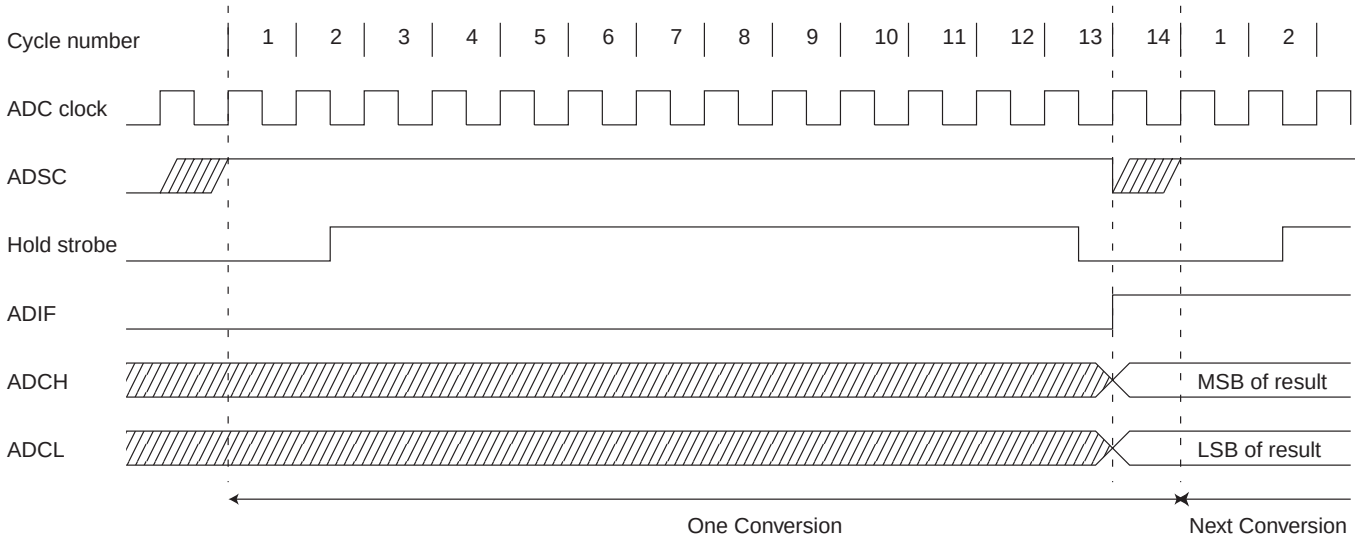


Figure 52. Port B Schematic Diagram (Pin PB2)

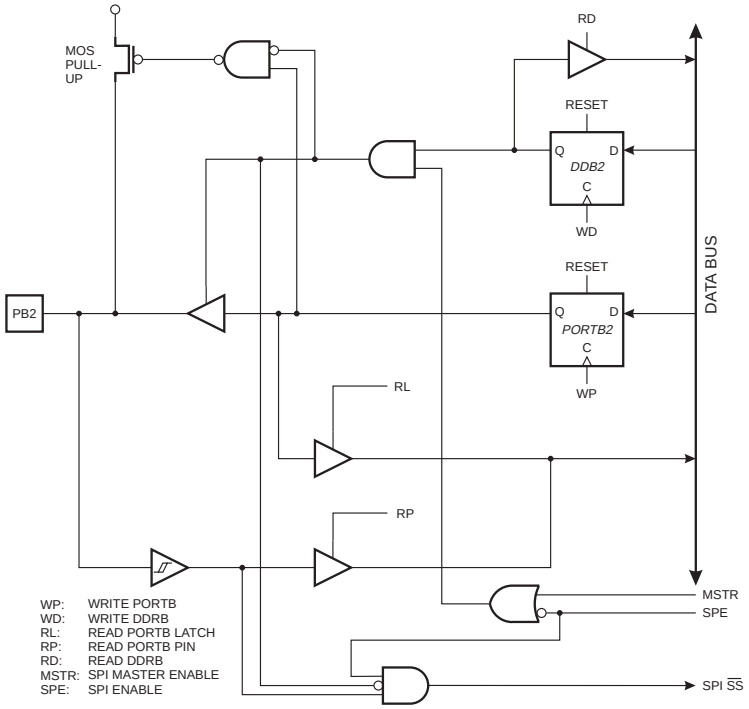


Figure 53. Port B Schematic Diagram (Pin PB3)

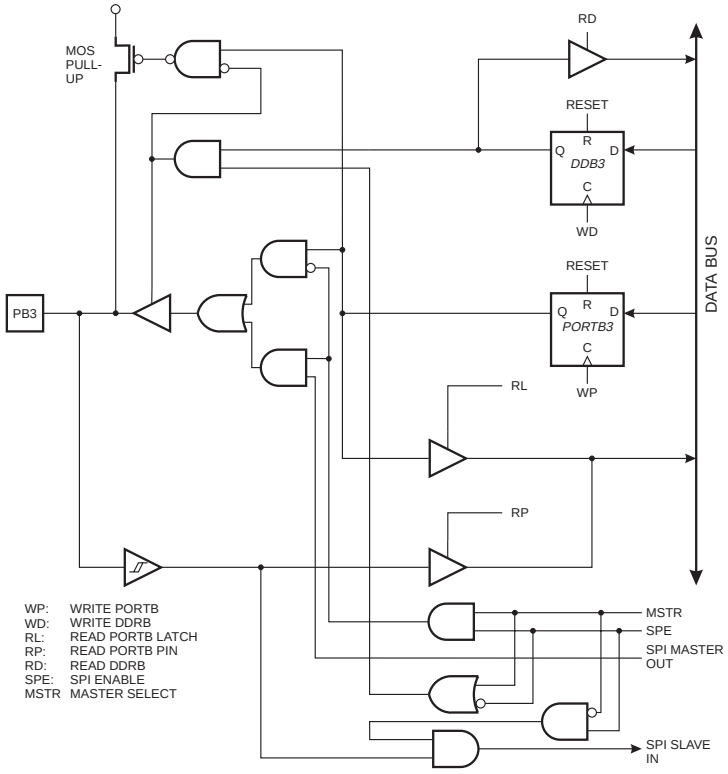


Table 25. DDCn Effects on Port C Pins

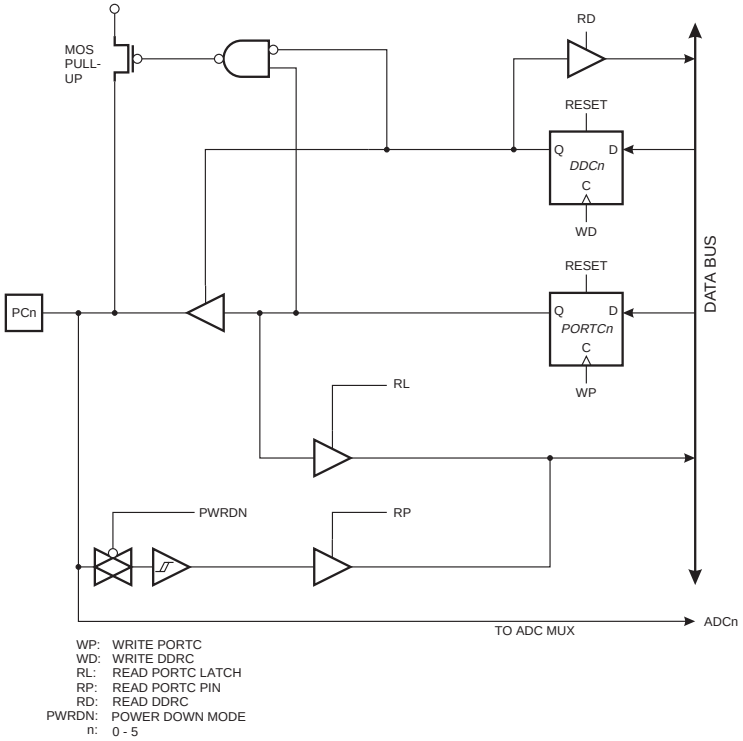
DDCn	PORTCn	I/O	Pull Up	Comment
0	0	Input	No	Tri-state (Hi-Z)
0	1	Input	Yes	PCn will source current if ext. pulled low.
1	0	Output	No	Push-Pull Zero Output
1	1	Output	No	Push-Pull One Output

Note: n: 5…0, pin number

Port C Schematics

Note that all port pins are synchronized. The synchronization latch is however, not shown in the figure.

Figure 56. Port C Schematic Diagrams (Pins PC0 - PC5)



Port D

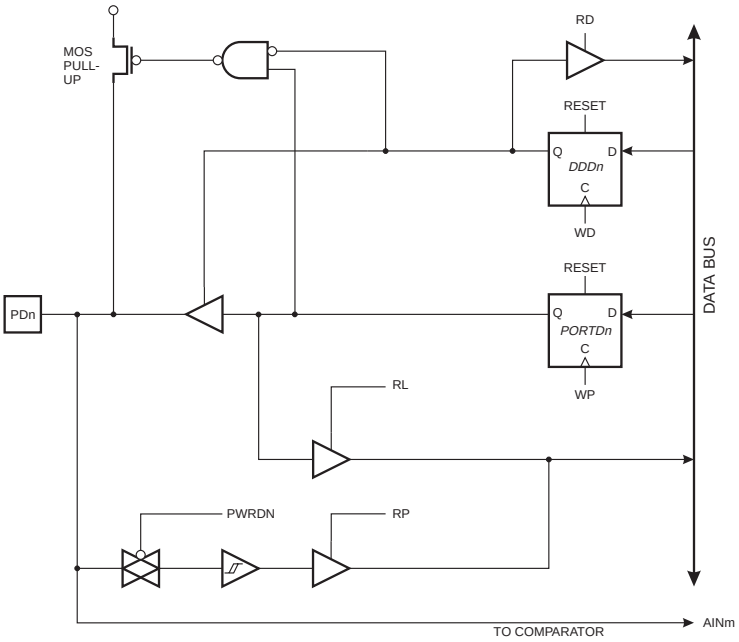
Port D is an 8 bit bi-directional I/O port with internal pull-up resistors.

Three I/O memory address locations are allocated for Port D, one each for the Data Register - PORTD, $12($32), Data Direction Register - DDRD, $11($31) and the Port D Input Pins - PIND, $10($30). The Port D Input Pins address is read only, while the Data Register and the Data Direction Register are read/write.

The Port D output buffers can sink 20 mA. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated.

Some Port D pins have alternate functions as shown in the following table:

Figure 61. Port D Schematic Diagram (Pins PD6 and PD7)



WP: WRITE PORTD
WD: WRITE DDRD
RL: READ PORTD LATCH
RP: READ PORTD PIN
RD: READ DDRD
PWRDN: POWER DOWN MODE
n: 6, 7
m: 0, 1

The Program and Data memory arrays on the AT90S2333/4433 are programmed byte-by-byte in either programming modes. For the EEPROM, an auto-erase cycle is provided within the self-timed write instruction in the serial programming mode. During programming, the supply voltage must be in accordance with Table 29.

Table 29. Supply voltage during programming

Part	Serial programming	Parallel programming
AT90LS2333	2.7 - 6.0 V	4.5 - 5.5 V
AT90S2333	4.0 - 6.0 V	4.5 - 5.5 V
AT90LS4433	2.7 - 6.0 V	4.5 - 5.5 V
AT90S4433	4.0 - 6.0 V	4.5 - 5.5 V

Parallel Programming

This section describes how to parallel program and verify Flash Program memory, EEPROM Data memory, Lock bits and Fuse bits in the AT90S2333/4433.

Signal Names

In this section, some pins of the AT90S2333/4433 are referenced by signal names describing their function during parallel programming. See Figure 62 and Table 30. Pins not described in Table 30 are referenced by pin names.

The XA1/XA0 pins determine the action executed when the XTAL1 pin is given a positive pulse. The bit coding are shown in Table 31.

When pulsing $\overline{WR}$ or $\overline{OE}$, the command loaded determines the action executed. The Command is a byte where the different bits are assigned functions as shown in Table 32.

Figure 62. Parallel Programming

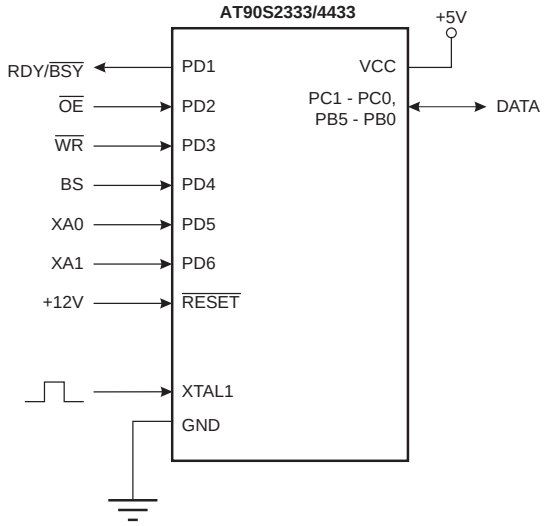


Table 33. Parallel Programming Characteristics T_A = 25°C ± 10%, V_{CC} =5V ± 10%

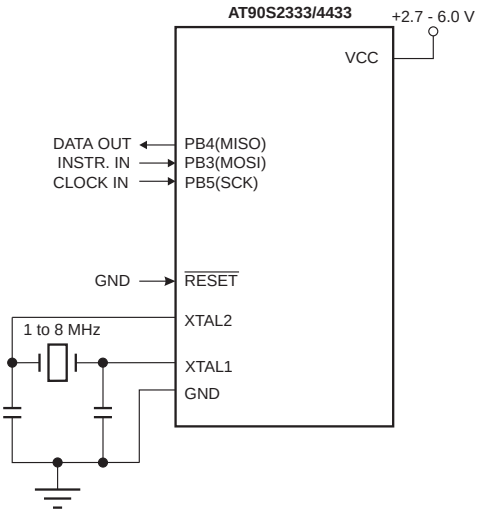
Symbol	Parameter	Min	Typ	Max	Units
V_{PP}	Programming Enable Voltage	11.5		12.5	V
I_{PP}	Programming Enable Current			250	µA
t_{DVXH}	Data and Control Setup before XTAL1 High	67			ns
t_{XHXL}	XTAL1 Pulse Width High	67			ns
t_{XLDX}	Data and Control Hold after XTAL1 Low	67			ns
t_{XLWL}	XTAL1 Low to $\overline{WR}$ Low	67			ns
t_{BVWL}	BS Valid to $\overline{WR}$ Low	67			ns
t_{RHBX}	BS Hold after RDY/$\overline{BSY}$ High	67			ns
t_{WLWH}	$\overline{WR}$ Pulse Width Low(1)	67			ns
t_{WHRL}	$\overline{WR}$ High to RDY/$\overline{BSY}$ Low(2)		20		ns
t_{WLRH}	$\overline{WR}$ Low to RDY/$\overline{BSY}$ High(2)	0.5	0.7	0.9	ms
t_{XLOL}	XTAL1 Low to $\overline{OE}$ Low	67			ns
t_{OLDV}	$\overline{OE}$ Low to DATA Valid		20		ns
t_{OHDZ}	$\overline{OE}$ High to DATA Tristated			20	ns
t_{WLWH_CE}	$\overline{WR}$ Pulse Width Low for Chip Erase	5	10	15	ms
t_{WLWH_PFB}	$\overline{WR}$ Pulse Width Low for Programming the Fuse Bits	1.0	1.5	1.8	ms

Notes: 1. Use t_{WLWH_CE} for Chip Erase and t_{WLWH_PFB} for Programming the Fuse Bits.
2. If t_{WLWH} is held longer than t_{WLRH}, no RDY/$\overline{BSY}$ pulse will be seen.

Serial Downloading

Both the Program and Data memory arrays can be programmed using the SPI bus while $\overline{RESET}$ is pulled to GND. The serial interface consists of pins SCK, MOSI (input) and MISO (output), see Figure 66. After $\overline{RESET}$ is set low, the Programming Enable instruction needs to be executed first before program/erase instructions can be executed.

Figure 66. Serial Programming and Verify



For the EEPROM, an auto-erase cycle is provided within the self-timed write instruction and there is no need to first execute the Chip Erase instruction. The Chip Erase instruction turns the content of every memory location in both the Program and EEPROM arrays into $FF.

The Program and EEPROM memory arrays have separate address spaces:

0000 to $03FF/$07FF (AT90S2333/AT90S4433) for Program memory and $0000 to $007F/$00FF (AT90S2333/AT90S4433) for EEPROM memory.

Either an external system clock is supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2.The minimum low and high periods for the serial clock (SCK) input are defined as follows:

Low:> 2 XTAL1 clock cycles

High:> 2 XTAL1 clock cycles

Serial Programming Algorithm

When writing serial data to the AT90S2333/AT90S4433, data is clocked on the rising edge of CLK.

When reading data from the AT90S2333/AT90S4433, data is clocked on the falling edge of CLK. See Figure 67, Figure 68 and Table 36 for details.

To program and verify the AT90S2333/AT90S4433 in the serial programming mode, the following sequence is recommended (See four byte instruction formats in Table 35):

1. Power-up sequence:

   Apply power between V_{CC} and GND while $\overline{\text{RESET}}$ and SCK are set to ‘0’. If a crystal is not connected across pins XTAL1 and XTAL2, apply a clock signal to the XTAL1 pin. In some systems, the programmer can not guarantee that SCK is held low during power-up. In this case, $\overline{\text{RESET}}$ must be given a positive pulse of at least two XTAL1 cycles duration after SCK has been set to ‘0’.
2. Wait for at least 20 ms and enable serial programming by sending the Programming Enable serial instruction to pin MOSI/PB3.
3. The serial programming instructions will not work if the communication is out of syncronization. When in sync, the second byte ($53) will echo back when issuing the third byte of the Programming Enable instruction. Wheter the echo is correct or not, all 4 bytes of the instruction must be transmitted. If the $53 did not echo back, give SCK a positive pulse and issue a new Programming Enable instruction. If the $53 is not seen within 32 attempts, there is no functional device connected.
4. If a Chip Erase is performed (must be done to erase the Flash), wait t_{WD_ERASE} after the instruction, give $\overline{\text{RESET}}$ a positive pulse, and start over from Step 2. See Table 37 on page 82 for t_{WD_ERASE} value.
5. The Flash or EEPROM array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. An EEPROM memory location is first automatically erased before new data is written. Use Data Polling to detect when the next byte in the Flash or EEPROM can be written. If polling is not used, wait t_{WD_PROG} before transmitting the next instruction. In an erased device, no $FFs in the data file(s) needs to be programmed. See Table 38 on page 82 for t_{WD_PROG} value.
6. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/PB4.
7. At the end of the programming session, $\overline{\text{RESET}}$ can be set high to commence normal operation.
8. Power-off sequence (if needed):

   Set XTAL1 to ‘0’ (if a crystal is not used).

   Set $\overline{\text{RESET}}$ to ‘1’.

   Turn V_{CC} power off

Serial Programming Characteristics

Figure 68. Serial Programming Timing

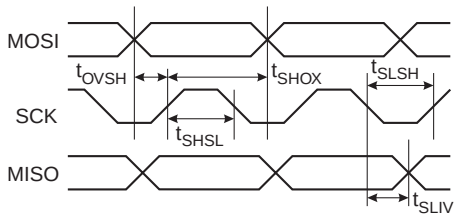


Table 36. Serial Programming Characteristics

T_A = -40°C to 85°C, V_{CC} = 2.7 - 6.0V (Unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency (V_{CC} = 2.7 - 6.0V)	0		4	MHz
t_{CLCL}	Oscillator Period (V_{CC} = 2.7 - 6.0V)	250			ns
$1/t_{CLCL}$	Oscillator Frequency (V_{CC} = 4.0 - 6.0V)	0		8	MHz
t_{CLCL}	Oscillator Period (V_{CC} = 4.0 - 6.0V)	125			ns
t_{SHSL}	SCK Pulse Width High	2 t_{CLCL}			ns
t_{SLSH}	SCK Pulse Width Low	2 t_{CLCL}			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	2 t_{CLCL}			ns
t_{SLIV}	SCK Low to MISO Valid	10	16	32	ns

Table 37. Minimum wait delay after the Chip Erase instruction

Symbol	3.2V	3.6V	4.0V	5.0V
t_{WD_ERASE}	18ms	14ms	12ms	8ms

Table 38. Minimum wait delay after writing a Flash or EEPROM location

Symbol	3.2V	3.6V	4.0V	5.0V
t_{WD_PROG}	9ms	7ms	6ms	4ms

Figure 79. Analog Comparator Offset Voltage vs. Common Mode Voltage

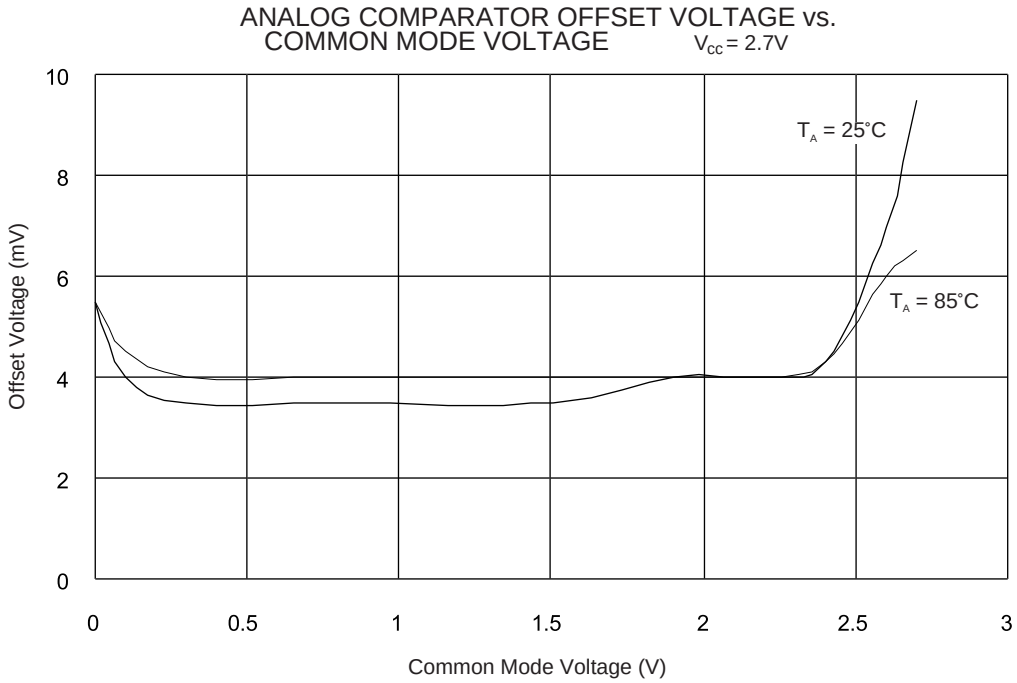


Figure 80. Analog Comparator Input Leakage Current

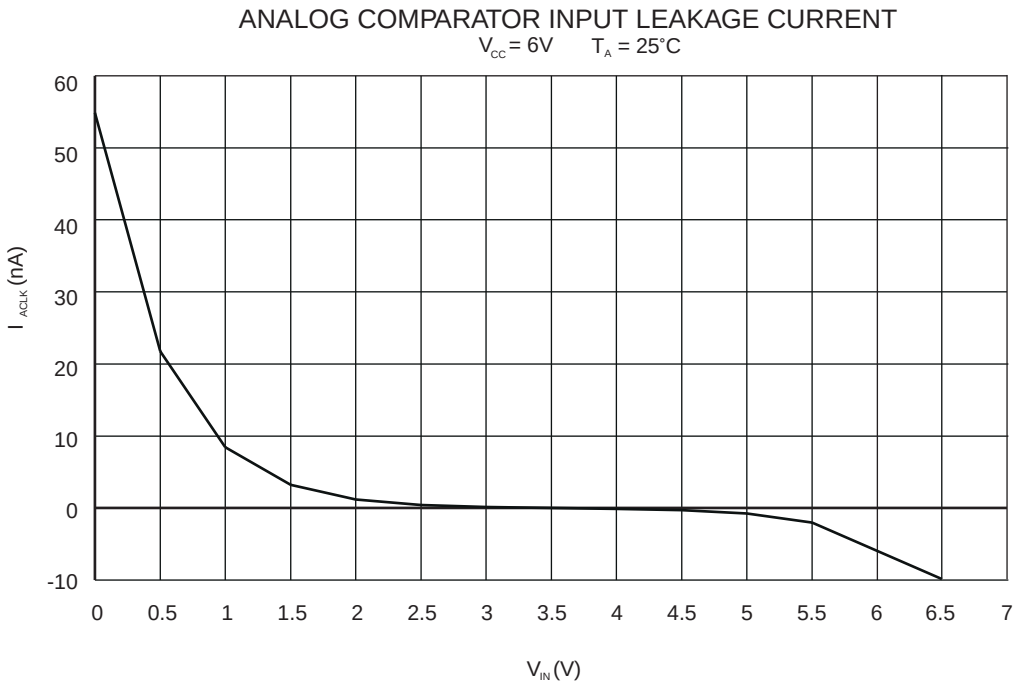


Figure 81. Watchdog Oscillator Frequency vs. V_{CC}

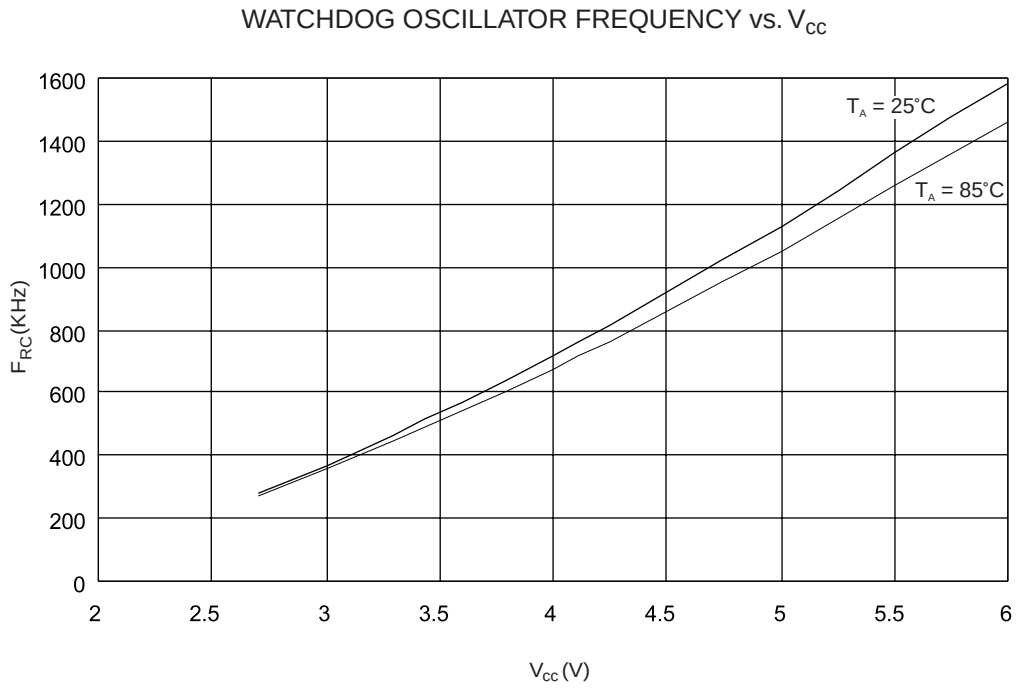


Figure 88. I/O Pin Input Threshold Voltage vs. V_{CC}

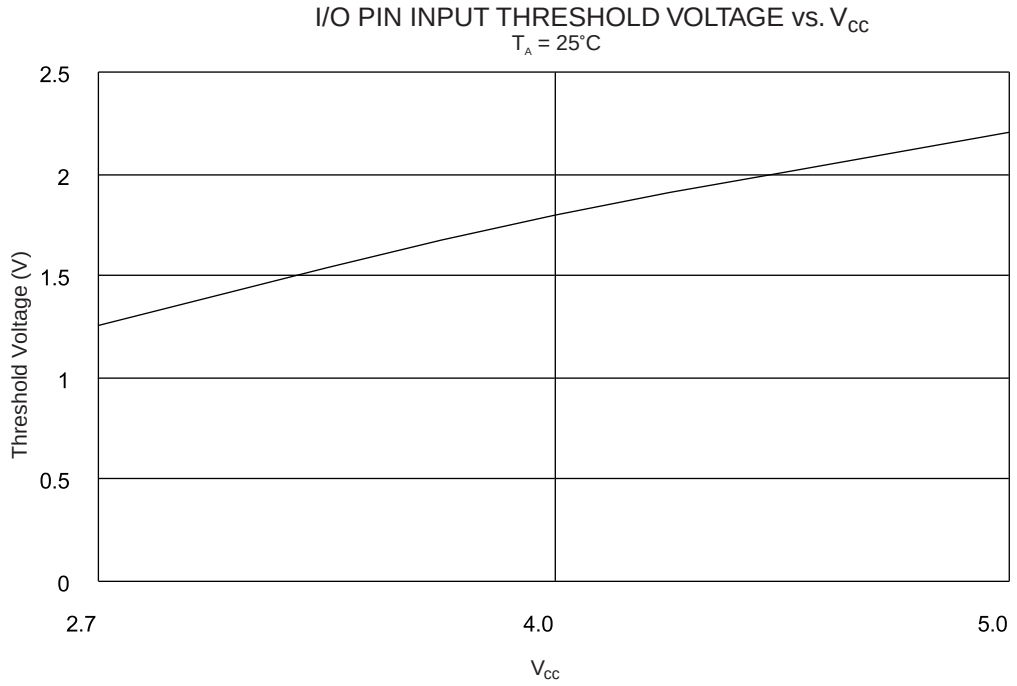
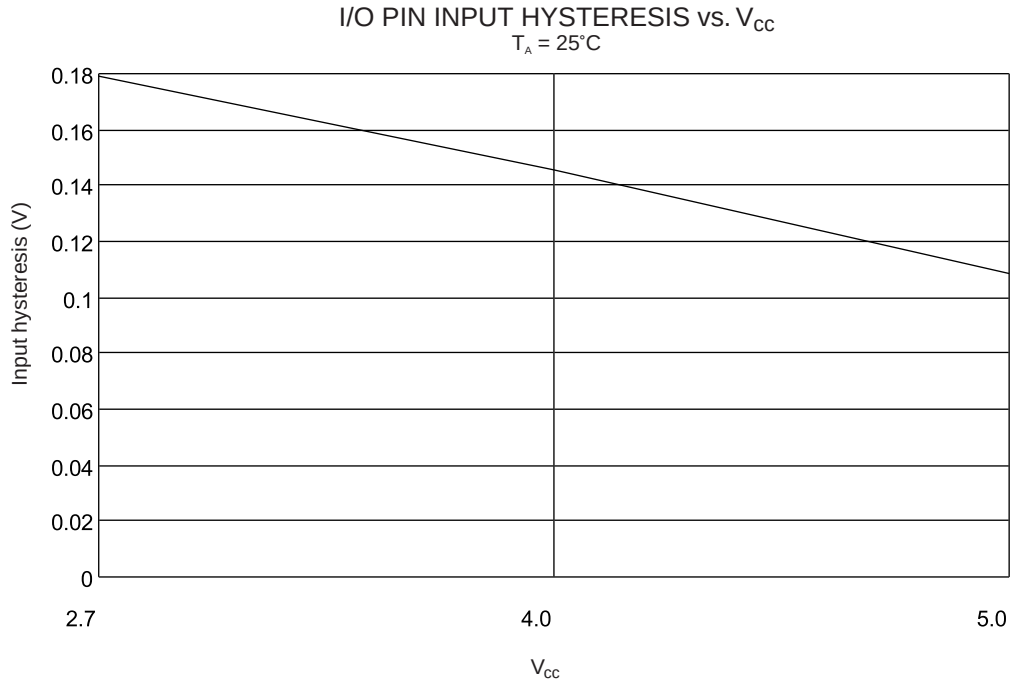


Figure 89. I/O Pin Input Hysteresis vs. V_{CC}



Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
$3F ($5F)	SREG	I	T	H	S	V	N	Z	C	page 17
$3E ($5E)	Reserved	-	-	-	-	-	-	-	-	page 17
$3D ($5D)	SP	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	page 17
$3C ($5C)	Reserved									
$3B ($5B)	GIMSK	INT1	INT0	-	-	-	-	-	-	page 23
$3A ($5A)	GIFR	INTF1	INTF0							page 24
$39 ($59)	TIMSK	TOIE1	OCIE1	-	-	TICIE1	-	TOIE0	-	page 24
$38 ($58)	TIFR	TOV1	OCF1	-	-	ICF1	-	TOV0	-	page 25
$37 ($57)	Reserved									
$36 ($56)	Reserved									
$35 ($55)	MCUCR	-		SE	SM	ISC11	ISC10	ISC01	ISC00	page 26
$34 ($54)	MCUSR	-	-	-	-	WDRF	BORF	EXTRF	PORF	page 22
$33 ($53)	TCCR0	-	-	-	-	-	CS02	CS01	CS00	page 29
$32 ($52)	TCNT0	Timer/Counter0 (8 Bits)								page 30
$31 ($51)	Reserved									
$30 ($50)	Reserved									
$2F ($4F)	TCCR1A	COM11	COM10	-	-	-	-	PWM11	PWM10	page 31
$2E ($4E)	TCCR1B	ICNC1	ICES1	-	-	CTC1	CS12	CS11	CS10	page 32
$2D ($4D)	TCNT1H	Timer/Counter1 - Counter Register High Byte								page 33
$2C ($4C)	TCNT1L	Timer/Counter1 - Counter Register Low Byte								page 33
$2B ($4B)	OCR1H	Timer/Counter1 - Output Compare Register High Byte								page 34
$2A ($4A)	OCR1L	Timer/Counter1 - Output Compare Register Low Byte								page 34
$29 ($49)	Reserved									
$28 ($48)	Reserved									
$27 ($47)	ICR1H	Timer/Counter1 - Input Capture Register High Byte								page 34
$26 ($46)	ICR1L	Timer/Counter1 - Input Capture Register Low Byte								page 34
$25 ($45)	Reserved									
$24 ($44)	Reserved									
$23 ($43)	Reserved									
$22 ($42)	Reserved									
$21 ($41)	WDTCR	-	-	-	WDTOE	WDE	WDP2	WDP1	WDP0	page 36
$20 ($40)	Reserved									
$1F ($3F)	Reserved									
$1E ($3E)	EEAR	EEPROM Address Register								page 38
$1D ($3D)	EEDR	EEPROM Data Register								page 38
$1C ($3C)	EECR	-	-	-	-	EERIE	EEMWE	EEWE	EERE	page 38
$1B ($3B)	Reserved									
$1A ($3A)	Reserved									
$19 ($39)	Reserved									
$18 ($38)	PORTB	-	-	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	page 59
$17 ($37)	DDRB	-	-	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	page 59
$16 ($36)	PINB	-	-	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	page 59
$15 ($35)	PORTC	-	-	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	page 64
$14 ($34)	DDRC	-	-	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	page 64
$13 ($33)	PINC	-	-	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	page 64
$12 ($32)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	page 66
$11 ($31)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	page 66
$10 ($30)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	page 66
$0F ($2F)	SPDR	SPI Data Register								page 43
$0E ($2E)	SPSR	SPIF	WCOL	-	-	-	-	-	-	page 43
$0D ($2D)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	page 42
$0C ($2C)	UDR	UART I/O Data Register								page 47
$0B ($2B)	UCSRA	RXC	TXC	UDRE	FE	OR	-	-	-	page 47
$0A ($2A)	UCSRB	RXCIE	TXCIE	UDRIE	RXEN	TXEN	CHR9	RXB8	TXB8	page 48
$09 ($29)	UBRR	UART Baud Rate Register								page 50
$08 ($28)	ACSR	ACD	AINBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	page 50
$07 ($27)	ADMUX	-	ADCBG	-	-	-	MUX2	MUX1	MUX0	page 55
$06 ($26)	ADCSR	ADEN	ADSC	ADFR	ADIF	ADIE	ADPS2	ADPS1	ADPS0	page 56
$05 ($25)	ADCH	-	-	-	-	-	-	ADC9	ADC8	page 57
$04 ($24)	ADCL	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	page 57
$03 ($23)	UBRRHI					UART Baud Rate Register High				page 50