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Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40/20MHz
Connectivity	UART/USART
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at87c54x2-slsum

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AT/TS8xC54/8X2

5. Pin Configuration



*NIC: No Internal Connection





Figure 6-2. Mode Switching Waveforms

The X2 bit in the CKCON register (See Table 6-1.) allows to switch from 12 clock cycles per instruction to 6 clock cycles and vice versa. At reset, the standard speed is activated (STD mode). Setting this bit activates the X2 feature (X2 mode).

CAUTION

In order to prevent any incorrect operation while operating in X2 mode, user must be aware that all peripherals using clock frequency as time reference (UART, timers) will have their time reference divided by two. For example a free running timer generating an interrupt every 20 ms will then generate an interrupt every 10 ms. UART with 4800 baud rate will have 9600 baud rate.





Table 6-1. CKCON Register CKCON - Clock Control Register (8Fh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	X2

Bit	Bit	
Number	Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
3	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
1	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
0	X2	CPU and peripheral clock bit Clear to select 12 clock periods per machine cycle (STD mode, $F_{OSC}=F_{XTAL}/2$). Set to select 6 clock periods per machine cycle (X2 mode, $F_{OSC}=F_{XTAL}$).

Reset Value = XXXX XXX0b Not bit addressable

For further details on the X2 feature, please refer to ANM072 available on the web (http://www.atmel.com)

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7. Dual Data Pointer Register Ddptr

The additional data pointer can be used to speed up code execution and reduce code size in a number of ways.

The dual DPTR structure is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called

DPS = AUXR1/bit0 (See Table 7-1.) that allows the program code to switch between them (Refer to Figure 7-1).



Figure 7-1. Use of Dual Pointer





Table 7-1.AUXR1: Auxiliary Register 1

7	6	5	4	3	2	1	0
-	-	-	-	GF3	0	-	DPS

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
3	GF3	This bit is a general purpose user flag
2	0	Reserved Always stuck at 0.
1	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
0	DPS	Data Pointer Selection Clear to select DPTR0. Set to select DPTR1.

Reset Value = XXXX 00X0 Not bit addressable

User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new feature. In that case, the reset value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

7.1 Application

Software can take advantage of the additional data pointers to both increase speed and reduce code size, for example, block operations (copy, compare, search ...) are well served by using one data pointer as a 'source' pointer and the other one as a "destination" pointer.

ASSEMBLY LANGUAGE

; Block move using ; Destroys DPTR0 ; note: DPS exits o	g dual data), DPTR1, A opposite of	pointers A and PSW entry state	
; unless an extra l	NC AUXR1	is added	
;			
00A2	AUXR	1 EQU 0A2H	
;			
0000 909000	MOV	DPTR,#SOURCE	; address of SOURCE
0003 05A2	INC	AUXR1	; switch data pointers
0005 90A000	MOV	DPTR,#DEST	; address of DEST
0008	LOOP		
0008 05A2	INC	AUXR1	; switch data pointers
000A E0	MOVX	A, @DPTR	; get a byte from SOURCE
000B A3	INC	DPTR	; increment SOURCE address
000C 05A2	INC	AUXR1	; switch data pointers
000E F0	MOVX	@DPTR,A	; write the byte to DEST
000F A3	INC	DPTR	; increment DEST address
0010 70F6	JNZ	LOOP	; check for 0 terminator
0012 05A2	INC	AUXR1	; (optional) restore DPS

INC is a short (2 bytes) and fast (12 clocks) way to manipulate the DPS bit in the AUXR1 SFR. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry. Observe that without the last instruction (INC AUXR1), the routine will exit with DPS in the opposite state.







8.1.1 Programmable Clock-Output

In the clock-out mode, timer 2 operates as a 50%-duty-cycle, programmable clock generator (See Figure 8-2) . The input clock increments TL2 at frequency $F_{OSC}/2$. The timer repeatedly counts to overflow from a loaded value. At overflow, the contents of RCAP2H and RCAP2L registers are loaded into TH2 and TL2. In this mode, timer 2 overflows do not generate interrupts. The formula gives the clock-out frequency as a function of the system oscillator frequency and the value in the RCAP2H and RCAP2L registers :

$$Clock - OutFrequency = \frac{F_{osc}}{4 \times (65536 - RCAP2H/RCAP2L)}$$

For a 16 MHz system clock, timer 2 has a programmable frequency range of 61 Hz $(F_{OSC}/2^{16})$ to 4 MHz $(F_{OSC}/4)$. The generated clock signal is brought out to T2 pin (P1.0).

Timer 2 is programmed for the clock-out mode as follows:

- Set T2OE bit in T2MOD register.
- Clear C/T2 bit in T2CON register.
- Determine the 16-bit reload value from the formula and enter it in RCAP2H/RCAP2L registers.



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Table 8-1.	T2CON Register
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T2CON - Timer 2 Control Register (C8h)

7	6	5	4	3	2	1	0
TF2	EXF2	RCLK	RCLK TCLK EXEN2 TR2 C/T2# CP/I				CP/RL2#
Bit Number	Bit Mnemonic			Descrip	otion		
7	TF2	Timer 2 overflow Must be cleared b Set by hardware c	r Flag by software. on timer 2 over	flow, if RCLK =	0 and TCLK =	0.	
6	EXF2	Timer 2 External F Set when a captur When set, causes enabled. Must be cleared b (DCEN = 1)	Flag re or a reload is the CPU to ve y software. EX	s caused by a n ctor to timer 2 ir F2 doesn't caus	egative transiti hterrupt routine se an interrupt i	on on T2EX pir when timer 2 i n Up/down cou	n if EXEN2=1. nterrupt is unter mode
5	RCLK	Receive Clock bit Clear to use timer Set to use timer 2	1 overflow as overflow as re	receive clock fo ceive clock for s	r serial port in serial port in mo	mode 1 or 3. ode 1 or 3.	
4	TCLK	Transmit Clock bit Clear to use timer Set to use timer 2	1 overflow as overflow as tra	transmit clock for	or serial port in serial port in m	mode 1 or 3. node 1 or 3.	
3	EXEN2	Timer 2 External Enable bit Clear to ignore events on T2EX pin for timer 2 operation. Set to cause a capture or reload when a negative transition on T2EX pin is detected, if timer 2 is not used to clock the serial port.					
2	TR2	Timer 2 Run contr Clear to turn off tir Set to turn on time	ol bit ner 2. er 2.				
1	C/T2#	Timer/Counter 2 select bit Clear for timer operation (input from internal clock system: F _{OSC}). Set for counter operation (input from T2 input pin, falling edge trigger). Must be 0 for clock out mode.				e 0 for clock	
0	CP/RL2#	Timer 2 Capture/F If RCLK=1 or TCL overflow. Clear to auto-reloa Set to capture on	Reload bit K=1, CP/RL2# ad on timer 2 o negative transi	is ignored and verflows or neg tions on T2EX p	timer is forced ative transition pin if EXEN2=1	to auto-reload s on T2EX pin	on timer 2 if EXEN2=1.

Reset Value = 0000 0000b Bit addressable





Table 8-2.	T2MOD Register	

T2MOD	- Timer 2	2 Mode	Control	Register	(C9h)
-------	-----------	--------	---------	----------	-------

7	6	5	4	3	2	1	0
-	-	-	-	-	-	T2OE	DCEN
Bit Number	Bit Mnemonic			Descrip	otion		
7	-	Reserved The value read	from this bit is in	determinate. Do	o not set this bit		
6	-	Reserved The value read	from this bit is in	determinate. Do	o not set this bit		
5	-	Reserved The value read	Reserved The value read from this bit is indeterminate. Do not set this bit.				
4	-	Reserved The value read	Reserved The value read from this bit is indeterminate. Do not set this bit.				
3	-	Reserved The value read	Reserved The value read from this bit is indeterminate. Do not set this bit.				
2	-	Reserved The value read	Reserved The value read from this bit is indeterminate. Do not set this bit.				
1	T2OE	Timer 2 Output Clear to progra Set to program	Fimer 2 Output Enable bit Clear to program P1.0/T2 as clock input or I/O port. Set to program P1.0/T2 as clock output.				
0	DCEN	Down Counter Clear to disable Set to enable ti	Jown Counter Enable bit Clear to disable timer 2 as up/down counter. Set to enable timer 2 as up/down counter.				

Reset Value = XXXX XX00b Not bit addressable

10. Interrupt System

The TS80C54/58X2 has a total of 7 interrupt vectors: two external interrupts (INT0 and INT1), three timer interrupts (timers 0, 1 and 2) and the serial port interrupt. These interrupts are shown in Figure 10-1.



Figure 10-1. Interrupt Control System

Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (See Table 10-2.). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one out of four priority levels by setting or clearing a bit in the Interrupt Priority register (See Table 10-3.) and in the Interrupt Priority High register (See Table 10-4.). shows the bit values and priority levels associated with each combination.

IPH.x	IP.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

Table 10-1. Priority Level Bit Values

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.





Table 10-4.	IPH Register

IPH - In	terrupt Priority	High Re	egister (B7h)	
	itoriaper nonty	1		

7	6		5	4	3	2	1	0
-	-		PT2H	PSH	PT1H	PX1H	PT0H	PX0H
Bit Number	Bit Mnemonic				Descrip	tion		
7	-	Reserve The value	ed ue read fr	om this bit is in	determinate. Do	o not set this bit		
6	-	Reserve The value	ed ue read fr	om this bit is in	determinate. Do	o not set this bit		
5	PT2H	Timer 2 <u>PT2H</u> 0 0 1 1	Timer 2 overflow interrupt Priority High bit PT2H PT2 Priority Level 0 0 Lowest 0 1 1 0 1 Highest					
4	PSH	Serial po <u>PSH</u> 0 1 1	ort Priority <u>PS P</u> 0 Lo 1 0 1 H	r High bit riority Level owest ighest				
3	PT1H	Timer 1 overflow interrupt Priority High bit PT1H PT1 Priority Level 0 0 Lowest 0 1 1 0 1 1						
2	PX1H	External <u>PX1H</u> 0 0 1 1	l interrupt <u>PX1</u> P 0 Lo 1 0 1 H	1 Priority High riority Level owest ighest	bit			
1	РТОН	Timer 0 <u>PT0H</u> 0 1 1	overflow i <u>PT0 P</u> 0 Lo 1 0 1 H	nterrupt Priority <u>riority Level</u> owest ighest	/ High bit			
0	РХОН	External <u>PX0H</u> 0 1 1	l interrupt <u>PX0 P</u> 0 Lo 1 0 1 H	0 Priority High <u>riority Level</u> owest ighest	bit			

Reset Value = XX00 0000b Not bit addressable



Figure 11-1. Power-Down Exit Waveform



Exit from power-down by reset redefines all the SFRs, exit from power-down by external interrupt does no affect the SFRs.

Exit from power-down by either reset or external interrupt does not affect the internal RAM content.

NOTE: If idle mode is activated with power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data*	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data*	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

 Table 11-1.
 The state of ports during idle and power-down modes

* Port 0 can force a "zero" level A "one" Level will leave port floating.



7	6		5	4	3 2 1		1	0	
T4	Т3		T2	T1	T0 S2 S1				
Bit Number	Bit Mnemonic	Description							
7	T4								
6	Т3								
5	T2	Reserve Do not	ved try to set o	or clear this bit					
4	T1								
3	Т0								
2	S2	WDT T	īme-out se	lect bit 2					
1	S1	WDT T	īme-out se	lect bit 1					
0	S0	WDT T	īme-out se	lect bit 0					
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$									

Table 12-2. WDTPRG Register WDTPRG Address (0A7h)

Reset value XXXX X000

12.1.1 WDT during Power Down and Idle

In Power Down mode the oscillator stops, which means the WDT also stops. While in Power Down mode the user does not need to service the WDT. There are 2 methods of exiting Power Down mode: by a hardware reset or via a level activated external interrupt which is enabled prior to entering Power Down mode. When Power Down is exited with hardware reset, servicing the WDT should occur as it normally should whenever the TS80C54/58X2 is reset. Exiting Power Down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service routine.

To ensure that the WDT does not overflow within a few states of exiting of powerdown, it is best to reset the WDT just before entering powerdown.

In the Idle mode, the oscillator continues to run. To prevent the WDT from resetting the TS80C54/58X2 while in Idle mode, the user should always set up a timer that will periodically exit Idle, service the WDT, and re-enter Idle mode.



14. Power-Off Flag

The power-off flag allows the user to distinguish between a "cold start" reset and a "warm start" reset.

A cold start reset is the one induced by V_{CC} switch-on. A warm start reset occurs while V_{CC} is still applied to the device and could be generated for example by an exit from power-down.

The power-off flag (POF) is located in PCON register (See Table 14-1.). POF is set by hardware when V_{CC} rises from 0 to its nominal voltage. The POF can be set or cleared by software allowing the user to determine the type of reset.

The POF value is only relevant with a Vcc range from 4.5V to 5.5V. For lower Vcc value, reading POF bit will return indeterminate value.

	6	5	4	3	2	1	0		
SMOD1	SMOD	00 - POF GF1 GF0 PD II							
Bit Number	Bit Mnemonic	Description							
7	SMOD1	Serial port M Set to select	o de bit 1 double baud rate i	n mode 1, 2 or :	3.				
6	SMOD0	Serial port M Clear to selec Set to to selec	Serial port Mode bit 0 Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.						
5	-	Reserved The value rea	d from this bit is in	determinate. Do	o not set this bit	i.			
4	POF	Power-Off Flag Clear to recognize next reset type. Set by hardware when V _{CC} rises from 0 to its nominal voltage. Can also be set by software.							
3	GF1	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.							
2	GF0	General purp Cleared by us Set by user fo	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.						
1	PD	Power-Down mode bit Cleared by hardware when reset occurs. Set to enter power-down mode.							
0	IDL	Idle mode bit Clear by hardware when interrupt or reset occurs. Set to enter idle mode.							

Table 14-1. PCON Register PCON - Power Control Register (87h)

Reset Value = 00X1 0000b Not bit addressable



The encryption array cannot be directly verified. Verification of the encryption array is done by observing that the code array is well encrypted.





17.4 EPROM Erasure (Windowed Packages Only)

Erasing the EPROM erases the code array, the encryption array and the lock bits returning the parts to full functionality.

Erasure leaves all the EPROM cells in a 1's state (FF).

17.4.1 Erasure Characteristics

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Å) to an integrated dose at least 15 W-sec/cm². Exposing the EPROM to an ultraviolet lamp of 12,000 μ W/cm² rating for 30 minutes, at a distance of about 25 mm, should be sufficient. An exposure of 1 hour is recommended with most of standard erasers.

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Å. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

18. Signature Bytes

The TS87C54/58X2 has four signature bytes in location 30h, 31h, 60h and 61h. To read these bytes follow the procedure for EPROM verify but activate the control lines provided in Table 31. for Read Signature Bytes. Table 18-1. shows the content of the signature byte for the TS80C54/58X2.



19. Electrical Characteristics

19.1 Absolute Maximum Ratings ⁽¹⁾

Ambiant Temperature Under Bias: C = commercial0°C to 70°C I = industrial -40°C to 85°C Storage Temperature-65°C to + 150°C Voltage on V_{CC} to V_{SS}-0.5 V to + 7 V Voltage on V_{PP} to V_{SS}-0.5 V to + 13 V Voltage on Any Pin to V_{SS}-0.5 V to V_{CC} + 0.5 V Power Dissipation1 W⁽²⁾

- 1. Stresses at or above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.
- 2. This value is based on the maximum allowable die temperature and the thermal resistance of the package.

19.2 Power consumption measurement

Since the introduction of the first C51 devices, every manufacturer made operating lcc measurements under reset, which made sense for the designs were the CPU was running under reset. In Atmel new devices, the CPU is no more active during reset, so the power consumption is very low but is not really representative of what will happen in the customer system. That's why, while keeping measurements under Reset, Atmel presents a new way to measure the operating lcc:

Using an internal test ROM, the following code is executed:

Label:

SJMP Label (80 FE)

Ports 1, 2, 3 are disconnected, Port 0 is tied to FFh, EA = Vcc, RST = Vss, XTAL2 is not connected and XTAL1 is driven by the clock.

This is much more representative of the real operating Icc.

19.3 DC Parameters for Standard Voltage

 $\begin{array}{l} T_{A}=0^{\circ}C \ to \ +70^{\circ}C; \ V_{SS}=0 \ V; \ V_{CC}=5 \ V \pm 10\%; \ F=0 \ to \ 40 \ MHz. \\ T_{A}=-40^{\circ}C \ to \ +85^{\circ}C; \ V_{SS}=0 \ V; \ V_{CC}=5 \ V \pm 10\%; \ F=0 \ to \ 40 \ MHz. \end{array}$

Table 19-1.	DC Parameters in Standard Voltage
-------------	-----------------------------------

Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
V _{IL}	Input Low Voltage	-0.5		0.2 V _{CC} - 0.1	V	
V _{IH}	Input High Voltage except XTAL1, RST	0.2 V _{CC} + 0.9		V _{CC} + 0.5	V	
V _{IH1}	Input High Voltage, XTAL1, RST	0.7 V _{CC}		V _{CC} + 0.5	V	
				0.3	V	$I_{OL} = 100 \ \mu A^{(4)}$
V _{OL}	Output Low Voltage, ports 1, 2, 3 ⁽⁶⁾			0.45	V	I _{OL} = 1.6 mA ⁽⁴⁾
				1.0	V	I _{OL} = 3.5 mA ⁽⁴⁾

- 5. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
- Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows: Maximum I_{OL} per port pin: 10 mA Maximum I_{OL} per 8-bit port: Port 0: 26 mA Ports 1, 2 and 3: 15 mA Maximum total I_{OL} for all output pins: 71 mA If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- 7. For other values, please contact your sales office.
- Operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH}, T_{CHCL} = 5 ns (see Figure 19-5.), V_{IL} = V_{SS} + 0.5 V,

 $V_{IH} = V_{CC} - 0.5V$; XTAL2 N.C.; $\overline{EA} = Port 0 = V_{CC}$; RST = V_{SS} . The internal ROM runs the code 80 FE (label: SJMP label). I_{CC} would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.





All other pins are disconnected.





All other pins are disconnected.







This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though ($T_A=25^{\circ}C$ fully loaded) RD and WR propagation delays are approximately 50ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.



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Part Number	Supply Voltage	Temperature Range	Package	Packing
TS87C58X2-MCE	5V ±10%	Commercial	VQFP44	Tray
TS87C58X2-VCA	5V ±10%	Commercial	PDIL40	Stick
TS87C58X2-VCB	5V ±10%	Commercial	Commercial PLCC44	
TS87C58X2-VCC	5V ±10%	Commercial	PQFP44	Tray
TS87C58X2-VCE	5V ±10%	Commercial	VQFP44	Tray
TS87C58X2-LCA	2.7 to 5.5V	Commercial	PDIL40	Stick
TS87C58X2-LCB	2.7 to 5.5V	Commercial	PLCC44	Stick
TS87C58X2-LCC	2.7 to 5.5V	Commercial	PQFP44	Tray
TS87C58X2-LCE	2.7 to 5.5V	Commercial	VQFP44	Tray
TS87C58X2-MIA	5V ±10%	Industrial	PDIL40	Stick
TS87C58X2-MIB	5V ±10%	Industrial	PLCC44	Stick
TS87C58X2-MIC	5V ±10%	Industrial	PQFP44	Tray
TS87C58X2-MIE	5V ±10%	Industrial	VQFP44	Tray
TS87C58X2-VIA	5V ±10%	Industrial	PDIL40	Stick
TS87C58X2-VIB	5V ±10%	Industrial	PLCC44	Stick
TS87C58X2-VIC	5V ±10%	Industrial	PQFP44	Tray
TS87C58X2-VIE	5V ±10%	Industrial	VQFP44	Tray
TS87C58X2-LIA	2.7 to 5.5V	Industrial	PDIL40	Stick
TS87C58X2-LIB	2.7 to 5.5V	Industrial	PLCC44	Stick
TS87C58X2-LIC	2.7 to 5.5V	Industrial	PQFP44	Tray
TS87C58X2-LIE	2.7 to 5.5V	Industrial	VQFP44	Tray
	·			
AT87C58X2-3CSUM	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUM	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUM	5V ±10%	Industrial & Green	VQFP44	Tray
AT87C58X2-3CSUL	2.7 to 5.5V	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUL	2.7 to 5.5V	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUL	2.7 to 5.5V	Industrial & Green	VQFP44	Tray
AT87C58X2-3CSUV	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUV	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUV	5V ±10%	Industrial & Green	VQFP44	Tray

21. Datasheet Revision History

21.1 Changes from Rev. C 01/01 to Rev. D 11/05

1. Added green product Ordering Information.

21.2 Changes from Rev. D 11/05 to Rev. E 04/06

1. Changed value of AUXR register.





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