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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	30/20MHz
Connectivity	UART/USART
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIL
Purchase URL	<a href="https://www.e-xfl.com/product-detail/atmel/at87c58x2-3csul">https://www.e-xfl.com/product-detail/atmel/at87c58x2-3csul</a>

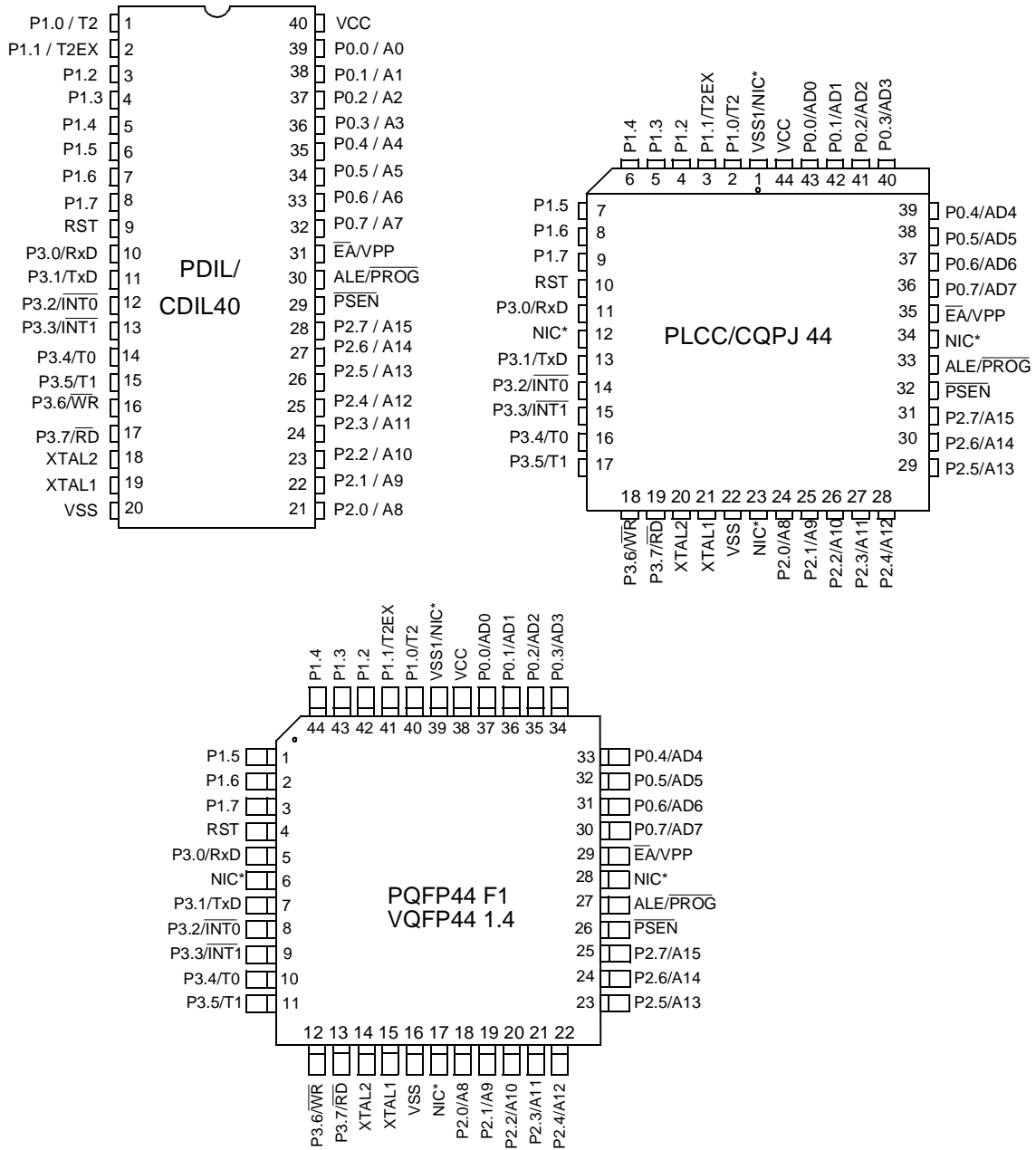


**Table 4-1.** All SFRs with their address and their reset value

	Bit addressable	Non Bit addressable							
		0/8	1/9	2/A	3/B	4/C	5/D	6/E	
F8h									FFh
F0h	B 0000 0000								F7h
E8h									EFh
E0h	ACC 0000 0000								E7h
D8h									DFh
D0h	PSW 0000 0000								D7h
C8h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			CFh
C0h									C7h
B8h	IP XX00 0000	SADEN 0000 0000							BFh
B0h	P3 1111 1111							IPH XX00 0000	B7h
A8h	IE 0X00 0000	SADDR 0000 0000							AFh
A0h	P2 1111 1111		AUXR1 XXXX 0XX0				WDTRST XXXX XXXX	WDTPRG XXXX X000	A7h
98h	SCON 0000 0000	SBUF XXXX XXXX							9Fh
90h	P1 1111 1111								97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XXXX XXX0	CKCON XXXX XXX0	8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00X1 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

reserved

## 5. Pin Configuration



\*NIC: No Internal Connection

## 6. TS80C54/58X2 Enhanced Features

In comparison to the original 80C52, the TS80C54/58X2 implements some new features, which are:

- The X2 option.
- The Dual Data Pointer.
- The Watchdog.
- The 4 level interrupt priority system.
- The power-off flag.
- The ONCE mode.
- The ALE disabling.
- Some enhanced features are also located in the UART and the timer 2.

### 6.1 X2 Feature

The TS80C54/58X2 core needs only 6 clock periods per machine cycle. This feature called "X2" provides the following advantages:

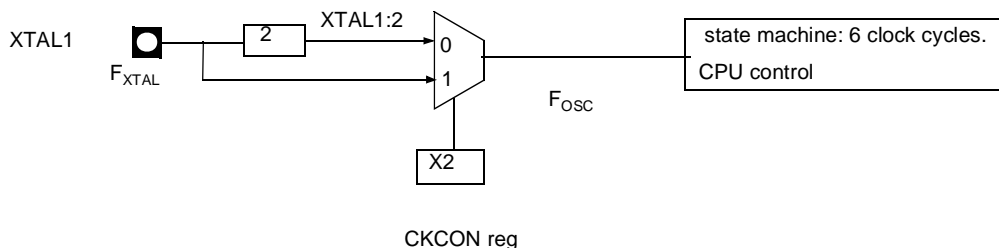
- Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power.
- Save power consumption while keeping same CPU power (oscillator power saving).
- Save power consumption by dividing dynamically operating frequency by 2 in operating and idle modes.
- Increase CPU power by 2 while keeping same crystal frequency.

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

#### 6.1.1 Description

The clock for the whole circuit and peripheral is first divided by two before being used by the CPU core and peripherals. This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%. Figure 6-2. shows the clock generation block diagram. X2 bit is validated on XTAL1÷2 rising edge to avoid glitches when switching from X2 to STD mode. Figure 6-2. shows the mode switching waveforms.

**Figure 6-1.** Clock Generation Diagram



**Table 6-1.** CKCON Register  
CKCON - Clock Control Register (8Fh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	X2

Bit Number	Bit Mnemonic	Description
7	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
4	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
3	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
2	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
1	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
0	X2	<b>CPU and peripheral clock bit</b> Clear to select 12 clock periods per machine cycle (STD mode, $F_{OSC}=F_{XTAL}/2$ ). Set to select 6 clock periods per machine cycle (X2 mode, $F_{OSC}=F_{XTAL}$ ).

Reset Value = XXXX XXX0b

Not bit addressable

For further details on the X2 feature, please refer to ANM072 available on the web (<http://www.atmel.com>)

## 7.1 Application

Software can take advantage of the additional data pointers to both increase speed and reduce code size, for example, block operations (copy, compare, search ...) are well served by using one data pointer as a 'source' pointer and the other one as a "destination" pointer.

### ASSEMBLY LANGUAGE

```

; Block move using dual data pointers
; Destroys DPTR0, DPTR1, A and PSW
; note: DPS exits opposite of entry state
; unless an extra INC AUXR1 is added
;
00A2          AUXR1 EQU 0A2H
;
0000 909000   MOV  DPTR,#SOURCE      ; address of SOURCE
0003 05A2     INC  AUXR1          ; switch data pointers
0005 90A000   MOV  DPTR,#DEST      ; address of DEST
0008          LOOP:
0008 05A2     INC  AUXR1          ; switch data pointers
000A E0       MOVX A,@DPTR       ; get a byte from SOURCE
000B A3       INC  DPTR          ; increment SOURCE address
000C 05A2     INC  AUXR1          ; switch data pointers
000E F0       MOVX @DPTR,A       ; write the byte to DEST
000F A3       INC  DPTR          ; increment DEST address
0010 70F6     JNZ  LOOP          ; check for 0 terminator
0012 05A2     INC  AUXR1          ; (optional) restore DPS

```

INC is a short (2 bytes) and fast (12 clocks) way to manipulate the DPS bit in the AUXR1 SFR. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry. Observe that without the last instruction (INC AUXR1), the routine will exit with DPS in the opposite state.



**Table 8-1.** T2CON Register  
T2CON - Timer 2 Control Register (C8h)

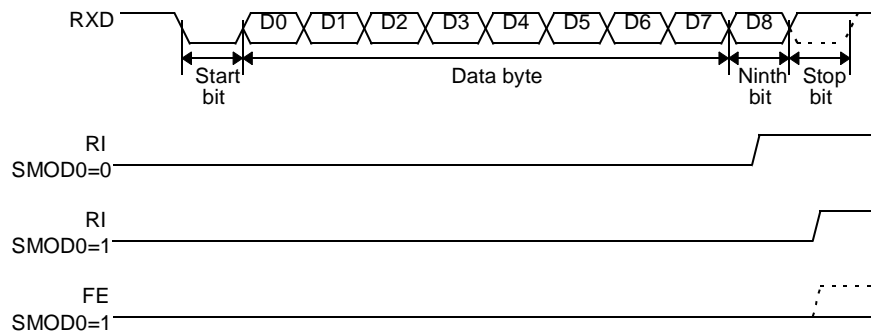
7	6	5	4	3	2	1	0
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#
Bit Number	Bit Mnemonic	Description					
7	TF2	<b>Timer 2 overflow Flag</b> Must be cleared by software. Set by hardware on timer 2 overflow, if RCLK = 0 and TCLK = 0.					
6	EXF2	Timer 2 External Flag Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. When set, causes the CPU to vector to timer 2 interrupt routine when timer 2 interrupt is enabled. Must be cleared by software. EXF2 doesn't cause an interrupt in Up/down counter mode (DCEN = 1)					
5	RCLK	Receive Clock bit Clear to use timer 1 overflow as receive clock for serial port in mode 1 or 3. Set to use timer 2 overflow as receive clock for serial port in mode 1 or 3.					
4	TCLK	Transmit Clock bit Clear to use timer 1 overflow as transmit clock for serial port in mode 1 or 3. Set to use timer 2 overflow as transmit clock for serial port in mode 1 or 3.					
3	EXEN2	Timer 2 External Enable bit Clear to ignore events on T2EX pin for timer 2 operation. Set to cause a capture or reload when a negative transition on T2EX pin is detected, if timer 2 is not used to clock the serial port.					
2	TR2	Timer 2 Run control bit Clear to turn off timer 2. Set to turn on timer 2.					
1	C/T2#	<b>Timer/Counter 2 select bit</b> Clear for timer operation (input from internal clock system: F <sub>OSC</sub> ). Set for counter operation (input from T2 input pin, falling edge trigger). Must be 0 for clock out mode.					
0	CP/RL2#	Timer 2 Capture/Reload bit If RCLK=1 or TCLK=1, CP/RL2# is ignored and timer is forced to auto-reload on timer 2 overflow. Clear to auto-reload on timer 2 overflows or negative transitions on T2EX pin if EXEN2=1. Set to capture on negative transitions on T2EX pin if EXEN2=1.					

Reset Value = 0000 0000b

Bit addressable



**Figure 9-3.** UART Timings in Modes 2 and 3



### 9.1.1 Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.

To support automatic address recognition, a device is identified by a given address and a broadcast address.

**NOTE:** The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).

### 9.1.2 Given Address

Each device has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don't-care bits (defined by zeros) to form the device's given address. The don't-care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed.

To address a device by its individual address, the SADEN mask byte must be 1111 1111b.

For example:

SADDR	0101 0110b
SADEN	1111 1100b
Given	0101 01XXb



The following is an example of how to use given addresses to address different slaves:

Slave A:	SADDR	1111 0001b
	<u>SADEN</u>	<u>1111 1010b</u>
	Given	1111 0X0Xb
Slave B:	SADDR	1111 0011b
	<u>SADEN</u>	<u>1111 1001b</u>
	Given	1111 0XX1b
Slave C:	SADDR	1111 0010b
	<u>SADEN</u>	<u>1111 1101b</u>
	Given	1111 00X1b

The SADEN byte is selected so that each slave may be addressed separately.

For slave A, bit 0 (the LSB) is a don't-care bit; for slaves B and C, bit 0 is a 1. To communicate with slave A only, the master must send an address where bit 0 is clear (e.g. 1111 0000b).

For slave A, bit 1 is a 1; for slaves B and C, bit 1 is a don't care bit. To communicate with slaves B and C, but not slave A, the master must send an address with bits 0 and 1 both set (e.g. 1111 0011b).

To communicate with slaves A, B and C, the master must send an address with bit 0 set, bit 1 clear, and bit 2 clear (e.g. 1111 0001b).

### 9.1.3 Broadcast Address

A broadcast address is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't-care bits, e.g.:

	SADDR	0101 0110b
	SADEN	1111 1100b
Broadcast =SADDR OR SADEN		1111 111Xb

The use of don't-care bits provides flexibility in defining the broadcast address, however in most applications, a broadcast address is FFh. The following is an example of using broadcast addresses:

Slave A:	SADDR	1111 0001b
	<u>SADEN</u>	<u>1111 1010b</u>
	Broadcast	1111 1X11b,
Slave B:	SADDR	1111 0011b
	<u>SADEN</u>	<u>1111 1001b</u>
	Broadcast	1111 1X11b,
Slave C:	SADDR=	1111 0010b
	<u>SADEN</u>	<u>1111 1101b</u>
	Broadcast	1111 1111b

For slaves A and B, bit 2 is a don't care bit; for slave C, bit 2 is set. To communicate with all of the slaves, the master must send an address FFh. To communicate with slaves A and B, but not slave C, the master can send an address FBh.

### 9.1.4 Reset Addresses

On reset, the SADDR and SADEN registers are initialized to 00h, i.e. the given and broadcast addresses are XXXX XXXXb (all don't-care bits). This ensures that the serial port will reply to any address, and so, that it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

**Table 10-2.** IE Register  
IE - Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	-	ET2	ES	ET1	EX1	ET0	EX0

Bit Number	Bit Mnemonic	Description
7	EA	Enable All interrupt bit Clear to disable all interrupts. Set to enable all interrupts. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its own interrupt enable bit.
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
5	ET2	Timer 2 overflow interrupt Enable bit Clear to disable timer 2 overflow interrupt. Set to enable timer 2 overflow interrupt.
4	ES	Serial port Enable bit Clear to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	Timer 1 overflow interrupt Enable bit Clear to disable timer 1 overflow interrupt. Set to enable timer 1 overflow interrupt.
2	EX1	External interrupt 1 Enable bit Clear to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	Timer 0 overflow interrupt Enable bit Clear to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.
0	EX0	External interrupt 0 Enable bit Clear to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0X00 0000b

Bit addressable

**Table 10-3.** IP Register  
IP - Interrupt Priority Register (B8h)

7	6	5	4	3	2	1	0
-	-	PT2	PS	PT1	PX1	PT0	PX0

Bit Number	Bit Mnemonic	Description
7	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
5	PT2	<b>Timer 2 overflow interrupt Priority bit</b> Refer to PT2H for priority level.
4	PS	<b>Serial port Priority bit</b> Refer to PSH for priority level.
3	PT1	<b>Timer 1 overflow interrupt Priority bit</b> Refer to PT1H for priority level.
2	PX1	<b>External interrupt 1 Priority bit</b> Refer to PX1H for priority level.
1	PT0	<b>Timer 0 overflow interrupt Priority bit</b> Refer to PT0H for priority level.
0	PX0	<b>External interrupt 0 Priority bit</b> Refer to PX0H for priority level.

Reset Value = XX00 0000b

Bit addressable

**Table 12-2.** WDTPRG Register  
WDTPRG Address (0A7h)

7	6	5	4	3	2	1	0
T4	T3	T2	T1	T0	S2	S1	S0
Bit Number	Bit Mnemonic	Description					
7	T4	<b>Reserved</b> Do not try to set or clear this bit.					
6	T3						
5	T2						
4	T1						
3	T0						
2	S2	WDT Time-out select bit 2					
1	S1	WDT Time-out select bit 1					
0	S0	WDT Time-out select bit 0					
		<u>S2S1</u>	<u>S0</u>	<u>Selected Time-out</u>			
		0	0	0	(2 <sup>14</sup> - 1) machine cycles, 16.3 ms @ 12 MHz		
		0	0	1	(2 <sup>15</sup> - 1) machine cycles, 32.7 ms @ 12 MHz		
		0	1	0	(2 <sup>16</sup> - 1) machine cycles, 65.5 ms @ 12 MHz		
		0	1	1	(2 <sup>17</sup> - 1) machine cycles, 131 ms @ 12 MHz		
		1	0	0	(2 <sup>18</sup> - 1) machine cycles, 262 ms @ 12 MHz		
		1	0	1	(2 <sup>19</sup> - 1) machine cycles, 542 ms @ 12 MHz		
		1	1	0	(2 <sup>20</sup> - 1) machine cycles, 1.05 s @ 12 MHz		
		1	1	1	(2 <sup>21</sup> - 1) machine cycles, 2.09 s @ 12 MHz		

Reset value XXXX X000

### 12.1.1 WDT during Power Down and Idle

In Power Down mode the oscillator stops, which means the WDT also stops. While in Power Down mode the user does not need to service the WDT. There are 2 methods of exiting Power Down mode: by a hardware reset or via a level activated external interrupt which is enabled prior to entering Power Down mode. When Power Down is exited with hardware reset, servicing the WDT should occur as it normally should whenever the TS80C54/58X2 is reset. Exiting Power Down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service routine.

To ensure that the WDT does not overflow within a few states of exiting of powerdown, it is best to reset the WDT just before entering powerdown.

In the Idle mode, the oscillator continues to run. To prevent the WDT from resetting the TS80C54/58X2 while in Idle mode, the user should always set up a timer that will periodically exit Idle, service the WDT, and re-enter Idle mode.

## 16. TS80C54/58X2 ROM

### 16.1 ROM Structure

The TS80C54/58X2 ROM memory is in three different arrays:

- the code array:16/32 Kbytes.
- the encryption array:64 bytes.
- the signature array:4 bytes.

### 16.2 ROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

#### 16.2.1 Encryption Array

Within the ROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

#### 16.2.2 Program Lock Bits

The lock bits when programmed according to Table 16-1. will provide different level of protection for the on-chip code and data.

**Table 16-1.** Program Lock bits

Program Lock Bits				Protection Description
Security level	LB1	LB2	LB3	
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data.
2	P	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset.

U: unprogrammed  
P: programmed

#### 16.2.3 Signature bytes

The TS80C54/58X2 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in section 8.3.

#### 16.2.4 Verify Algorithm

Refer to 17.3.4

### 17.2.3 Signature bytes

The TS87C54/58X2 contains 4 factory programmed signature bytes. To read these bytes, perform the process described in section 8.3.

## 17.3 EPROM Programming

### 17.3.1 Set-up modes

In order to program and verify the EPROM or to read the signature bytes, the TS87C54/58X2 is placed in specific set-up modes (See Figure 17-1.).

Control and program signals must be held at the levels indicated in Table 17-2.

### 17.3.2 Definition of terms








**Address Lines:**P1.0-P1.7, P2.0-P2.5, P3.4 respectively for A0-A14 (P2.5 (A13) for TS87C54X2, P3.4 (A14) for TS87C58X2).

**Data Lines:**P0.0-P0.7 for D0-D7

**Control Signals:**RST,  $\overline{\text{PSEN}}$ , P2.6, P2.7, P3.3, P3.6, P3.7.

**Program Signals:**ALE/ $\overline{\text{PROG}}$ ,  $\overline{\text{EA}}$ / $\overline{\text{VPP}}$ .

**Table 17-2.** EPROM Set-Up Modes

Mode	RST	PSEN	ALE/ $\overline{\text{PROG}}$	$\overline{\text{EA}}$ / $\overline{\text{VPP}}$	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code data	1	0		12.75	0	1	1	1	1
Verify Code data	1	0	1	1	0		0	1	1
Program Encryption Array Address 0-3Fh	1	0		12.75	0	1	1	0	1
Read Signature Bytes	1	0	1	1	0		0	0	0
Program Lock bit 1	1	0		12.75	1	1	1	1	1
Program Lock bit 2	1	0		12.75	1	1	1	0	0
Program Lock bit 3	1	0		12.75	1	0	1	1	0

## 19.4 DC Parameters for Low Voltage

$T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ;  $V_{SS} = 0\text{ V}$ ;  $V_{CC} = 2.7\text{ V}$  to  $5.5\text{ V} \pm 10\%$ ;  $F = 0$  to  $30\text{ MHz}$ .

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ;  $V_{SS} = 0\text{ V}$ ;  $V_{CC} = 2.7\text{ V}$  to  $5.5\text{ V} \pm 10\%$ ;  $F = 0$  to  $30\text{ MHz}$ .

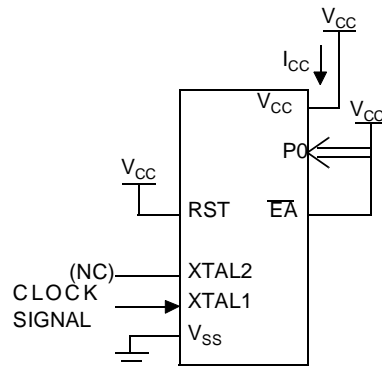
**Table 19-2.** DC Parameters for Low Voltage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$V_{IL}$	Input Low Voltage	-0.5		$0.2 V_{CC} - 0.1$	V	
$V_{IH}$	Input High Voltage except XTAL1, RST	$0.2 V_{CC} + 0.9$		$V_{CC} + 0.5$	V	
$V_{IH1}$	Input High Voltage, XTAL1, RST	$0.7 V_{CC}$		$V_{CC} + 0.5$	V	
$V_{OL}$	Output Low Voltage, ports 1, 2, 3 <sup>(6)</sup>			0.45	V	$I_{OL} = 0.8\text{ mA}^{(4)}$
$V_{OL1}$	Output Low Voltage, port 0, ALE, $\overline{\text{PSEN}}$ <sup>(6)</sup>			0.45	V	$I_{OL} = 1.6\text{ mA}^{(4)}$
$V_{OH}$	Output High Voltage, ports 1, 2, 3	$0.9 V_{CC}$			V	$I_{OH} = -10\text{ }\mu\text{A}$
$V_{OH1}$	Output High Voltage, port 0, ALE, $\overline{\text{PSEN}}$	$0.9 V_{CC}$			V	$I_{OH} = -40\text{ }\mu\text{A}$
$I_{IL}$	Logical 0 Input Current ports 1, 2 and 3			-50	$\mu\text{A}$	$V_{in} = 0.45\text{ V}$
$I_{LI}$	Input Leakage Current			$\pm 10$	$\mu\text{A}$	$0.45\text{ V} < V_{in} < V_{CC}$
$I_{TL}$	Logical 1 to 0 Transition Current, ports 1, 2, 3			-650	$\mu\text{A}$	$V_{in} = 2.0\text{ V}$
$R_{RST}$	RST Pulldown Resistor	50	90 <sup>(5)</sup>	200	k $\Omega$	
C <sub>IO</sub>	Capacitance of I/O Buffer			10	pF	$F_c = 1\text{ MHz}$ $T_A = 25^\circ\text{C}$
$I_{PD}$	Power Down Current		20 <sup>(5)</sup> 10 <sup>(5)</sup>	50 30	$\mu\text{A}$	$V_{CC} = 2.0\text{ V}$ to $5.5\text{ V}^{(3)}$ $V_{CC} = 2.0\text{ V}$ to $3.3\text{ V}^{(3)}$
$I_{CC}$ under RESET	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			1 + 0.2 Freq (MHz) @12MHz 3.4 @16MHz 4.2	mA	$V_{CC} = 3.3\text{ V}^{(1)}$
$I_{CC}$ operating	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			1 + 0.3 Freq (MHz) @12MHz 4.6 @16MHz 5.8	mA	$V_{CC} = 3.3\text{ V}^{(8)}$
$I_{CC}$ idle	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			0.15 Freq (MHz) + 0.2 @12MHz 2 @16MHz 2.6	mA	$V_{CC} = 3.3\text{ V}^{(2)}$

- $I_{CC}$  under reset is measured with all output pins disconnected; XTAL1 driven with  $T_{CLCH}$ ,  $T_{CHCL} = 5\text{ ns}$  (see Figure 19-5.),  $V_{IL} = V_{SS} + 0.5\text{ V}$ ,  $V_{IH} = V_{CC} - 0.5\text{ V}$ ; XTAL2 N.C.;  $\overline{\text{EA}} = \text{RST} = \text{Port } 0 = V_{CC}$ .  $I_{CC}$  would be slightly higher if a crystal oscillator used..
- Idle  $I_{CC}$  is measured with all output pins disconnected; XTAL1 driven with  $T_{CLCH}$ ,  $T_{CHCL} = 5\text{ ns}$ ,  $V_{IL} = V_{SS} + 0.5\text{ V}$ ,  $V_{IH} = V_{CC} - 0.5\text{ V}$ ; XTAL2 N.C; Port 0 =  $V_{CC}$ ;  $\overline{\text{EA}} = \text{RST} = V_{SS}$  (see Figure 19-3.).
- Power Down  $I_{CC}$  is measured with all output pins disconnected;  $\overline{\text{EA}} = V_{SS}$ , PORT 0 =  $V_{CC}$ ; XTAL2 NC.; RST =  $V_{SS}$  (see Figure 19-4.).
- Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the  $V_{OL}$ s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100pF), the noise pulse on the ALE line may exceed 0.45V with maxi  $V_{OL}$  peak 0.6V. A Schmitt Trigger use is not necessary.

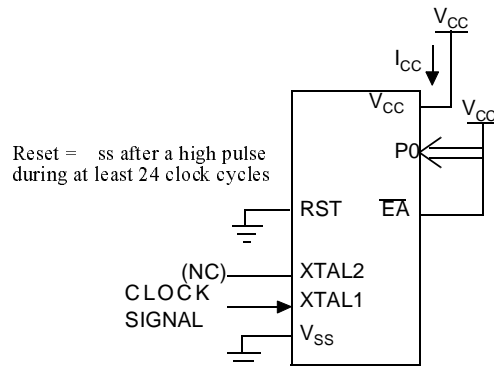
5. Typical values are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
6. Under steady state (non-transient) conditions,  $I_{OL}$  must be externally limited as follows:
  - Maximum  $I_{OL}$  per port pin: 10 mA
  - Maximum  $I_{OL}$  per 8-bit port:
    - Port 0: 26 mA
    - Ports 1, 2 and 3: 15 mA
  - Maximum total  $I_{OL}$  for all output pins: 71 mA
 If  $I_{OL}$  exceeds the test condition,  $V_{OL}$  may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
7. For other values, please contact your sales office.
8. Operating  $I_{CC}$  is measured with all output pins disconnected; XTAL1 driven with  $T_{CLCH}$ ,  $T_{CHCL} = 5$  ns (see Figure 19-5.),  $V_{IL} = V_{SS} + 0.5$  V,  $V_{IH} = V_{CC} - 0.5$  V; XTAL2 N.C.;  $\overline{EA} = \text{Port 0} = V_{CC}$ ;  $\text{RST} = V_{SS}$ . The internal ROM runs the code 80 FE (label: SJMP label).  $I_{CC}$  would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.

**Figure 19-1.**  $I_{CC}$  Test Condition, under reset



All other pins are disconnected.

**Figure 19-2.** Operating  $I_{CC}$  Test Condition



All other pins are disconnected.

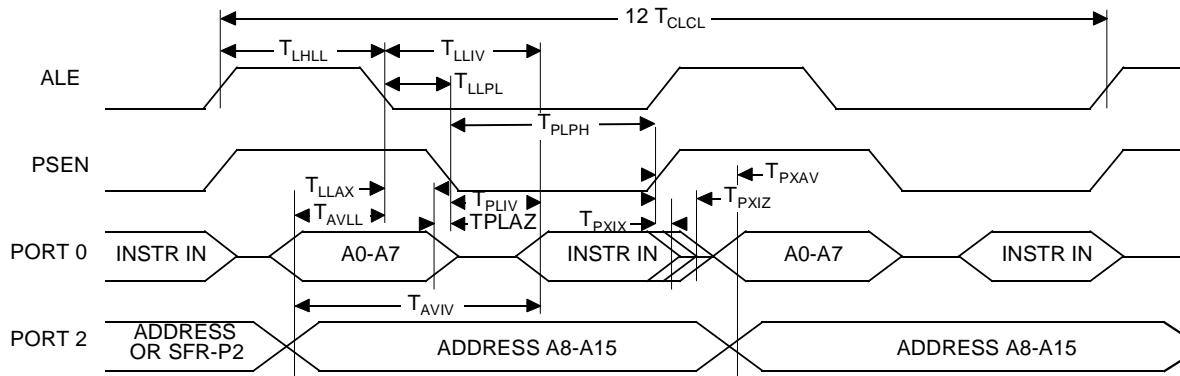


**Table 19-7.** AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
$T_{LHLL}$	Min	$2 T - x$	$T - x$	10	8	15	ns
$T_{AVLL}$	Min	$T - x$	$0.5 T - x$	15	13	20	ns
$T_{LLAX}$	Min	$T - x$	$0.5 T - x$	15	13	20	ns
$T_{LLIV}$	Max	$4 T - x$	$2 T - x$	30	22	35	ns
$T_{LLPL}$	Min	$T - x$	$0.5 T - x$	10	8	15	ns
$T_{PLPH}$	Min	$3 T - x$	$1.5 T - x$	20	15	25	ns
$T_{PLIV}$	Max	$3 T - x$	$1.5 T - x$	40	25	45	ns
$T_{PXIX}$	Min	x	x	0	0	0	ns
$T_{PXIZ}$	Max	$T - x$	$0.5 T - x$	7	5	15	ns
$T_{AVIV}$	Max	$5 T - x$	$2.5 T - x$	40	30	45	ns
$T_{PLAZ}$	Max	x	x	10	10	10	ns

### 19.5.3 External Program Memory Read Cycle

**Figure 19-6.** External Program Memory Read Cycle

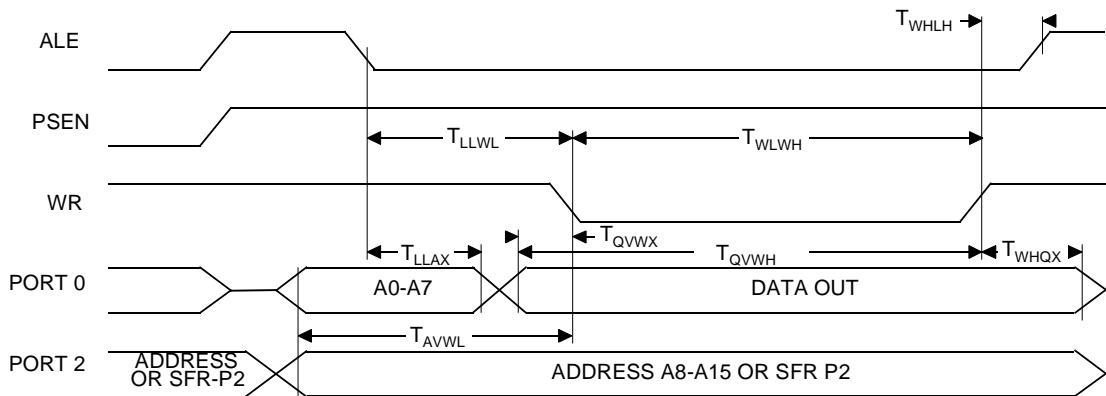


**Table 19-10.** AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
$T_{RLRH}$	Min	6 T - x	3 T - x	20	15	25	ns
$T_{WLWH}$	Min	6 T - x	3 T - x	20	15	25	ns
$T_{RLDV}$	Max	5 T - x	2.5 T - x	25	23	30	ns
$T_{RHDZ}$	Max	2 T - x	T - x	20	15	25	ns
$T_{RLDX}$	Min	x	x	0	0	0	ns
$T_{RLDZ}$	Max	2 T - x	T - x	20	15	25	ns
$T_{LLDV}$	Max	8 T - x	4T -x	40	35	45	ns
$T_{AVDV}$	Max	9 T - x	4.5 T - x	60	50	65	ns
$T_{LLWL}$	Min	3 T - x	1.5 T - x	25	20	30	ns
$T_{LLWL}$	Max	3 T + x	1.5 T + x	25	20	30	ns
$T_{AVWL}$	Min	4 T - x	2 T - x	25	20	30	ns
$T_{QVWX}$	Min	T - x	0.5 T - x	15	10	20	ns
$T_{QVWH}$	Min	7 T - x	3.5 T - x	15	10	20	ns
$T_{WHQX}$	Min	T - x	0.5 T - x	10	8	15	ns
$T_{RLAZ}$	Max	x	x	0	0	0	ns
$T_{WHLH}$	Min	T - x	0.5 T - x	15	10	20	ns
$T_{WHLH}$	Max	T + x	0.5 T + x	15	10	20	ns

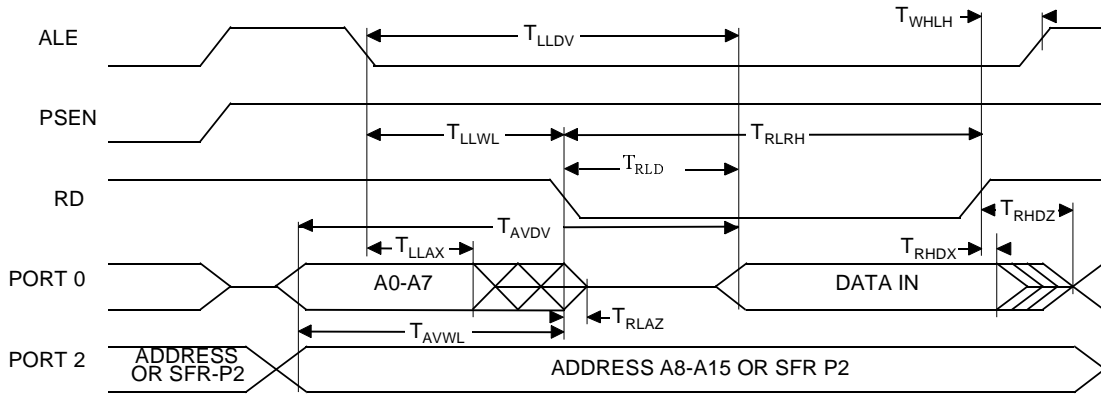
**19.5.5 External Data Memory Write Cycle**

**Figure 19-7.** External Data Memory Write Cycle



### 19.5.6 External Data Memory Read Cycle

Figure 19-8. External Data Memory Read Cycle



### 19.5.7 Serial Port Timing - Shift Register Mode

Table 19-11. Symbol Description

Symbol	Parameter
$T_{XLXL}$	Serial port clock cycle time
$T_{QVHX}$	Output data set-up to clock rising edge
$T_{XHGX}$	Output data hold after clock rising edge
$T_{XHDX}$	Input data hold after clock rising edge
$T_{XHDX}$	Clock rising edge to input data valid

Table 19-12. AC Parameters for a Fix Clock

Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$T_{XLXL}$	300		200		300		300		400		ns
$T_{QVHX}$	200		117		200		200		283		ns
$T_{XHGX}$	30		13		30		30		47		ns
$T_{XHDX}$	0		0		0		0		0		ns
$T_{XHDX}$		117		34		117		117		200	ns

Part Number	Supply Voltage	Temperature Range	Package	Packing
TS87C54X2-MCC	5V ±10%	Commercial	PQFP44	Tray
TS87C54X2-MCE	5V ±10%	Commercial	VQFP44	Tray
TS87C54X2-VCA	5V ±10%	Commercial	PDIL40	Stick
TS87C54X2-VCB	5V ±10%	Commercial	PLCC44	Stick
TS87C54X2-VCC	5V ±10%	Commercial	PQFP44	Tray
TS87C54X2-VCE	5V ±10%	Commercial	VQFP44	Tray
TS87C54X2-LCA	2.7 to 5.5V	Commercial	PDIL40	Stick
TS87C54X2-LCB	2.7 to 5.5V	Commercial	PLCC44	Stick
TS87C54X2-LCC	2.7 to 5.5V	Commercial	PQFP44	Tray
TS87C54X2-LCE	2.7 to 5.5V	Commercial	VQFP44	Tray
TS87C54X2-MIA	5V ±10%	Industrial	PDIL40	Stick
TS87C54X2-MIB	5V ±10%	Industrial	PLCC44	Stick
TS87C54X2-MIC	5V ±10%	Industrial	PQFP44	Tray
TS87C54X2-MIE	5V ±10%	Industrial	VQFP44	Tray
TS87C54X2-VIA	5V ±10%	Industrial	PDIL40	Stick
TS87C54X2-VIB	5V ±10%	Industrial	PLCC44	Stick
TS87C54X2-VIC	5V ±10%	Industrial	PQFP44	Tray
TS87C54X2-VIE	5V ±10%	Industrial	VQFP44	Tray
TS87C54X2-LIA	2.7 to 5.5V	Industrial	PDIL40	Stick
TS87C54X2-LIB	2.7 to 5.5V	Industrial	PLCC44	Stick
TS87C54X2-LIC	2.7 to 5.5V	Industrial	PQFP44	Tray
TS87C54X2-LIE	2.7 to 5.5V	Industrial	VQFP44	Tray
AT87C54X2-3CSUM	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C54X2-SLSUM	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C54X2-RLTUM	5V ±10%	Industrial & Green	VQFP44	Tray
AT87C54X2-3CSUL	2.7 to 5.5V	Industrial & Green	PDIL40	Stick
AT87C54X2-SLSUL	2.7 to 5.5V	Industrial & Green	PLCC44	Stick
AT87C54X2-RLTUL	2.7 to 5.5V	Industrial & Green	VQFP44	Tray
AT87C54X2-3CSUV	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C54X2-SLSUV	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C54X2-RLTUV	5V ±10%	Industrial & Green	VQFP44	Tray

Part Number	Supply Voltage	Temperature Range	Package	Packing
TS87C58X2-MCE	5V ±10%	Commercial	VQFP44	Tray
TS87C58X2-VCA	5V ±10%	Commercial	PDIL40	Stick
TS87C58X2-VCB	5V ±10%	Commercial	PLCC44	Stick
TS87C58X2-VCC	5V ±10%	Commercial	PQFP44	Tray
TS87C58X2-VCE	5V ±10%	Commercial	VQFP44	Tray
TS87C58X2-LCA	2.7 to 5.5V	Commercial	PDIL40	Stick
TS87C58X2-LCB	2.7 to 5.5V	Commercial	PLCC44	Stick
TS87C58X2-LCC	2.7 to 5.5V	Commercial	PQFP44	Tray
TS87C58X2-LCE	2.7 to 5.5V	Commercial	VQFP44	Tray
TS87C58X2-MIA	5V ±10%	Industrial	PDIL40	Stick
TS87C58X2-MIB	5V ±10%	Industrial	PLCC44	Stick
TS87C58X2-MIC	5V ±10%	Industrial	PQFP44	Tray
TS87C58X2-MIE	5V ±10%	Industrial	VQFP44	Tray
TS87C58X2-VIA	5V ±10%	Industrial	PDIL40	Stick
TS87C58X2-VIB	5V ±10%	Industrial	PLCC44	Stick
TS87C58X2-VIC	5V ±10%	Industrial	PQFP44	Tray
TS87C58X2-VIE	5V ±10%	Industrial	VQFP44	Tray
TS87C58X2-LIA	2.7 to 5.5V	Industrial	PDIL40	Stick
TS87C58X2-LIB	2.7 to 5.5V	Industrial	PLCC44	Stick
TS87C58X2-LIC	2.7 to 5.5V	Industrial	PQFP44	Tray
TS87C58X2-LIE	2.7 to 5.5V	Industrial	VQFP44	Tray
AT87C58X2-3CSUM	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUM	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUM	5V ±10%	Industrial & Green	VQFP44	Tray
AT87C58X2-3CSUL	2.7 to 5.5V	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUL	2.7 to 5.5V	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUL	2.7 to 5.5V	Industrial & Green	VQFP44	Tray
AT87C58X2-3CSUV	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUV	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUV	5V ±10%	Industrial & Green	VQFP44	Tray

## 21. Datasheet Revision History

### 21.1 Changes from Rev. C 01/01 to Rev. D 11/05

1. Added green product Ordering Information.

### 21.2 Changes from Rev. D 11/05 to Rev. E 04/06

1. Changed value of AUXR register.