



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

|                            |                                                                                                                                     |
|----------------------------|-------------------------------------------------------------------------------------------------------------------------------------|
| Product Status             | Obsolete                                                                                                                            |
| Core Processor             | 80C51                                                                                                                               |
| Core Size                  | 8-Bit                                                                                                                               |
| Speed                      | 40/20MHz                                                                                                                            |
| Connectivity               | UART/USART                                                                                                                          |
| Peripherals                | POR, WDT                                                                                                                            |
| Number of I/O              | 32                                                                                                                                  |
| Program Memory Size        | 32KB (32K x 8)                                                                                                                      |
| Program Memory Type        | OTP                                                                                                                                 |
| EEPROM Size                | -                                                                                                                                   |
| RAM Size                   | 256 x 8                                                                                                                             |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V                                                                                                                         |
| Data Converters            | -                                                                                                                                   |
| Oscillator Type            | Internal                                                                                                                            |
| Operating Temperature      | -40°C ~ 85°C (TA)                                                                                                                   |
| Mounting Type              | Surface Mount                                                                                                                       |
| Package / Case             | 44-LQFP                                                                                                                             |
| Supplier Device Package    | 44-VQFP (10x10)                                                                                                                     |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/atmel/at87c58x2-rltum">https://www.e-xfl.com/product-detail/atmel/at87c58x2-rltum</a> |

**Table 4-1.** All SFRs with their address and their reset value

|     | Bit<br>address-<br>able | Non Bit addressable |                     |                     |                  |                  |                     |                     |     |
|-----|-------------------------|---------------------|---------------------|---------------------|------------------|------------------|---------------------|---------------------|-----|
|     | 0/8                     | 1/9                 | 2/A                 | 3/B                 | 4/C              | 5/D              | 6/E                 | 7/F                 |     |
| F8h |                         |                     |                     |                     |                  |                  |                     |                     | FFh |
| F0h | B<br>0000 0000          |                     |                     |                     |                  |                  |                     |                     | F7h |
| E8h |                         |                     |                     |                     |                  |                  |                     |                     | EFh |
| E0h | ACC<br>0000 0000        |                     |                     |                     |                  |                  |                     |                     | E7h |
| D8h |                         |                     |                     |                     |                  |                  |                     |                     | DFh |
| D0h | PSW<br>0000 0000        |                     |                     |                     |                  |                  |                     |                     | D7h |
| C8h | T2CON<br>0000 0000      | T2MOD<br>XXXX XX00  | RCAP2L<br>0000 0000 | RCAP2H<br>0000 0000 | TL2<br>0000 0000 | TH2<br>0000 0000 |                     |                     | CFh |
| C0h |                         |                     |                     |                     |                  |                  |                     |                     | C7h |
| B8h | IP<br>XX00 0000         | SADEN<br>0000 0000  |                     |                     |                  |                  |                     |                     | BFh |
| B0h | P3<br>1111 1111         |                     |                     |                     |                  |                  |                     | IPH<br>XX00 0000    | B7h |
| A8h | IE<br>0X00 0000         | SADDR<br>0000 0000  |                     |                     |                  |                  |                     |                     | AFh |
| A0h | P2<br>1111 1111         |                     | AUXR1<br>XXXX 0XX0  |                     |                  |                  | WDTRST<br>XXXX XXXX | WDTPRG<br>XXXX X000 | A7h |
| 98h | SCON<br>0000 0000       | SBUF<br>XXXX XXXX   |                     |                     |                  |                  |                     |                     | 9Fh |
| 90h | P1<br>1111 1111         |                     |                     |                     |                  |                  |                     |                     | 97h |
| 88h | TCON<br>0000 0000       | TMOD<br>0000 0000   | TL0<br>0000 0000    | TL1<br>0000 0000    | TH0<br>0000 0000 | TH1<br>0000 0000 | AUXR<br>XXXX XXX0   | CKCON<br>XXXX XXX0  | 8Fh |
| 80h | P0<br>1111 1111         | SP<br>0000 0111     | DPL<br>0000 0000    | DPH<br>0000 0000    |                  |                  |                     | PCON<br>00X1 0000   | 87h |
|     | 0/8                     | 1/9                 | 2/A                 | 3/B                 | 4/C              | 5/D              | 6/E                 | 7/F                 |     |

reserved

**Table 5-1.** Pin Description for 40/44 pin packages

| MNEMONIC         | PIN NUMBER |              |              | TYPE | Name And Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------------------|------------|--------------|--------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  | DIL        | LCC          | VQFP 1.4     |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| V <sub>SS</sub>  | 20         | 22           | 16           | I    | <b>Ground:</b> 0V reference                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| V <sub>SS1</sub> |            | 1            | 39           | I    | Optional Ground: <b>Contact the Sales Office for ground connection.</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| V <sub>CC</sub>  | 40         | 44           | 38           | I    | <b>Power Supply:</b> This is the power supply voltage for normal, idle and power-down operation                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| P0.0-P0.7        | 39-32      | 43-36        | 37-30        | I/O  | <b>Port 0:</b> Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. Port 0 pins must be polarized to V <sub>CC</sub> or V <sub>SS</sub> in order to prevent any parasitic current consumption. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-up when emitting 1s. Port 0 also inputs the code bytes during EPROM programming. External pull-ups are required during program verification during which P0 outputs the code bytes.                                                                                                                                                                |
|                  |            |              |              |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| P1.0-P1.7        | 1-8        | 2-9          | 40-44<br>1-3 | I/O  | <b>Port 1:</b> Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups. Port 1 also receives the low-order address byte during memory programming and verification.<br>Alternate functions for Port 1 include:                                                                                                                                                                                                                                                                                                                                                          |
|                  |            |              |              |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|                  | 1          | 2            | 40           | I/O  | <b>T2 (P1.0):</b> Timer/Counter 2 external count input/Clockout                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|                  | 2          | 3            | 41           | I    | <b>T2EX (P1.1):</b> Timer/Counter 2 Reload/Capture/Direction Control                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| P2.0-P2.7        | 21-28      | 24-31        | 18-25        | I/O  | <b>Port 2:</b> Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 emits the contents of the P2 SFR. Some Port 2 pins receive the high order address bits during EPROM programming and verification:<br>P2.0 to P2.5 for A8 to A13 |
|                  |            |              |              |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| P3.0-P3.7        | 10-17      | 11,<br>13-19 | 5,<br>7-13   | I/O  | <b>Port 3:</b> Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Some Port 3 pin P3.4 receive the high order address bits during EPROM programming and verification for TS8xC58X2 devices.<br>Port 3 also serves the special features of the 80C51 family, as listed below.                                                                                                                                                                                                                                                                                      |
|                  |            |              |              |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|                  | 10         | 11           | 5            | I    | <b>RXD (P3.0):</b> Serial input port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|                  | 11         | 13           | 7            | O    | <b>TXD (P3.1):</b> Serial output port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|                  | 12         | 14           | 8            | I    | <b>INT0 (P3.2):</b> External interrupt 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|                  | 13         | 15           | 9            | I    | <b>INT1 (P3.3):</b> External interrupt 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|                  | 14         | 16           | 10           | I    | <b>T0 (P3.4):</b> Timer 0 external input                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|                  | 15         | 17           | 11           | I    | <b>T1 (P3.5):</b> Timer 1 external input                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|                  | 16         | 18           | 12           | O    | <b>WR (P3.6):</b> External data memory write strobe                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|                  | 17         | 19           | 13           | O    | <b>RD (P3.7):</b> External data memory read strobe<br>P3.4 also receives A14 during TS87C58X2 EPROM Programming.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| Reset            | 9          | 10           | 4            | I    | <b>Reset:</b> A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V <sub>SS</sub> permits a power-on reset using only an external capacitor to V <sub>CC</sub> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|                  |            |              |              |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

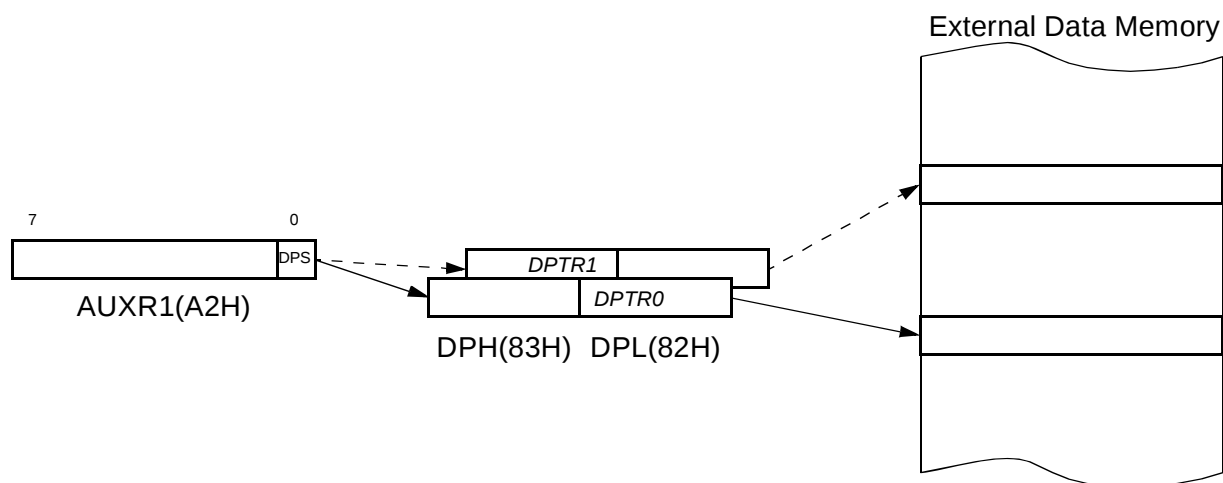
## 7. Dual Data Pointer Register Ddptr

The additional data pointer can be used to speed up code execution and reduce code size in a number of ways.

The dual DPTR structure is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called

DPS = AUXR1/bit0 (See Table 7-1.) that allows the program code to switch between them (Refer to Figure 7-1).

**Figure 7-1.** Use of Dual Pointer



**Table 7-1.** AUXR1: Auxiliary Register 1

| 7 | 6 | 5 | 4 | 3   | 2 | 1 | 0   |
|---|---|---|---|-----|---|---|-----|
| - | - | - | - | GF3 | 0 | - | DPS |

| Bit Number | Bit Mnemonic | Description                                                                            |
|------------|--------------|----------------------------------------------------------------------------------------|
| 7          | -            | <b>Reserved</b><br>The value read from this bit is indeterminate. Do not set this bit. |
| 6          | -            | <b>Reserved</b><br>The value read from this bit is indeterminate. Do not set this bit. |
| 5          | -            | <b>Reserved</b><br>The value read from this bit is indeterminate. Do not set this bit. |
| 4          | -            | <b>Reserved</b><br>The value read from this bit is indeterminate. Do not set this bit. |
| 3          | GF3          | This bit is a general purpose user flag                                                |
| 2          | 0            | <b>Reserved</b><br>Always stuck at 0.                                                  |
| 1          | -            | <b>Reserved</b><br>The value read from this bit is indeterminate. Do not set this bit. |
| 0          | DPS          | <b>Data Pointer Selection</b><br>Clear to select DPTR0.<br>Set to select DPTR1.        |

Reset Value = XXXX 00X0

Not bit addressable

User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new feature. In that case, the reset value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

## 8. Timer 2

The timer 2 in the TS80C54/58X2 is compatible with the timer 2 in the 80C52.

It is a 16-bit timer/counter: the count is maintained by two eight-bit timer registers, TH2 and TL2, connected in cascade. It is controlled by T2CON register (See Table 8-1) and T2MOD register (See Table 8-2). Timer 2 operation is similar to Timer 0 and Timer 1.  $\overline{C/T2}$  selects  $F_{OSC}/12$  (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows TL2 to be incremented by the selected input.

Timer 2 has 3 operating modes: capture, autoreload and Baud Rate Generator. These modes are selected by the combination of RCLK, TCLK and CP/RL2 (T2CON), as described in the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description.

Refer to the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description for the description of Capture and Baud Rate Generator Modes.

In TS80C54/58X2 Timer 2 includes the following enhancements:

- Auto-reload mode with up or down counter
- Programmable clock-output

### 8.1 Auto-Reload Mode

The auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. If DCEN bit in T2MOD is cleared, timer 2 behaves as in 80C52 (refer to the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description). If DCEN bit is set, timer 2 acts as an Up/down timer/counter as shown in Figure 8-1. In this mode the T2EX pin controls the direction of count.

When T2EX is high, timer 2 counts up. Timer overflow occurs at FFFFh which sets the TF2 flag and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L registers to be loaded into the timer registers TH2 and TL2.

When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers TH2 and TL2 equals the value stored in RCAP2H and RCAP2L registers. The underflow sets TF2 flag and reloads FFFFh into the timer registers.

The EXF2 bit toggles when timer 2 overflows or underflows according to the the direction of the count. EXF2 does not generate any interrupt. This bit can be used to provide 17-bit resolution

**Table 8-2.** T2MOD Register  
T2MOD - Timer 2 Mode Control Register (C9h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1    | 0    |
|---|---|---|---|---|---|------|------|
| - | - | - | - | - | - | T2OE | DCEN |

| Bit Number | Bit Mnemonic | Description                                                                                                                         |
|------------|--------------|-------------------------------------------------------------------------------------------------------------------------------------|
| 7          | -            | <b>Reserved</b><br>The value read from this bit is indeterminate. Do not set this bit.                                              |
| 6          | -            | <b>Reserved</b><br>The value read from this bit is indeterminate. Do not set this bit.                                              |
| 5          | -            | <b>Reserved</b><br>The value read from this bit is indeterminate. Do not set this bit.                                              |
| 4          | -            | <b>Reserved</b><br>The value read from this bit is indeterminate. Do not set this bit.                                              |
| 3          | -            | <b>Reserved</b><br>The value read from this bit is indeterminate. Do not set this bit.                                              |
| 2          | -            | <b>Reserved</b><br>The value read from this bit is indeterminate. Do not set this bit.                                              |
| 1          | T2OE         | <b>Timer 2 Output Enable bit</b><br>Clear to program P1.0/T2 as clock input or I/O port.<br>Set to program P1.0/T2 as clock output. |
| 0          | DCEN         | <b>Down Counter Enable bit</b><br>Clear to disable timer 2 as up/down counter.<br>Set to enable timer 2 as up/down counter.         |

Reset Value = XXXX XX00b

Not bit addressable

The following is an example of how to use given addresses to address different slaves:

|          |              |                   |
|----------|--------------|-------------------|
| Slave A: | SADDR        | 1111 0001b        |
|          | <u>SADEN</u> | <u>1111 1010b</u> |
|          | Given        | 1111 0X0Xb        |
| Slave B: | SADDR        | 1111 0011b        |
|          | <u>SADEN</u> | <u>1111 1001b</u> |
|          | Given        | 1111 0XX1b        |
| Slave C: | SADDR        | 1111 0010b        |
|          | <u>SADEN</u> | <u>1111 1101b</u> |
|          | Given        | 1111 00X1b        |

The SADEN byte is selected so that each slave may be addressed separately.

For slave A, bit 0 (the LSB) is a don't-care bit; for slaves B and C, bit 0 is a 1. To communicate with slave A only, the master must send an address where bit 0 is clear (e.g. 1111 0000b).

For slave A, bit 1 is a 1; for slaves B and C, bit 1 is a don't care bit. To communicate with slaves B and C, but not slave A, the master must send an address with bits 0 and 1 both set (e.g. 1111 0011b).

To communicate with slaves A, B and C, the master must send an address with bit 0 set, bit 1 clear, and bit 2 clear (e.g. 1111 0001b).

### 9.1.3 Broadcast Address

A broadcast address is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't-care bits, e.g.:

|                           |       |            |
|---------------------------|-------|------------|
|                           | SADDR | 0101 0110b |
|                           | SADEN | 1111 1100b |
| Broadcast =SADDR OR SADEN |       | 1111 111Xb |

The use of don't-care bits provides flexibility in defining the broadcast address, however in most applications, a broadcast address is FFh. The following is an example of using broadcast addresses:

|          |              |                   |
|----------|--------------|-------------------|
| Slave A: | SADDR        | 1111 0001b        |
|          | <u>SADEN</u> | <u>1111 1010b</u> |
|          | Broadcast    | 1111 1X11b,       |
| Slave B: | SADDR        | 1111 0011b        |
|          | <u>SADEN</u> | <u>1111 1001b</u> |
|          | Broadcast    | 1111 1X11b,       |
| Slave C: | SADDR=       | 1111 0010b        |
|          | <u>SADEN</u> | <u>1111 1101b</u> |
|          | Broadcast    | 1111 1111b        |

For slaves A and B, bit 2 is a don't care bit; for slave C, bit 2 is set. To communicate with all of the slaves, the master must send an address FFh. To communicate with slaves A and B, but not slave C, the master can send an address FBh.

### 9.1.4 Reset Addresses

On reset, the SADDR and SADEN registers are initialized to 00h, i.e. the given and broadcast addresses are xxxx xxxxb (all don't-care bits). This ensures that the serial port will reply to any address, and so, that it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition.

**Table 9-4.** PCON Register

**Table 9-5.** PCON - Power Control Register (87h)

|       |       |   |     |     |     |    |     |
|-------|-------|---|-----|-----|-----|----|-----|
| 7     | 6     | 5 | 4   | 3   | 2   | 1  | 0   |
| SMOD1 | SMOD0 | - | POF | GF1 | GF0 | PD | IDL |

| Bit Number | Bit Mnemonic | Description                                                                                                                                                |
|------------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7          | SMOD1        | <b>Serial port Mode bit 1</b><br>Set to select double baud rate in mode 1, 2 or 3.                                                                         |
| 6          | SMOD0        | <b>Serial port Mode bit 0</b><br>Clear to select SM0 bit in SCON register.<br>Set to to select FE bit in SCON register.                                    |
| 5          | -            | <b>Reserved</b><br>The value read from this bit is indeterminate. Do not set this bit.                                                                     |
| 4          | POF          | <b>Power-Off Flag</b><br>Clear to recognize next reset type.<br>Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software. |
| 3          | GF1          | <b>General purpose Flag</b><br>Cleared by user for general purpose usage.<br>Set by user for general purpose usage.                                        |
| 2          | GF0          | <b>General purpose Flag</b><br>Cleared by user for general purpose usage.<br>Set by user for general purpose usage.                                        |
| 1          | PD           | <b>Power-Down mode bit</b><br>Cleared by hardware when reset occurs.<br>Set to enter power-down mode.                                                      |
| 0          | IDL          | <b>Idle mode bit</b><br>Clear by hardware when interrupt or reset occurs.<br>Set to enter idle mode.                                                       |

Reset Value = 00X1 0000b

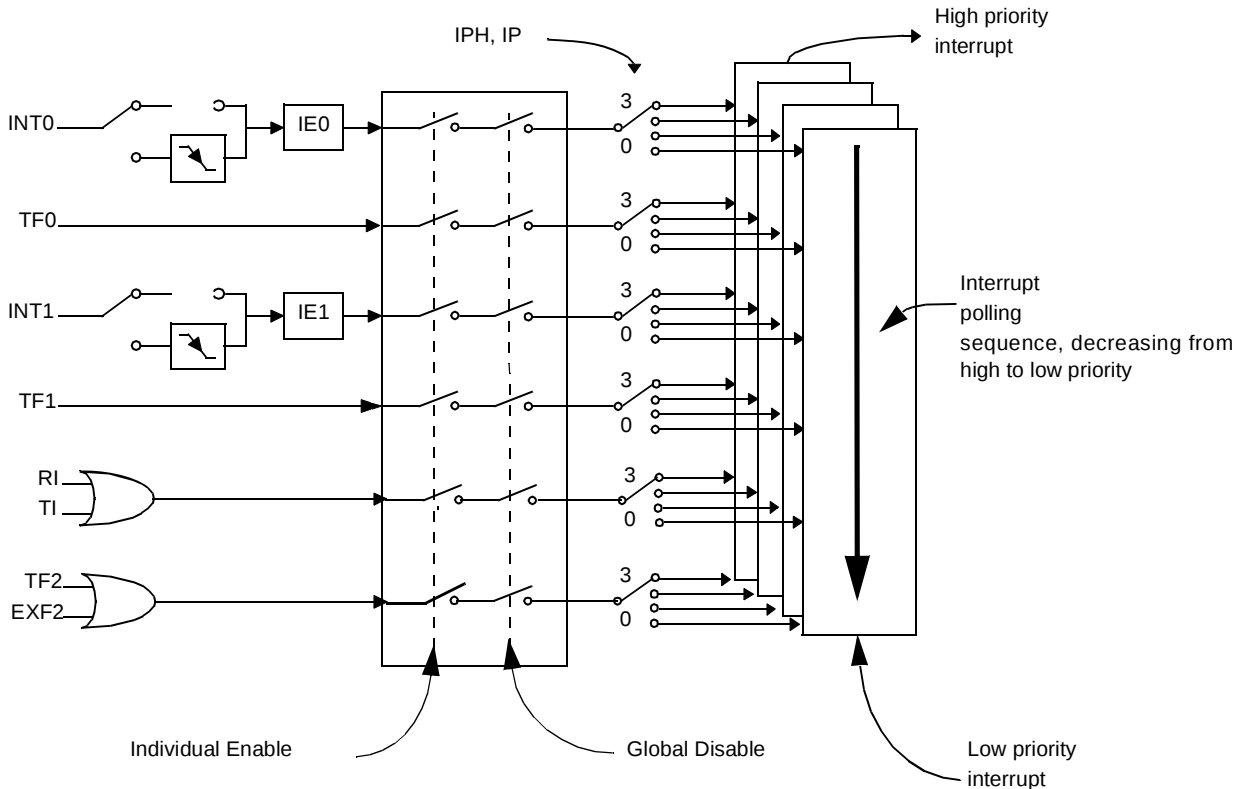
Not bit addressable

Power-off flag reset value will be 1 only after a power on (cold reset). A warm reset doesn't affect the value of this bit.

## 10. Interrupt System

The TS80C54/58X2 has a total of 7 interrupt vectors: two external interrupts ( $\overline{\text{INT0}}$  and  $\overline{\text{INT1}}$ ), three timer interrupts (timers 0, 1 and 2) and the serial port interrupt. These interrupts are shown in Figure 10-1.

**Figure 10-1.** Interrupt Control System



Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (See Table 10-2.). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one out of four priority levels by setting or clearing a bit in the Interrupt Priority register (See Table 10-3.) and in the Interrupt Priority High register (See Table 10-4.). shows the bit values and priority levels associated with each combination.

**Table 10-1.** Priority Level Bit Values

| IPH.x | IP.x | Interrupt Level Priority |
|-------|------|--------------------------|
| 0     | 0    | 0 (Lowest)               |
| 0     | 1    | 1                        |
| 1     | 0    | 2                        |
| 1     | 1    | 3 (Highest)              |

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

**Table 10-3.** IP Register  
IP - Interrupt Priority Register (B8h)

| 7 | 6 | 5   | 4  | 3   | 2   | 1   | 0   |
|---|---|-----|----|-----|-----|-----|-----|
| - | - | PT2 | PS | PT1 | PX1 | PT0 | PX0 |

| Bit Number | Bit Mnemonic | Description                                                                            |
|------------|--------------|----------------------------------------------------------------------------------------|
| 7          | -            | <b>Reserved</b><br>The value read from this bit is indeterminate. Do not set this bit. |
| 6          | -            | <b>Reserved</b><br>The value read from this bit is indeterminate. Do not set this bit. |
| 5          | PT2          | <b>Timer 2 overflow interrupt Priority bit</b><br>Refer to PT2H for priority level.    |
| 4          | PS           | <b>Serial port Priority bit</b><br>Refer to PSH for priority level.                    |
| 3          | PT1          | <b>Timer 1 overflow interrupt Priority bit</b><br>Refer to PT1H for priority level.    |
| 2          | PX1          | <b>External interrupt 1 Priority bit</b><br>Refer to PX1H for priority level.          |
| 1          | PT0          | <b>Timer 0 overflow interrupt Priority bit</b><br>Refer to PT0H for priority level.    |
| 0          | PX0          | <b>External interrupt 0 Priority bit</b><br>Refer to PX0H for priority level.          |

Reset Value = XX00 0000b

Bit addressable

**Table 10-4.** IPH Register  
IPH - Interrupt Priority High Register (B7h)

| 7 | 6 | 5    | 4   | 3    | 2    | 1    | 0    |
|---|---|------|-----|------|------|------|------|
| - | - | PT2H | PSH | PT1H | PX1H | PT0H | PX0H |

| Bit Number  | Bit Mnemonic | Description                                                                                                                                                                                                                                                                                                                   |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
|-------------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|------------|-----------------------|---|---|--------|---|---|--|---|---|--|---|---|---------|
| 7           | -            | <b>Reserved</b><br>The value read from this bit is indeterminate. Do not set this bit.                                                                                                                                                                                                                                        |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 6           | -            | <b>Reserved</b><br>The value read from this bit is indeterminate. Do not set this bit.                                                                                                                                                                                                                                        |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 5           | PT2H         | Timer 2 overflow interrupt Priority High bit<br><table> <tr> <td><u>PT2H</u></td><td><u>PT2</u></td><td><u>Priority Level</u></td></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table> | <u>PT2H</u> | <u>PT2</u> | <u>Priority Level</u> | 0 | 0 | Lowest | 0 | 1 |  | 1 | 0 |  | 1 | 1 | Highest |
| <u>PT2H</u> | <u>PT2</u>   | <u>Priority Level</u>                                                                                                                                                                                                                                                                                                         |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 0           | 0            | Lowest                                                                                                                                                                                                                                                                                                                        |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 0           | 1            |                                                                                                                                                                                                                                                                                                                               |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 1           | 0            |                                                                                                                                                                                                                                                                                                                               |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 1           | 1            | Highest                                                                                                                                                                                                                                                                                                                       |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 4           | PSH          | Serial port Priority High bit<br><table> <tr> <td><u>PSH</u></td><td><u>PS</u></td><td><u>Priority Level</u></td></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>                  | <u>PSH</u>  | <u>PS</u>  | <u>Priority Level</u> | 0 | 0 | Lowest | 0 | 1 |  | 1 | 0 |  | 1 | 1 | Highest |
| <u>PSH</u>  | <u>PS</u>    | <u>Priority Level</u>                                                                                                                                                                                                                                                                                                         |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 0           | 0            | Lowest                                                                                                                                                                                                                                                                                                                        |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 0           | 1            |                                                                                                                                                                                                                                                                                                                               |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 1           | 0            |                                                                                                                                                                                                                                                                                                                               |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 1           | 1            | Highest                                                                                                                                                                                                                                                                                                                       |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 3           | PT1H         | Timer 1 overflow interrupt Priority High bit<br><table> <tr> <td><u>PT1H</u></td><td><u>PT1</u></td><td><u>Priority Level</u></td></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table> | <u>PT1H</u> | <u>PT1</u> | <u>Priority Level</u> | 0 | 0 | Lowest | 0 | 1 |  | 1 | 0 |  | 1 | 1 | Highest |
| <u>PT1H</u> | <u>PT1</u>   | <u>Priority Level</u>                                                                                                                                                                                                                                                                                                         |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 0           | 0            | Lowest                                                                                                                                                                                                                                                                                                                        |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 0           | 1            |                                                                                                                                                                                                                                                                                                                               |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 1           | 0            |                                                                                                                                                                                                                                                                                                                               |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 1           | 1            | Highest                                                                                                                                                                                                                                                                                                                       |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 2           | PX1H         | External interrupt 1 Priority High bit<br><table> <tr> <td><u>PX1H</u></td><td><u>PX1</u></td><td><u>Priority Level</u></td></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>       | <u>PX1H</u> | <u>PX1</u> | <u>Priority Level</u> | 0 | 0 | Lowest | 0 | 1 |  | 1 | 0 |  | 1 | 1 | Highest |
| <u>PX1H</u> | <u>PX1</u>   | <u>Priority Level</u>                                                                                                                                                                                                                                                                                                         |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 0           | 0            | Lowest                                                                                                                                                                                                                                                                                                                        |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 0           | 1            |                                                                                                                                                                                                                                                                                                                               |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 1           | 0            |                                                                                                                                                                                                                                                                                                                               |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 1           | 1            | Highest                                                                                                                                                                                                                                                                                                                       |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 1           | PT0H         | Timer 0 overflow interrupt Priority High bit<br><table> <tr> <td><u>PT0H</u></td><td><u>PT0</u></td><td><u>Priority Level</u></td></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table> | <u>PT0H</u> | <u>PT0</u> | <u>Priority Level</u> | 0 | 0 | Lowest | 0 | 1 |  | 1 | 0 |  | 1 | 1 | Highest |
| <u>PT0H</u> | <u>PT0</u>   | <u>Priority Level</u>                                                                                                                                                                                                                                                                                                         |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 0           | 0            | Lowest                                                                                                                                                                                                                                                                                                                        |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 0           | 1            |                                                                                                                                                                                                                                                                                                                               |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 1           | 0            |                                                                                                                                                                                                                                                                                                                               |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 1           | 1            | Highest                                                                                                                                                                                                                                                                                                                       |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 0           | PX0H         | External interrupt 0 Priority High bit<br><table> <tr> <td><u>PX0H</u></td><td><u>PX0</u></td><td><u>Priority Level</u></td></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>       | <u>PX0H</u> | <u>PX0</u> | <u>Priority Level</u> | 0 | 0 | Lowest | 0 | 1 |  | 1 | 0 |  | 1 | 1 | Highest |
| <u>PX0H</u> | <u>PX0</u>   | <u>Priority Level</u>                                                                                                                                                                                                                                                                                                         |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 0           | 0            | Lowest                                                                                                                                                                                                                                                                                                                        |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 0           | 1            |                                                                                                                                                                                                                                                                                                                               |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 1           | 0            |                                                                                                                                                                                                                                                                                                                               |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |
| 1           | 1            | Highest                                                                                                                                                                                                                                                                                                                       |             |            |                       |   |   |        |   |   |  |   |   |  |   |   |         |

Reset Value = XX00 0000b

Not bit addressable

## 11. Idle mode

An instruction that sets PCON.0 causes that to be the last instruction executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer, and Serial Port functions. The CPU status is preserved in its entirety : the Stack Pointer, Program Counter, Program Status Word, Accumulator and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels.

There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bits GF0 and GF1 can be used to give an indication if an interrupt occurred during normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

### 11.1 Power-Down Mode

To save maximum power, a power-down mode can be invoked by software (Refer to Table 9-4., PCON register).

In power-down mode, the oscillator is stopped and the instruction that invoked power-down mode is the last instruction executed. The internal RAM and SFRs retain their value until the power-down mode is terminated.  $V_{CC}$  can be lowered to save further power. Either a hardware reset or an external interrupt can cause an exit from power-down. To properly terminate power-down, the reset or external interrupt should not be executed before  $V_{CC}$  is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.

Only external interrupts  $\overline{INT0}$  and  $\overline{INT1}$  are useful to exit from power-down. For that, interrupt must be enabled and configured as level or edge sensitive interrupt input.

Holding the pin low restarts the oscillator but bringing the pin high completes the exit as detailed in Figure 11-1. When both interrupts are enabled, the oscillator restarts as soon as one of the two inputs is held low and power down exit will be completed when the first input will be released. In this case the higher priority interrupt service routine is executed.

Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put TS80C54/58X2 into power-down mode.

### 13. ONCE™ Mode (ON Chip Emulation)

The ONCE mode facilitates testing and debugging of systems using TS80C54/58X2 without removing the circuit from the board. The ONCE mode is invoked by driving certain pins of the TS80C54/58X2; the following sequence must be exercised:

- Pull ALE low while the device is in reset (RST high) and  $\overline{\text{PSEN}}$  is high.
- Hold ALE low as RST is deactivated.

While the TS80C54/58X2 is in ONCE mode, an emulator or test CPU can be used to drive the circuit. Table 13-1 shows the status of the port pins during ONCE mode.

Normal operation is restored when normal reset is applied.

**Table 13-1.** External Pin Status during ONCE Mode

| ALE          | PSEN         | Port 0 | Port 1       | Port 2       | Port 3       | XTAL1/2 |
|--------------|--------------|--------|--------------|--------------|--------------|---------|
| Weak pull-up | Weak pull-up | Float  | Weak pull-up | Weak pull-up | Weak pull-up | Active  |

## 15. Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0. As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

**Table 15-1.** AUXR Register  
AUXR - Auxiliary Register (8Eh)

| 7 | 6 | 5 | 4 | 3 | 2 | 1        | 0  |
|---|---|---|---|---|---|----------|----|
| - | - | - | - | - | - | RESERVED | AO |

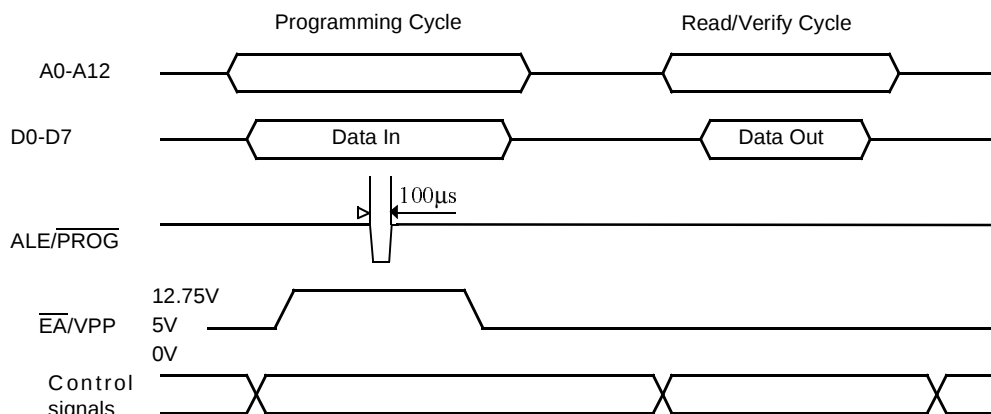
| Bit Number | Bit Mnemonic | Description                                                                                                                               |
|------------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| 7          | -            | <b>Reserved</b><br>The value read from this bit is indeterminate. Do not set this bit.                                                    |
| 6          | -            | <b>Reserved</b><br>The value read from this bit is indeterminate. Do not set this bit.                                                    |
| 5          | -            | <b>Reserved</b><br>The value read from this bit is indeterminate. Do not set this bit.                                                    |
| 4          | -            | <b>Reserved</b><br>The value read from this bit is indeterminate. Do not set this bit.                                                    |
| 3          | -            | <b>Reserved</b><br>The value read from this bit is indeterminate. Do not set this bit.                                                    |
| 2          | -            | <b>Reserved</b><br>The value read from this bit is indeterminate. Do not set this bit.                                                    |
| 1          | -            | <b>Reserved</b><br>The value read from this bit is indeterminate. Do not set this bit.                                                    |
| 0          | AO           | <b>ALE Output bit</b><br>Clear to restore ALE operation during internal fetches.<br>Set to disable ALE operation during internal fetches. |

Reset Value = XXXX XXX0b

Not bit addressable

The encryption array cannot be directly verified. Verification of the encryption array is done by observing that the code array is well encrypted.

**Figure 17-2.** Programming and Verification Signal's Waveform



## 17.4 EPROM Erasure (Windowed Packages Only)

Erasing the EPROM erases the code array, the encryption array and the lock bits returning the parts to full functionality.

Erasure leaves all the EPROM cells in a 1's state (FF).

### 17.4.1 Erasure Characteristics

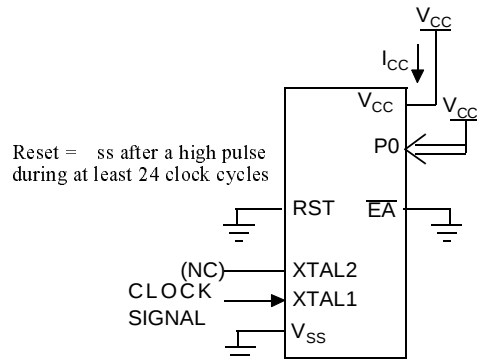
The recommended erasure procedure is exposure to ultraviolet light (at 2537 Å) to an integrated dose at least 15 W-sec/cm<sup>2</sup>. Exposing the EPROM to an ultraviolet lamp of 12,000 µW/cm<sup>2</sup> rating for 30 minutes, at a distance of about 25 mm, should be sufficient. An exposure of 1 hour is recommended with most of standard erasers.

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Å. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

## 18. Signature Bytes

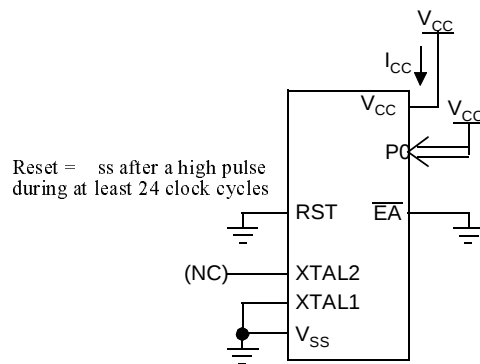
The TS87C54/58X2 has four signature bytes in location 30h, 31h, 60h and 61h. To read these bytes follow the procedure for EPROM verify but activate the control lines provided in Table 31. for Read Signature Bytes. Table 18-1. shows the content of the signature byte for the TS80C54/58X2.

**Figure 19-3.**  $I_{CC}$  Test Condition, Idle Mode



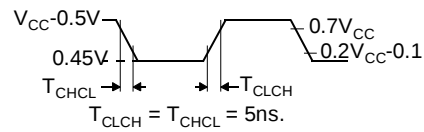
All other pins are disconnected.

**Figure 19-4.**  $I_{CC}$  Test Condition, Power-Down Mode



All other pins are disconnected.

**Figure 19-5.** Clock Signal Waveform for  $I_{CC}$  Tests in Active and Idle Modes



## 19.5.2 External Program Memory Characteristics

**Table 19-5.** Symbol Description

| Symbol            | Parameter                                              |
|-------------------|--------------------------------------------------------|
| T                 | Oscillator clock period                                |
| T <sub>LHLL</sub> | ALE pulse width                                        |
| T <sub>AVLL</sub> | Address Valid to ALE                                   |
| T <sub>LLAX</sub> | Address Hold After ALE                                 |
| T <sub>LLIV</sub> | ALE to Valid Instruction In                            |
| T <sub>LLPL</sub> | ALE to $\overline{\text{PSEN}}$                        |
| T <sub>PLPH</sub> | $\overline{\text{PSEN}}$ Pulse Width                   |
| T <sub>PLIV</sub> | $\overline{\text{PSEN}}$ to Valid Instruction In       |
| T <sub>PXIX</sub> | Input Instruction Hold After $\overline{\text{PSEN}}$  |
| T <sub>PXIZ</sub> | Input Instruction Float After $\overline{\text{PSEN}}$ |
| T <sub>PXAV</sub> | $\overline{\text{PSEN}}$ to Address Valid              |
| T <sub>AVIV</sub> | Address to Valid Instruction In                        |
| T <sub>PLAZ</sub> | $\overline{\text{PSEN}}$ Low to Address Float          |

**Table 19-6.** AC Parameters for Fix Clock

| Speed             | -M<br>40 MHz |     | -V<br>X2 mode<br>30 MHz<br>60 MHz equiv. |     | -V<br>standard mode 40<br>MHz |     | -L<br>X2 mode<br>20 MHz<br>40 MHz equiv. |     | -L<br>standard mode<br>30 MHz |     | Units |
|-------------------|--------------|-----|------------------------------------------|-----|-------------------------------|-----|------------------------------------------|-----|-------------------------------|-----|-------|
|                   | Min          | Max | Min                                      | Max | Min                           | Max | Min                                      | Max | Min                           | Max |       |
| T                 | 25           |     | 33                                       |     | 25                            |     | 50                                       |     | 33                            |     | ns    |
| T <sub>LHLL</sub> | 40           |     | 25                                       |     | 42                            |     | 35                                       |     | 52                            |     | ns    |
| T <sub>AVLL</sub> | 10           |     | 4                                        |     | 12                            |     | 5                                        |     | 13                            |     | ns    |
| T <sub>LLAX</sub> | 10           |     | 4                                        |     | 12                            |     | 5                                        |     | 13                            |     | ns    |
| T <sub>LLIV</sub> |              | 70  |                                          | 45  |                               | 78  |                                          | 65  |                               | 98  | ns    |
| T <sub>LLPL</sub> | 15           |     | 9                                        |     | 17                            |     | 10                                       |     | 18                            |     | ns    |
| T <sub>PLPH</sub> | 55           |     | 35                                       |     | 60                            |     | 50                                       |     | 75                            |     | ns    |
| T <sub>PLIV</sub> |              | 35  |                                          | 25  |                               | 50  |                                          | 30  |                               | 55  | ns    |
| T <sub>PXIX</sub> | 0            |     | 0                                        |     | 0                             |     | 0                                        |     | 0                             |     | ns    |
| T <sub>PXIZ</sub> |              | 18  |                                          | 12  |                               | 20  |                                          | 10  |                               | 18  | ns    |
| T <sub>AVIV</sub> |              | 85  |                                          | 53  |                               | 95  |                                          | 80  |                               | 122 | ns    |
| T <sub>PLAZ</sub> |              | 10  |                                          | 10  |                               | 10  |                                          | 10  |                               | 10  | ns    |

### 19.5.11 External Clock Drive Characteristics (XTAL1)

Table 19-15. AC Parameters

| Symbol              | Parameter               | Min | Max | Units |
|---------------------|-------------------------|-----|-----|-------|
| $T_{CLCL}$          | Oscillator Period       | 25  |     | ns    |
| $T_{CHCX}$          | High Time               | 5   |     | ns    |
| $T_{CLCX}$          | Low Time                | 5   |     | ns    |
| $T_{CLCH}$          | Rise Time               |     | 5   | ns    |
| $T_{CHCL}$          | Fall Time               |     | 5   | ns    |
| $T_{CHCX}/T_{CLCX}$ | Cyclic ratio in X2 mode | 40  | 60  | %     |

### 19.5.12 External Clock Drive Waveforms

Figure 19-11. External Clock Drive Waveforms

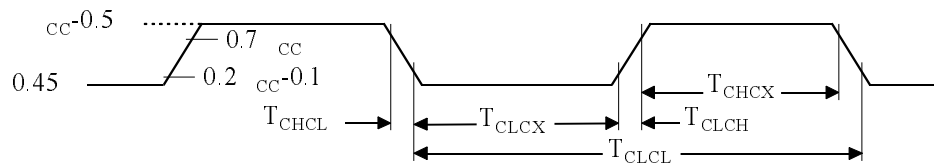
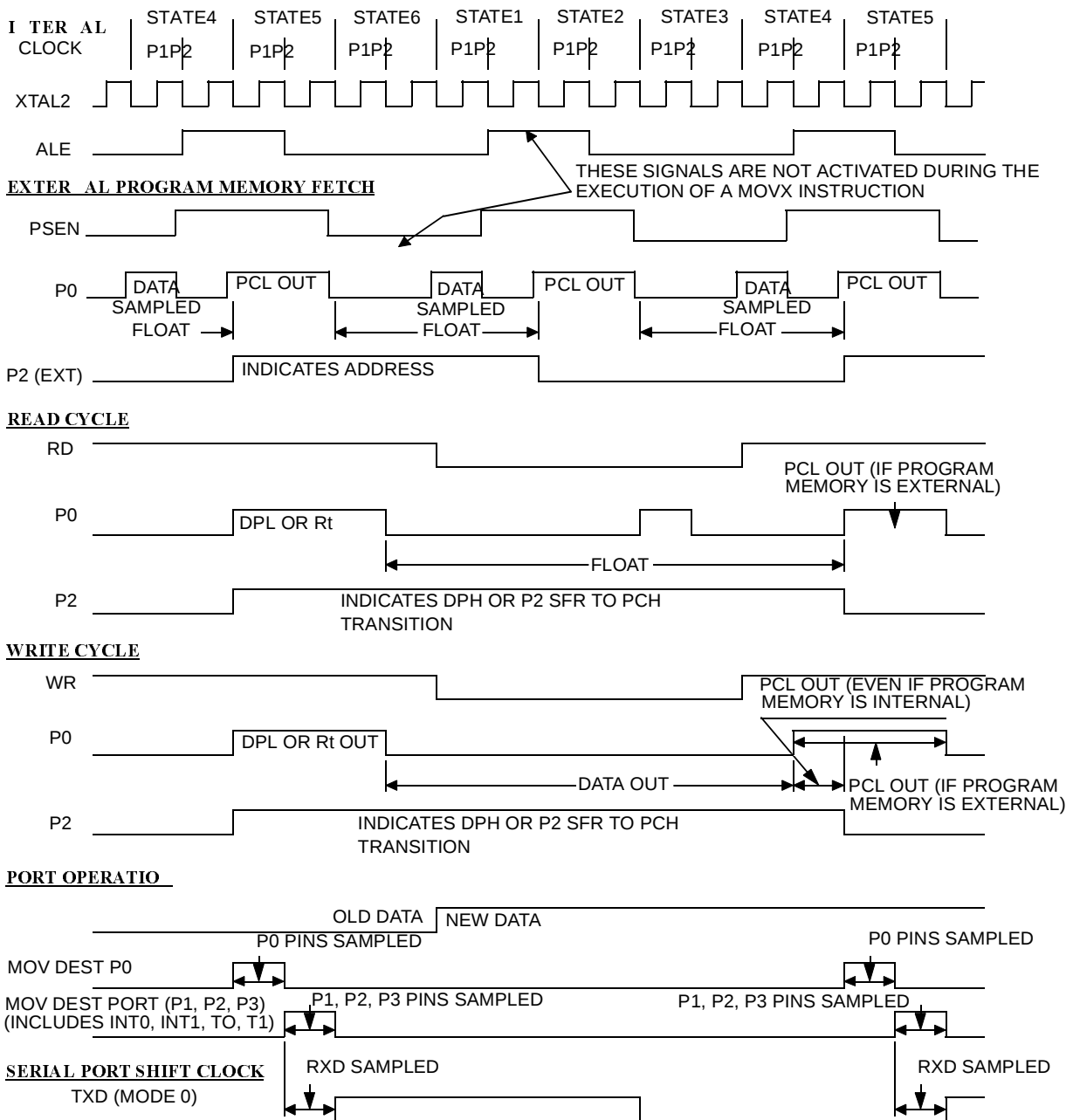


Figure 19-14. Clock Waveforms



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though ( $T_A=25^{\circ}\text{C}$  fully loaded)  $\overline{\text{RD}}$  and  $\overline{\text{WR}}$  propagation delays are approximately 50ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

| Part Number     | Supply Voltage | Temperature Range  | Package | Packing |
|-----------------|----------------|--------------------|---------|---------|
| TS87C58X2-MCE   | 5V ±10%        | Commercial         | VQFP44  | Tray    |
| TS87C58X2-VCA   | 5V ±10%        | Commercial         | PDIL40  | Stick   |
| TS87C58X2-VCB   | 5V ±10%        | Commercial         | PLCC44  | Stick   |
| TS87C58X2-VCC   | 5V ±10%        | Commercial         | PQFP44  | Tray    |
| TS87C58X2-VCE   | 5V ±10%        | Commercial         | VQFP44  | Tray    |
| TS87C58X2-LCA   | 2.7 to 5.5V    | Commercial         | PDIL40  | Stick   |
| TS87C58X2-LCB   | 2.7 to 5.5V    | Commercial         | PLCC44  | Stick   |
| TS87C58X2-LCC   | 2.7 to 5.5V    | Commercial         | PQFP44  | Tray    |
| TS87C58X2-LCE   | 2.7 to 5.5V    | Commercial         | VQFP44  | Tray    |
| TS87C58X2-MIA   | 5V ±10%        | Industrial         | PDIL40  | Stick   |
| TS87C58X2-MIB   | 5V ±10%        | Industrial         | PLCC44  | Stick   |
| TS87C58X2-MIC   | 5V ±10%        | Industrial         | PQFP44  | Tray    |
| TS87C58X2-MIE   | 5V ±10%        | Industrial         | VQFP44  | Tray    |
| TS87C58X2-VIA   | 5V ±10%        | Industrial         | PDIL40  | Stick   |
| TS87C58X2-VIB   | 5V ±10%        | Industrial         | PLCC44  | Stick   |
| TS87C58X2-VIC   | 5V ±10%        | Industrial         | PQFP44  | Tray    |
| TS87C58X2-VIE   | 5V ±10%        | Industrial         | VQFP44  | Tray    |
| TS87C58X2-LIA   | 2.7 to 5.5V    | Industrial         | PDIL40  | Stick   |
| TS87C58X2-LIB   | 2.7 to 5.5V    | Industrial         | PLCC44  | Stick   |
| TS87C58X2-LIC   | 2.7 to 5.5V    | Industrial         | PQFP44  | Tray    |
| TS87C58X2-LIE   | 2.7 to 5.5V    | Industrial         | VQFP44  | Tray    |
|                 |                |                    |         |         |
| AT87C58X2-3CSUM | 5V ±10%        | Industrial & Green | PDIL40  | Stick   |
| AT87C58X2-SLSUM | 5V ±10%        | Industrial & Green | PLCC44  | Stick   |
| AT87C58X2-RLTUM | 5V ±10%        | Industrial & Green | VQFP44  | Tray    |
| AT87C58X2-3CSUL | 2.7 to 5.5V    | Industrial & Green | PDIL40  | Stick   |
| AT87C58X2-SLSUL | 2.7 to 5.5V    | Industrial & Green | PLCC44  | Stick   |
| AT87C58X2-RLTUL | 2.7 to 5.5V    | Industrial & Green | VQFP44  | Tray    |
| AT87C58X2-3CSUV | 5V ±10%        | Industrial & Green | PDIL40  | Stick   |
| AT87C58X2-SLSUV | 5V ±10%        | Industrial & Green | PLCC44  | Stick   |
| AT87C58X2-RLTUV | 5V ±10%        | Industrial & Green | VQFP44  | Tray    |

## 21. Datasheet Revision History

### 21.1 Changes from Rev. C 01/01 to Rev. D 11/05

1. Added green product Ordering Information.

### 21.2 Changes from Rev. D 11/05 to Rev. E 04/06

1. Changed value of AUXR register.