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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	30/20MHz
Connectivity	UART/USART
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/atmel/at87c58x2-slsul">https://www.e-xfl.com/product-detail/atmel/at87c58x2-slsul</a>

## 6. TS80C54/58X2 Enhanced Features

In comparison to the original 80C52, the TS80C54/58X2 implements some new features, which are:

- The X2 option.
- The Dual Data Pointer.
- The Watchdog.
- The 4 level interrupt priority system.
- The power-off flag.
- The ONCE mode.
- The ALE disabling.
- Some enhanced features are also located in the UART and the timer 2.

### 6.1 X2 Feature

The TS80C54/58X2 core needs only 6 clock periods per machine cycle. This feature called "X2" provides the following advantages:

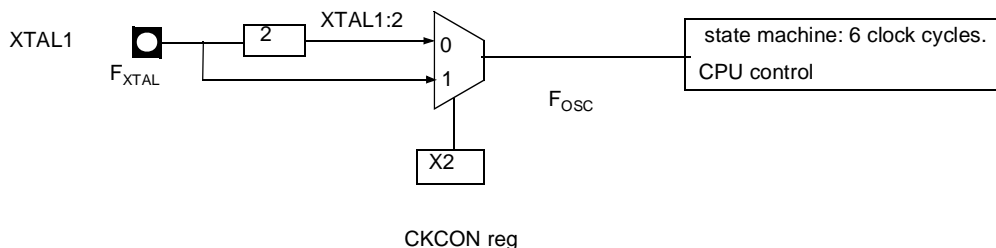
- Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power.
- Save power consumption while keeping same CPU power (oscillator power saving).
- Save power consumption by dividing dynamically operating frequency by 2 in operating and idle modes.
- Increase CPU power by 2 while keeping same crystal frequency.

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

#### 6.1.1 Description

The clock for the whole circuit and peripheral is first divided by two before being used by the CPU core and peripherals. This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%. Figure 6-2. shows the clock generation block diagram. X2 bit is validated on XTAL1÷2 rising edge to avoid glitches when switching from X2 to STD mode. Figure 6-2. shows the mode switching waveforms.

**Figure 6-1.** Clock Generation Diagram



**Table 7-1.** AUXR1: Auxiliary Register 1

7	6	5	4	3	2	1	0
-	-	-	-	GF3	0	-	DPS

Bit Number	Bit Mnemonic	Description
7	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
4	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
3	GF3	This bit is a general purpose user flag
2	0	<b>Reserved</b> Always stuck at 0.
1	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
0	DPS	<b>Data Pointer Selection</b> Clear to select DPTR0. Set to select DPTR1.

Reset Value = XXXX 00X0

Not bit addressable

User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new feature. In that case, the reset value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

## 8. Timer 2

The timer 2 in the TS80C54/58X2 is compatible with the timer 2 in the 80C52.

It is a 16-bit timer/counter: the count is maintained by two eight-bit timer registers, TH2 and TL2, connected in cascade. It is controlled by T2CON register (See Table 8-1) and T2MOD register (See Table 8-2). Timer 2 operation is similar to Timer 0 and Timer 1.  $\overline{C/T2}$  selects  $F_{OSC}/12$  (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows TL2 to be incremented by the selected input.

Timer 2 has 3 operating modes: capture, autoreload and Baud Rate Generator. These modes are selected by the combination of RCLK, TCLK and CP/RL2 (T2CON), as described in the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description.

Refer to the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description for the description of Capture and Baud Rate Generator Modes.

In TS80C54/58X2 Timer 2 includes the following enhancements:

- Auto-reload mode with up or down counter
- Programmable clock-output

### 8.1 Auto-Reload Mode

The auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. If DCEN bit in T2MOD is cleared, timer 2 behaves as in 80C52 (refer to the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description). If DCEN bit is set, timer 2 acts as an Up/down timer/counter as shown in Figure 8-1. In this mode the T2EX pin controls the direction of count.

When T2EX is high, timer 2 counts up. Timer overflow occurs at FFFFh which sets the TF2 flag and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L registers to be loaded into the timer registers TH2 and TL2.

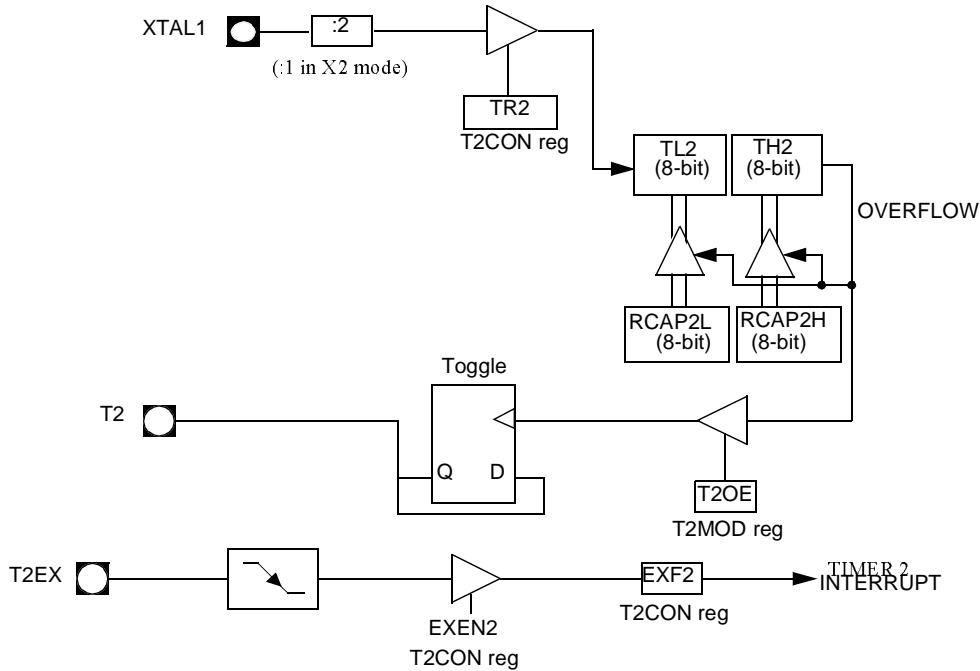
When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers TH2 and TL2 equals the value stored in RCAP2H and RCAP2L registers. The underflow sets TF2 flag and reloads FFFFh into the timer registers.

The EXF2 bit toggles when timer 2 overflows or underflows according to the the direction of the count. EXF2 does not generate any interrupt. This bit can be used to provide 17-bit resolution

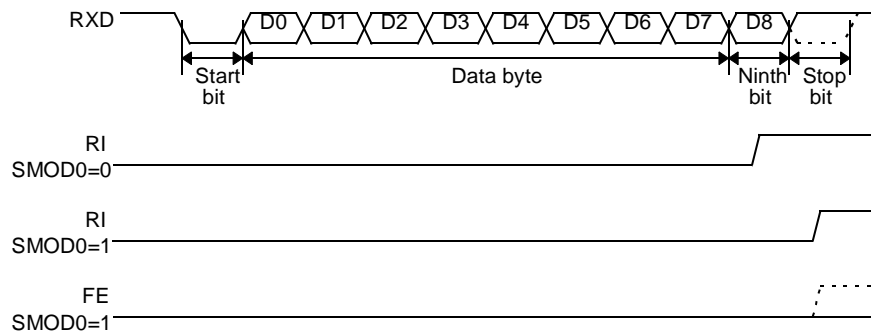
- Enter a 16-bit initial value in timer registers TH2/TL2. It can be the same as the reload value or a different one depending on the application.
- To start the timer, set TR2 run control bit in T2CON register.

It is possible to use timer 2 as a baud rate generator and a clock generator simultaneously. For this configuration, the baud rates and clock frequencies are not independent since both functions use the values in the RCAP2H and RCAP2L registers.

**Figure 8-2.** Clock-Out Mode  $C/\overline{T2} = 0$



**Figure 9-3.** UART Timings in Modes 2 and 3



### 9.1.1 Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.

To support automatic address recognition, a device is identified by a given address and a broadcast address.

**NOTE:** The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).

### 9.1.2 Given Address

Each device has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don't-care bits (defined by zeros) to form the device's given address. The don't-care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed.

To address a device by its individual address, the SADEN mask byte must be 1111 1111b.

For example:

SADDR	0101 0110b
SADEN	1111 1100b
Given	0101 01XXb

**Table 10-3.** IP Register  
IP - Interrupt Priority Register (B8h)

7	6	5	4	3	2	1	0
-	-	PT2	PS	PT1	PX1	PT0	PX0

Bit Number	Bit Mnemonic	Description
7	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
5	PT2	<b>Timer 2 overflow interrupt Priority bit</b> Refer to PT2H for priority level.
4	PS	<b>Serial port Priority bit</b> Refer to PSH for priority level.
3	PT1	<b>Timer 1 overflow interrupt Priority bit</b> Refer to PT1H for priority level.
2	PX1	<b>External interrupt 1 Priority bit</b> Refer to PX1H for priority level.
1	PT0	<b>Timer 0 overflow interrupt Priority bit</b> Refer to PT0H for priority level.
0	PX0	<b>External interrupt 0 Priority bit</b> Refer to PX0H for priority level.

Reset Value = XX00 0000b

Bit addressable

**Table 12-2.** WDTPRG Register  
WDTPRG Address (0A7h)

7	6	5	4	3	2	1	0
T4	T3	T2	T1	T0	S2	S1	S0

Bit Number	Bit Mnemonic	Description																											
7	T4	<b>Reserved</b> Do not try to set or clear this bit.																											
6	T3																												
5	T2																												
4	T1																												
3	T0																												
2	S2	WDT Time-out select bit 2																											
1	S1	WDT Time-out select bit 1																											
0	S0	WDT Time-out select bit 0																											
		<table> <tr> <th>S2S1</th><th>S0</th><th>Selected Time-out</th></tr> <tr> <td>0</td><td>0</td><td>(2<sup>14</sup> - 1) machine cycles, 16.3 ms @ 12 MHz</td></tr> <tr> <td>0</td><td>0</td><td>(2<sup>15</sup> - 1) machine cycles, 32.7 ms @ 12 MHz</td></tr> <tr> <td>0</td><td>1</td><td>(2<sup>16</sup> - 1) machine cycles, 65.5 ms @ 12 MHz</td></tr> <tr> <td>0</td><td>1</td><td>(2<sup>17</sup> - 1) machine cycles, 131 ms @ 12 MHz</td></tr> <tr> <td>1</td><td>0</td><td>(2<sup>18</sup> - 1) machine cycles, 262 ms @ 12 MHz</td></tr> <tr> <td>1</td><td>0</td><td>(2<sup>19</sup> - 1) machine cycles, 542 ms @ 12 MHz</td></tr> <tr> <td>1</td><td>1</td><td>(2<sup>20</sup> - 1) machine cycles, 1.05 s @ 12 MHz</td></tr> <tr> <td>1</td><td>1</td><td>(2<sup>21</sup> - 1) machine cycles, 2.09 s @ 12 MHz</td></tr> </table>	S2S1	S0	Selected Time-out	0	0	(2 <sup>14</sup> - 1) machine cycles, 16.3 ms @ 12 MHz	0	0	(2 <sup>15</sup> - 1) machine cycles, 32.7 ms @ 12 MHz	0	1	(2 <sup>16</sup> - 1) machine cycles, 65.5 ms @ 12 MHz	0	1	(2 <sup>17</sup> - 1) machine cycles, 131 ms @ 12 MHz	1	0	(2 <sup>18</sup> - 1) machine cycles, 262 ms @ 12 MHz	1	0	(2 <sup>19</sup> - 1) machine cycles, 542 ms @ 12 MHz	1	1	(2 <sup>20</sup> - 1) machine cycles, 1.05 s @ 12 MHz	1	1	(2 <sup>21</sup> - 1) machine cycles, 2.09 s @ 12 MHz
S2S1	S0	Selected Time-out																											
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0	0	(2 <sup>15</sup> - 1) machine cycles, 32.7 ms @ 12 MHz																											
0	1	(2 <sup>16</sup> - 1) machine cycles, 65.5 ms @ 12 MHz																											
0	1	(2 <sup>17</sup> - 1) machine cycles, 131 ms @ 12 MHz																											
1	0	(2 <sup>18</sup> - 1) machine cycles, 262 ms @ 12 MHz																											
1	0	(2 <sup>19</sup> - 1) machine cycles, 542 ms @ 12 MHz																											
1	1	(2 <sup>20</sup> - 1) machine cycles, 1.05 s @ 12 MHz																											
1	1	(2 <sup>21</sup> - 1) machine cycles, 2.09 s @ 12 MHz																											

Reset value XXXX X000

### 12.1.1 WDT during Power Down and Idle

In Power Down mode the oscillator stops, which means the WDT also stops. While in Power Down mode the user does not need to service the WDT. There are 2 methods of exiting Power Down mode: by a hardware reset or via a level activated external interrupt which is enabled prior to entering Power Down mode. When Power Down is exited with hardware reset, servicing the WDT should occur as it normally should whenever the TS80C54/58X2 is reset. Exiting Power Down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service routine.

To ensure that the WDT does not overflow within a few states of exiting of powerdown, it is best to reset the WDT just before entering powerdown.

In the Idle mode, the oscillator continues to run. To prevent the WDT from resetting the TS80C54/58X2 while in Idle mode, the user should always set up a timer that will periodically exit Idle, service the WDT, and re-enter Idle mode.



## 15. Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0. As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

**Table 15-1.** AUXR Register  
AUXR - Auxiliary Register (8Eh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	RESERVED	AO

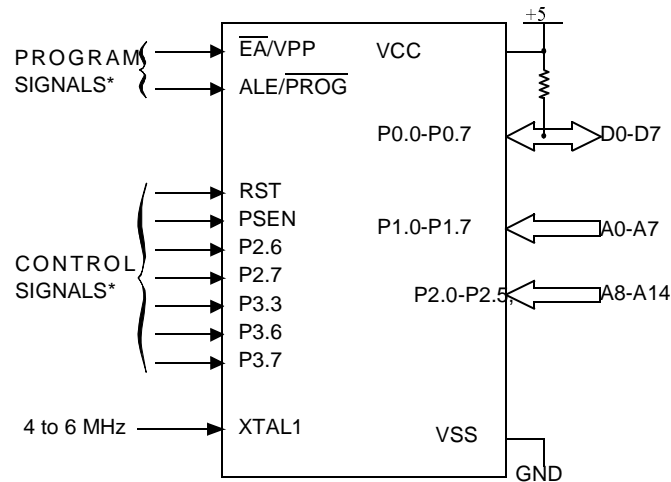
  

Bit Number	Bit Mnemonic	Description
7	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
4	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
3	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
2	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
1	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
0	AO	<b>ALE Output bit</b> Clear to restore ALE operation during internal fetches. Set to disable ALE operation during internal fetches.

Reset Value = XXXX XXX0b

Not bit addressable

**Figure 17-1.** Set-Up Modes Configuration



\* See Table 31. for proper value on these inputs

### 17.3.3 Programming Algorithm

The Improved Quick Pulse algorithm is based on the Quick Pulse algorithm and decreases the number of pulses applied during byte programming from 25 to 1.

To program the TS80C54/58X2 the following sequence must be exercised:

- Step 1: Activate the combination of control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Input the appropriate data on the data lines.
- Step 4: Raise  $\overline{EA}/VPP$  from VCC to VPP (typical 12.75V).
- Step 5: Pulse  $ALE/\overline{PROG}$  once.
- Step 6: Lower  $\overline{EA}/VPP$  from VPP to VCC

Repeat step 2 through 6 changing the address and data for the entire array or until the end of the object file is reached (See Figure 17-2.).

### 17.3.4 Verify algorithm

Code array verify must be done after each byte or block of bytes is programmed. In either case, a complete verify of the programmed array will ensure reliable programming of the TS87C54/58X2.

P 2.7 is used to enable data output.

To verify the TS87C54/58X2 code the following sequence must be exercised:

- Step 1: Activate the combination of program and control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Read data on the data lines.

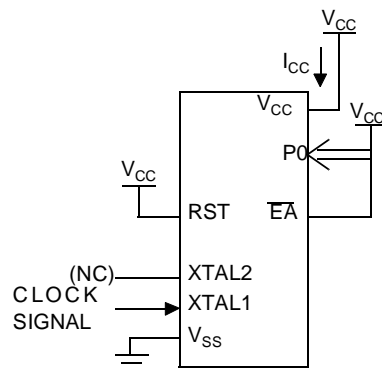
Repeat step 2 through 3 changing the address for the entire array verification (See Figure 17-2.)

**Table 18-1.** Signature Bytes Content

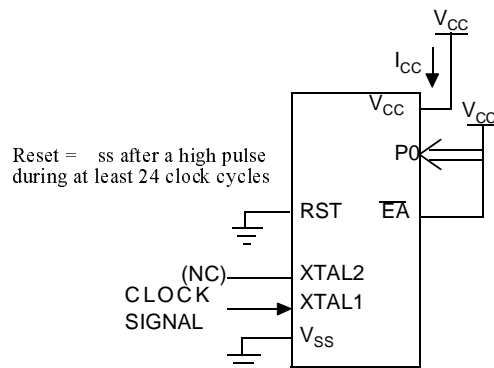
Location	Contents	Comment
30h	58h	Manufacturer Code: Atmel Wireless & Microcontrollers
31h	57h	Family Code: C51 X2
60h	37h	Product name: TS80C58X2
60h	B7h	Product name: TS87C58X2
60h	3Bh	Product name: TS80C54X2
60h	BBh	Product name: TS87C54X2
61h	FFh	Product revision number

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$V_{OL1}$	Output Low Voltage, port 0 <sup>(6)</sup>			0.3	V	$I_{OL} = 200 \mu A^{(4)}$
				0.45	V	$I_{OL} = 3.2 \text{ mA}^{(4)}$
				1.0	V	$I_{OL} = 7.0 \text{ mA}^{(4)}$
$V_{OL2}$	Output Low Voltage, ALE, $\overline{PSEN}$			0.3	V	$I_{OL} = 100 \mu A^{(4)}$
				0.45	V	$I_{OL} = 1.6 \text{ mA}^{(4)}$
				1.0	V	$I_{OL} = 3.5 \text{ mA}^{(4)}$
$V_{OH}$	Output High Voltage, ports 1, 2, 3	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$			V	$I_{OH} = -10 \mu A$
					V	$I_{OH} = -30 \mu A$
					V	$I_{OH} = -60 \mu A$ $V_{CC} = 5 \text{ V} \pm 10\%$
$V_{OH1}$	Output High Voltage, port 0	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$			V	$I_{OH} = -200 \mu A$
					V	$I_{OH} = -3.2 \text{ mA}$
					V	$I_{OH} = -7.0 \text{ mA}$ $V_{CC} = 5 \text{ V} \pm 10\%$
$V_{OH2}$	Output High Voltage, ALE, $\overline{PSEN}$	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$			V	$I_{OH} = -100 \mu A$
					V	$I_{OH} = -1.6 \text{ mA}$
					V	$I_{OH} = -3.5 \text{ mA}$ $V_{CC} = 5 \text{ V} \pm 10\%$
$R_{RST}$	RST Pulldown Resistor	50	90 <sup>(5)</sup>	200	k $\Omega$	
$I_{IL}$	Logical 0 Input Current ports 1, 2 and 3			-50	$\mu A$	$V_{in} = 0.45 \text{ V}$
$I_{LI}$	Input Leakage Current			$\pm 10$	$\mu A$	$0.45 \text{ V} < V_{in} < V_{CC}$
$I_{TL}$	Logical 1 to 0 Transition Current, ports 1, 2, 3			-650	$\mu A$	$V_{in} = 2.0 \text{ V}$
$C_{IO}$	Capacitance of I/O Buffer			10	pF	$F_c = 1 \text{ MHz}$ $T_A = 25^\circ C$
$I_{PD}$	Power Down Current		20 <sup>(5)</sup>	50	$\mu A$	$2.0 \text{ V} < V_{CC} < 5.5 \text{ V}^{(3)}$
$I_{CC}$ under RESET	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			1 + 0.4 Freq (MHz) @12MHz 5.8 @16MHz 7.4	mA	$V_{CC} = 5.5 \text{ V}^{(1)}$
$I_{CC}$ operating	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			3 + 0.6 Freq (MHz) @12MHz 10.2 @16MHz 12.6	mA	$V_{CC} = 5.5 \text{ V}^{(8)}$
$I_{CC}$ idle	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			0.25+0.3 Freq (MHz) @12MHz 3.9 @16MHz 5.1	mA	$V_{CC} = 5.5 \text{ V}^{(2)}$

5. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
6. Under steady state (non-transient) conditions,  $I_{OL}$  must be externally limited as follows:  
 Maximum  $I_{OL}$  per port pin: 10 mA  
 Maximum  $I_{OL}$  per 8-bit port:  
 Port 0: 26 mA  
 Ports 1, 2 and 3: 15 mA  
 Maximum total  $I_{OL}$  for all output pins: 71 mA  
 If  $I_{OL}$  exceeds the test condition,  $V_{OL}$  may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
7. For other values, please contact your sales office.
8. Operating  $I_{CC}$  is measured with all output pins disconnected; XTAL1 driven with  $T_{CLCH}$ ,  $T_{CHCL} = 5$  ns (see Figure 19-5.),  $V_{IL} = V_{SS} + 0.5$  V,  
 $V_{IH} = V_{CC} - 0.5$  V; XTAL2 N.C.;  $\overline{EA} = \text{Port 0} = V_{CC}$ ;  $RST = V_{SS}$ . The internal ROM runs the code 80 FE (label: SJMP label).  $I_{CC}$  would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.

**Figure 19-1.**  $I_{CC}$  Test Condition, under reset


All other pins are disconnected.

**Figure 19-2.** Operating  $I_{CC}$  Test Condition


All other pins are disconnected.

## 19.5 AC Parameters

### 19.5.1 Explanation of the AC Symbols

Each timing symbol has 5 characters. The first character is always a “T” (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example:  $T_{AVLL}$  = Time for Address Valid to ALE Low.

$T_{LLPL}$  = Time for ALE Low to PSEN Low.

$T_A = 0$  to  $+70^{\circ}\text{C}$  (commercial temperature range);  $V_{SS} = 0\text{ V}$ ;  $V_{CC} = 5\text{ V} \pm 10\%$ ; -M and -V ranges.  
 $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  (industrial temperature range);  $V_{SS} = 0\text{ V}$ ;  $V_{CC} = 5\text{ V} \pm 10\%$ ; -M and -V ranges.

$T_A = 0$  to  $+70^{\circ}\text{C}$  (commercial temperature range);  $V_{SS} = 0\text{ V}$ ;  $2.7\text{ V} < V_{CC} < 5.5\text{ V}$ ; -L range.

$T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  (industrial temperature range);  $V_{SS} = 0\text{ V}$ ;  $2.7\text{ V} < V_{CC} < 5.5\text{ V}$ ; -L range.

Table 19-3. gives the maximum applicable load capacitance for Port 0, Port 1, 2 and 3, and ALE and PSEN signals. Timings will be guaranteed if these capacitances are respected. Higher capacitance values can be used, but timings will then be degraded.

**Table 19-3.** Load Capacitance versus speed range, in pF

	-M	-V	-L
Port 0	100	50	100
Port 1, 2, 3	80	50	80
ALE / $\overline{\text{PSEN}}$	100	30	100

Table 19-5., Table 19-8. and Table 19-11. give the description of each AC symbols.

Table 19-6., Table 19-9. and Table 19-12. give for each range the AC parameter.

Table 19-7., Table 19-10. and Table 19-13. give the frequency derating formula of the AC parameter. To calculate each AC symbols, take the x value corresponding to the speed grade you need (-M, -V or -L) and replace this value in the formula. Values of the frequency must be limited to the corresponding speed grade:

**Table 19-4.** Max frequency for derating formula regarding the speed grade

	-M X1 mode	-M X2 mode	-V X1 mode	-V X2 mode	-L X1 mode	-L X2 mode
Freq (MHz)	40	20	40	30	30	20
T (ns)	25	50	25	33.3	33.3	50

Example:

$T_{LLIV}$  in X2 mode for a -V part at 20 MHz ( $T = 1/20^{\text{E}6} = 50\text{ ns}$ ):

$x = 22$  (Table 19-7.)

$T = 50\text{ ns}$

$T_{LLIV} = 2T - x = 2 \times 50 - 22 = 78\text{ ns}$

## 19.5.2 External Program Memory Characteristics

**Table 19-5.** Symbol Description

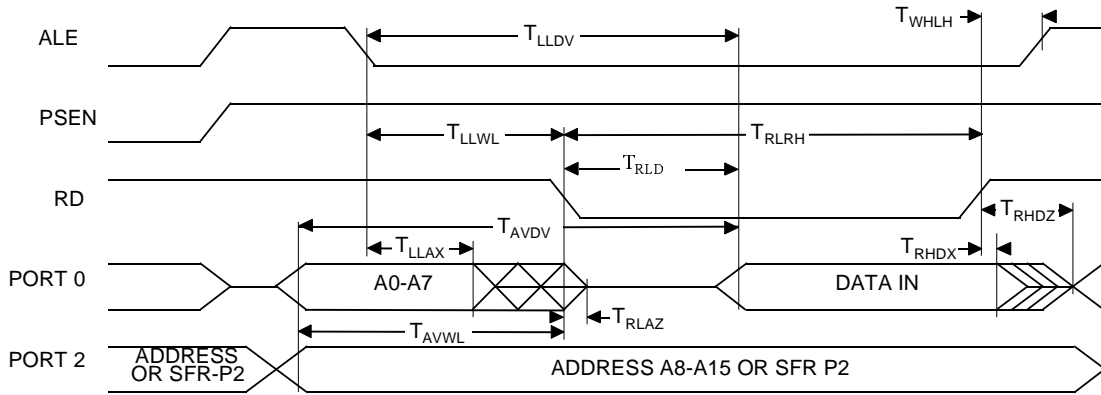
Symbol	Parameter
T	Oscillator clock period
T <sub>LHLL</sub>	ALE pulse width
T <sub>AVLL</sub>	Address Valid to ALE
T <sub>LLAX</sub>	Address Hold After ALE
T <sub>LLIV</sub>	ALE to Valid Instruction In
T <sub>LLPL</sub>	ALE to $\overline{\text{PSEN}}$
T <sub>PLPH</sub>	$\overline{\text{PSEN}}$ Pulse Width
T <sub>PLIV</sub>	$\overline{\text{PSEN}}$ to Valid Instruction In
T <sub>PXIX</sub>	Input Instruction Hold After $\overline{\text{PSEN}}$
T <sub>PXIZ</sub>	Input Instruction Float After $\overline{\text{PSEN}}$
T <sub>PXAV</sub>	$\overline{\text{PSEN}}$ to Address Valid
T <sub>AVIV</sub>	Address to Valid Instruction In
T <sub>PLAZ</sub>	$\overline{\text{PSEN}}$ Low to Address Float

**Table 19-6.** AC Parameters for Fix Clock

Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
T	25		33		25		50		33		ns
T <sub>LHLL</sub>	40		25		42		35		52		ns
T <sub>AVLL</sub>	10		4		12		5		13		ns
T <sub>LLAX</sub>	10		4		12		5		13		ns
T <sub>LLIV</sub>		70		45		78		65		98	ns
T <sub>LLPL</sub>	15		9		17		10		18		ns
T <sub>PLPH</sub>	55		35		60		50		75		ns
T <sub>PLIV</sub>		35		25		50		30		55	ns
T <sub>PXIX</sub>	0		0		0		0		0		ns
T <sub>PXIZ</sub>		18		12		20		10		18	ns
T <sub>AVIV</sub>		85		53		95		80		122	ns
T <sub>PLAZ</sub>		10		10		10		10		10	ns

## 19.5.6 External Data Memory Read Cycle

**Figure 19-8.** External Data Memory Read Cycle



## 19.5.7 Serial Port Timing - Shift Register Mode

**Table 19-11.** Symbol Description

Symbol	Parameter
$T_{XLXL}$	Serial port clock cycle time
$T_{QVHX}$	Output data set-up to clock rising edge
$T_{XHGX}$	Output data hold after clock rising edge
$T_{XHDX}$	Input data hold after clock rising edge
$T_{XHDX}$	Input data hold after clock rising edge
$T_{XHDV}$	Clock rising edge to input data valid

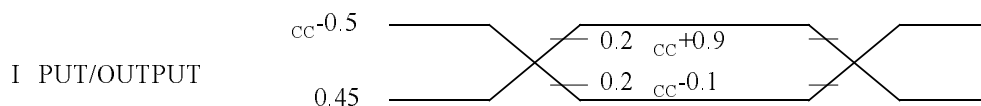
**Table 19-12.** AC Parameters for a Fix Clock

Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$T_{XLXL}$	300		200		300		300		400		ns
$T_{QVHX}$	200		117		200		200		283		ns
$T_{XHGX}$	30		13		30		30		47		ns
$T_{XHDX}$	0		0		0		0		0		ns
$T_{XHDV}$		117		34		117		117		200	ns



### 19.5.13 AC Testing Input/Output Waveforms

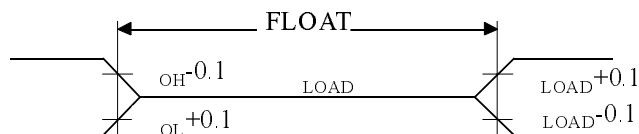
**Figure 19-12. AC Testing Input/Output Waveforms**



AC inputs during testing are driven at  $V_{CC} - 0.5$  for a logic "1" and 0.45V for a logic "0". Timing measurement are made at  $V_{IH}$  min for a logic "1" and  $V_{IL}$  max for a logic "0".

### 19.5.14 Float Waveforms

**Figure 19-13. Float Waveforms**



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded  $V_{OH}/V_{OL}$  level occurs.  $I_{OL}/I_{OH} \geq \pm 20\text{mA}$ .

### 19.5.15 Clock Waveforms

Valid in normal clock mode. In X2 mode XTAL2 signal must be changed to XTAL2 divided by two.

Part Number	Supply Voltage	Temperature Range	Package	Packing
TS87C54X2-MCC	5V ±10%	Commercial	PQFP44	Tray
TS87C54X2-MCE	5V ±10%	Commercial	VQFP44	Tray
TS87C54X2-VCA	5V ±10%	Commercial	PDIL40	Stick
TS87C54X2-VCB	5V ±10%	Commercial	PLCC44	Stick
TS87C54X2-VCC	5V ±10%	Commercial	PQFP44	Tray
TS87C54X2-VCE	5V ±10%	Commercial	VQFP44	Tray
TS87C54X2-LCA	2.7 to 5.5V	Commercial	PDIL40	Stick
TS87C54X2-LCB	2.7 to 5.5V	Commercial	PLCC44	Stick
TS87C54X2-LCC	2.7 to 5.5V	Commercial	PQFP44	Tray
TS87C54X2-LCE	2.7 to 5.5V	Commercial	VQFP44	Tray
TS87C54X2-MIA	5V ±10%	Industrial	PDIL40	Stick
TS87C54X2-MIB	5V ±10%	Industrial	PLCC44	Stick
TS87C54X2-MIC	5V ±10%	Industrial	PQFP44	Tray
TS87C54X2-MIE	5V ±10%	Industrial	VQFP44	Tray
TS87C54X2-VIA	5V ±10%	Industrial	PDIL40	Stick
TS87C54X2-VIB	5V ±10%	Industrial	PLCC44	Stick
TS87C54X2-VIC	5V ±10%	Industrial	PQFP44	Tray
TS87C54X2-VIE	5V ±10%	Industrial	VQFP44	Tray
TS87C54X2-LIA	2.7 to 5.5V	Industrial	PDIL40	Stick
TS87C54X2-LIB	2.7 to 5.5V	Industrial	PLCC44	Stick
TS87C54X2-LIC	2.7 to 5.5V	Industrial	PQFP44	Tray
TS87C54X2-LIE	2.7 to 5.5V	Industrial	VQFP44	Tray
AT87C54X2-3CSUM	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C54X2-SLSUM	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C54X2-RLTUM	5V ±10%	Industrial & Green	VQFP44	Tray
AT87C54X2-3CSUL	2.7 to 5.5V	Industrial & Green	PDIL40	Stick
AT87C54X2-SLSUL	2.7 to 5.5V	Industrial & Green	PLCC44	Stick
AT87C54X2-RLTUL	2.7 to 5.5V	Industrial & Green	VQFP44	Tray
AT87C54X2-3CSUV	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C54X2-SLSUV	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C54X2-RLTUV	5V ±10%	Industrial & Green	VQFP44	Tray

Part Number	Supply Voltage	Temperature Range	Package	Packing
TS80C58X2xxx-MCA	-5 to +/-10%	Commercial	PDIL40	Stick
TS80C58X2xxx-MCB	-5 to +/-10%	Commercial	PLCC44	Stick
TS80C58X2xxx-MCC	-5 to +/-10%	Commercial	PQFP44	Tray
TS80C58X2xxx-MCE	-5 to +/-10%	Commercial	VQFP44	Tray
TS80C58X2xxx-VCA	-5 to +/-10%	Commercial	PDIL40	Stick
TS80C58X2xxx-VCB	-5 to +/-10%	Commercial	PLCC44	Stick
TS80C58X2xxx-VCC	-5 to +/-10%	Commercial	PQFP44	Tray
TS80C58X2xxx-VCE	-5 to +/-10%	Commercial	VQFP44	Tray
TS80C58X2xxx-LCA	-5 to +/-10%	Commercial	PDIL40	Stick
TS80C58X2xxx-LCB	-5 to +/-10%	Commercial	PLCC44	Stick
TS80C58X2xxx-LCC	-5 to +/-10%	Commercial	PQFP44	Tray
TS80C58X2xxx-LCE	-5 to +/-10%	Commercial	VQFP44	Tray
TS80C58X2xxx-MIA	-5 to +/-10%	Industrial	PDIL40	Stick
TS80C58X2xxx-MIB	-5 to +/-10%	Industrial	PLCC44	Stick
TS80C58X2xxx-MIC	-5 to +/-10%	Industrial	PQFP44	Tray
TS80C58X2xxx-MIE	-5 to +/-10%	Industrial	VQFP44	Tray
TS80C58X2xxx-VIA	-5 to +/-10%	Industrial	PDIL40	Stick
TS80C58X2xxx-VIB	-5 to +/-10%	Industrial	PLCC44	Stick
TS80C58X2xxx-VIC	-5 to +/-10%	Industrial	PQFP44	Tray
TS80C58X2xxx-VIE	-5 to +/-10%	Industrial	VQFP44	Tray
TS80C58X2xxx-LIA	-5 to +/-10%	Industrial	PDIL40	Stick
TS80C58X2xxx-LIB	-5 to +/-10%	Industrial	PLCC44	Stick
TS80C58X2xxx-LIC	-5 to +/-10%	Industrial	PQFP44	Tray
TS80C58X2xxx-LIE	-5 to +/-10%	Industrial	VQFP44	Tray
AT80C58X2zzz-3CSUM	-5 to +/-10%	Industrial & Green	PDIL40	Stick
AT80C58X2zzz-SLSUM	-5 to +/-10%	Industrial & Green	PLCC44	Stick
AT80C58X2zzz-RLTUM	-5 to +/-10%	Industrial & Green	VQFP44	Tray
AT80C58X2zzz-3CSUL	-5 to +/-10%	Industrial & Green	PDIL40	Stick
AT80C58X2zzz-SLSUL	-5 to +/-10%	Industrial & Green	PLCC44	Stick
AT80C58X2zzz-RLTUL	-5 to +/-10%	Industrial & Green	VQFP44	Tray
AT80C58X2zzz-3CSUV	-5 to +/-10%	Industrial & Green	PDIL40	Stick
AT80C58X2zzz-SLSUV	-5 to +/-10%	Industrial & Green	PLCC44	Stick
AT80C58X2zzz-RLTUV	-5 to +/-10%	Industrial & Green	VQFP44	Tray
TS87C58X2-MCA	5V ±10%	Commercial	PDIL40	Stick
TS87C58X2-MCB	5V ±10%	Commercial	PLCC44	Stick
TS87C58X2-MCC	5V ±10%	Commercial	PQFP44	Tray

Part Number	Supply Voltage	Temperature Range	Package	Packing
TS87C58X2-MCE	5V $\pm$ 10%	Commercial	VQFP44	Tray
TS87C58X2-VCA	5V $\pm$ 10%	Commercial	PDIL40	Stick
TS87C58X2-VCB	5V $\pm$ 10%	Commercial	PLCC44	Stick
TS87C58X2-VCC	5V $\pm$ 10%	Commercial	PQFP44	Tray
TS87C58X2-VCE	5V $\pm$ 10%	Commercial	VQFP44	Tray
TS87C58X2-LCA	2.7 to 5.5V	Commercial	PDIL40	Stick
TS87C58X2-LCB	2.7 to 5.5V	Commercial	PLCC44	Stick
TS87C58X2-LCC	2.7 to 5.5V	Commercial	PQFP44	Tray
TS87C58X2-LCE	2.7 to 5.5V	Commercial	VQFP44	Tray
TS87C58X2-MIA	5V $\pm$ 10%	Industrial	PDIL40	Stick
TS87C58X2-MIB	5V $\pm$ 10%	Industrial	PLCC44	Stick
TS87C58X2-MIC	5V $\pm$ 10%	Industrial	PQFP44	Tray
TS87C58X2-MIE	5V $\pm$ 10%	Industrial	VQFP44	Tray
TS87C58X2-VIA	5V $\pm$ 10%	Industrial	PDIL40	Stick
TS87C58X2-VIB	5V $\pm$ 10%	Industrial	PLCC44	Stick
TS87C58X2-VIC	5V $\pm$ 10%	Industrial	PQFP44	Tray
TS87C58X2-VIE	5V $\pm$ 10%	Industrial	VQFP44	Tray
TS87C58X2-LIA	2.7 to 5.5V	Industrial	PDIL40	Stick
TS87C58X2-LIB	2.7 to 5.5V	Industrial	PLCC44	Stick
TS87C58X2-LIC	2.7 to 5.5V	Industrial	PQFP44	Tray
TS87C58X2-LIE	2.7 to 5.5V	Industrial	VQFP44	Tray
AT87C58X2-3CSUM	5V $\pm$ 10%	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUM	5V $\pm$ 10%	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUM	5V $\pm$ 10%	Industrial & Green	VQFP44	Tray
AT87C58X2-3CSUL	2.7 to 5.5V	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUL	2.7 to 5.5V	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUL	2.7 to 5.5V	Industrial & Green	VQFP44	Tray
AT87C58X2-3CSUV	5V $\pm$ 10%	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUV	5V $\pm$ 10%	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUV	5V $\pm$ 10%	Industrial & Green	VQFP44	Tray

## 21. Datasheet Revision History

### 21.1 Changes from Rev. C 01/01 to Rev. D 11/05

1. Added green product Ordering Information.

### 21.2 Changes from Rev. D 11/05 to Rev. E 04/06

1. Changed value of AUXR register.



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