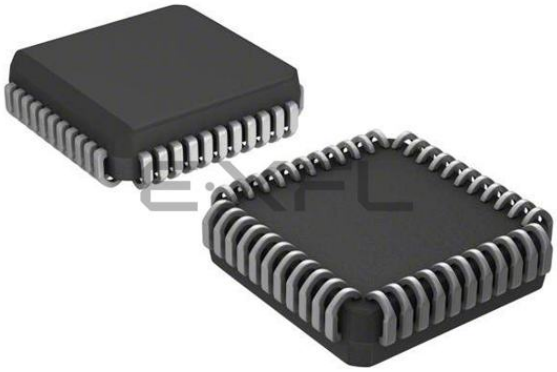

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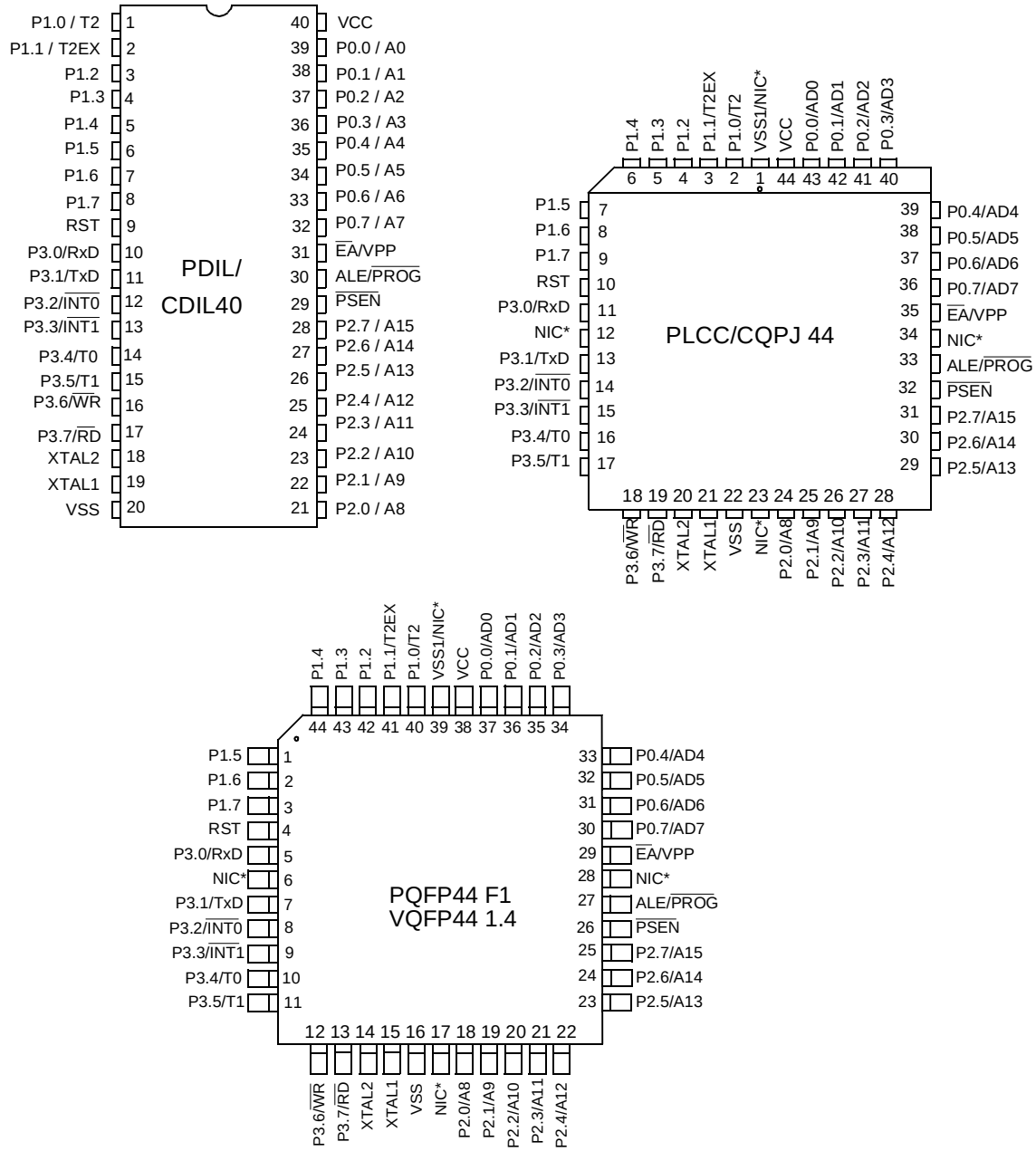
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	30/20MHz
Connectivity	UART/USART
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts87c54x2-lcb

5. Pin Configuration



*NIC: No Internal Connection

Table 5-1. Pin Description for 40/44 pin packages

MNEMONIC	PIN NUMBER			TYPE	Name And Function
	DIL	LCC	VQFP 1.4		
V_{SS}	20	22	16	I	**Ground:** 0V reference
Vss1		1	39	I	Optional Ground: **Contact the Sales Office for ground connection.**
V_{CC}	40	44	38	I	**Power Supply:** This is the power supply voltage for normal, idle and power-down operation
P0.0-P0.7	39-32	43-36	37-30	I/O	**Port 0**: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. Port 0 pins must be polarized to Vcc or Vss in order to prevent any parasitic current consumption. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-up when emitting 1s. Port 0 also inputs the code bytes during EPROM programming. External pull-ups are required during program verification during which P0 outputs the code bytes.
P1.0-P1.7	1-8	2-9	40-44 1-3	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups. Port 1 also receives the low-order address byte during memory programming and verification. Alternate functions for Port 1 include:
	1	2	40	I/O	**T2 (P1.0):** Timer/Counter 2 external count input/Clockout
	2	3	41	I	**T2EX (P1.1):** Timer/Counter 2 Reload/Capture/Direction Control
P2.0-P2.7	21-28	24-31	18-25	I/O	**Port 2**: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR).In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 emits the contents of the P2 SFR. Some Port 2 pins receive the high order address bits during EPROM programming and verification: P2.0 to P2.5 for A8 to A13
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Some Port 3 pin P3.4 receive the high order address bits during EPROM programming and verification for TS8xC58X2 devices. Port 3 also serves the special features of the 80C51 family, as listed below.
	10	11	5	I	**RXD (P3.0):** Serial input port
	11	13	7	O	**TXD (P3.1):** Serial output port
	12	14	8	I	**$\overline{\text{INT0}}$ (P3.2):** External interrupt 0
	13	15	9	I	**$\overline{\text{INT1}}$ (P3.3):** External interrupt 1
	14	16	10	I	**T0 (P3.4):** Timer 0 external input
	15	17	11	I	**T1 (P3.5):** Timer 1 external input
	16	18	12	O	**$\overline{\text{WR}}$ (P3.6):** External data memory write strobe
	17	19	13	O	**$\overline{\text{RD}}$ (P3.7):** External data memory read strobe P3.4 also receives A14 during TS87C58X2 EPROM Programming.
Reset	9	10	4	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC}.

7.1 Application

Software can take advantage of the additional data pointers to both increase speed and reduce code size, for example, block operations (copy, compare, search ...) are well served by using one data pointer as a 'source' pointer and the other one as a "destination" pointer.

ASSEMBLY LANGUAGE

```
; Block move using dual data pointers
; Destroys DPTR0, DPTR1, A and PSW
; note: DPS exits opposite of entry state
; unless an extra INC AUXR1 is added
;
00A2                AUXR1 EQU 0A2H
;
0000 909000         MOV   DPTR,#SOURCE      ; address of SOURCE
0003 05A2           INC   AUXR1             ; switch data pointers
0005 90A000         MOV   DPTR,#DEST        ; address of DEST
0008                LOOP:
0008 05A2           INC   AUXR1             ; switch data pointers
000A E0             MOVX  A,@DPTR           ; get a byte from SOURCE
000B A3             INC   DPTR              ; increment SOURCE address
000C 05A2           INC   AUXR1             ; switch data pointers
000E F0             MOVX  @DPTR,A           ; write the byte to DEST
000F A3             INC   DPTR              ; increment DEST address
0010 70F6           JNZ   LOOP              ; check for 0 terminator
0012 05A2           INC   AUXR1             ; (optional) restore DPS
```

INC is a short (2 bytes) and fast (12 clocks) way to manipulate the DPS bit in the AUXR1 SFR. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry. Observe that without the last instruction (INC AUXR1), the routine will exit with DPS in the opposite state.

8. Timer 2

The timer 2 in the TS80C54/58X2 is compatible with the timer 2 in the 80C52.
It is a 16-bit timer/counter: the count is maintained by two eight-bit timer registers, TH2 and TL2, connected in cascade. It is controlled by T2CON register (See Table 8-1) and T2MOD register (See Table 8-2). Timer 2 operation is similar to Timer 0 and Timer 1. C/$\overline{T2}$ selects F_{OSC}/12 (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows TL2 to be incremented by the selected input.

Timer 2 has 3 operating modes: capture, autoreload and Baud Rate Generator. These modes are selected by the combination of RCLK, TCLK and CP/$\overline{RL2}$ (T2CON), as described in the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description.

Refer to the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description for the description of Capture and Baud Rate Generator Modes.

In TS80C54/58X2 Timer 2 includes the following enhancements:

- Auto-reload mode with up or down counter
- Programmable clock-output

8.1 Auto-Reload Mode

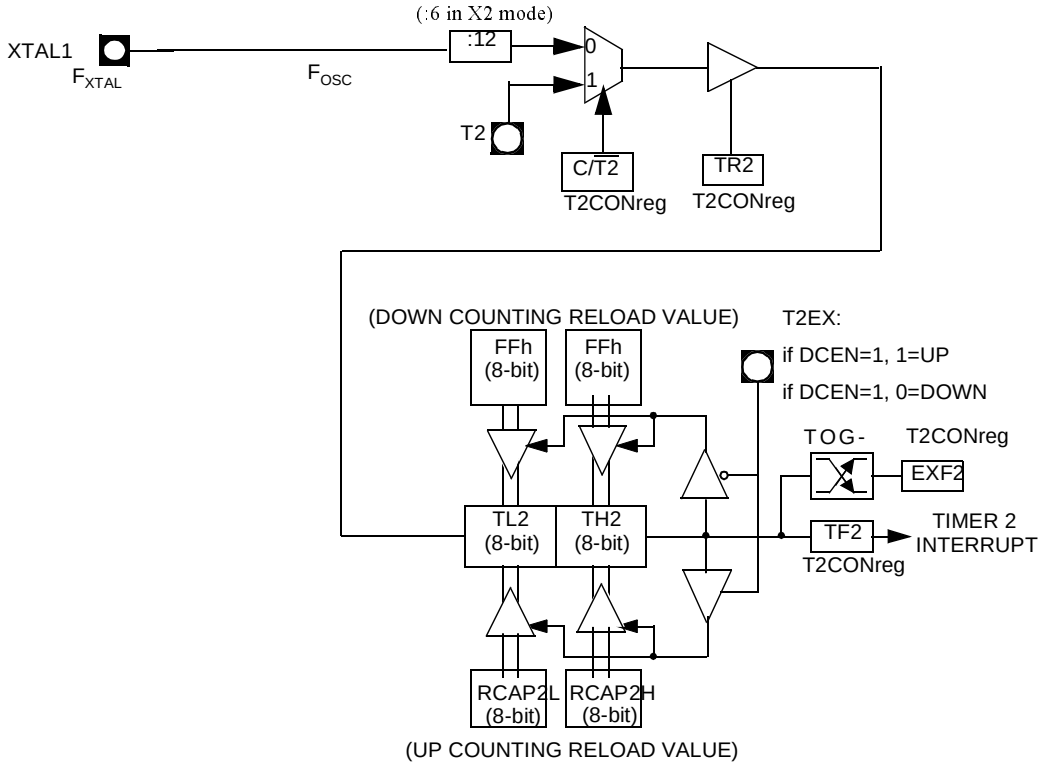
The auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. If DCEN bit in T2MOD is cleared, timer 2 behaves as in 80C52 (refer to the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description). If DCEN bit is set, timer 2 acts as an Up/down timer/counter as shown in Figure 8-1. In this mode the T2EX pin controls the direction of count.

When T2EX is high, timer 2 counts up. Timer overflow occurs at FFFFh which sets the TF2 flag and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L registers to be loaded into the timer registers TH2 and TL2.

When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers TH2 and TL2 equals the value stored in RCAP2H and RCAP2L registers. The underflow sets TF2 flag and reloads FFFFh into the timer registers.

The EXF2 bit toggles when timer 2 overflows or underflows according to the the direction of the count. EXF2 does not generate any interrupt. This bit can be used to provide 17-bit resolution

Figure 8-1. Auto-Reload Mode Up/Down Counter (DCEN = 1)



8.1.1 Programmable Clock-Output

In the clock-out mode, timer 2 operates as a 50%-duty-cycle, programmable clock generator (See Figure 8-2) . The input clock increments TL2 at frequency $F_{OSC}/2$. The timer repeatedly counts to overflow from a loaded value. At overflow, the contents of RCAP2H and RCAP2L registers are loaded into TH2 and TL2. In this mode, timer 2 overflows do not generate interrupts. The formula gives the clock-out frequency as a function of the system oscillator frequency and the value in the RCAP2H and RCAP2L registers :

$$Clock-OutFrequency = \frac{F_{osc}}{4 \times (65536 - RCAP2H/RCAP2L)}$$

For a 16 MHz system clock, timer 2 has a programmable frequency range of 61 Hz ($F_{OSC}/2^{16)}$ to 4 MHz ($F_{OSC}/4$). The generated clock signal is brought out to T2 pin (P1.0).

Timer 2 is programmed for the clock-out mode as follows:

- Set T2OE bit in T2MOD register.
- Clear C/$\overline{T2}$ bit in T2CON register.
- Determine the 16-bit reload value from the formula and enter it in RCAP2H/RCAP2L registers.

- Enter a 16-bit initial value in timer registers TH2/TL2. It can be the same as the reload value or a different one depending on the application.
- To start the timer, set TR2 run control bit in T2CON register.

It is possible to use timer 2 as a baud rate generator and a clock generator simultaneously. For this configuration, the baud rates and clock frequencies are not independent since both functions use the values in the RCAP2H and RCAP2L registers.

Figure 8-2. Clock-Out Mode C/$\overline{T2}$ = 0

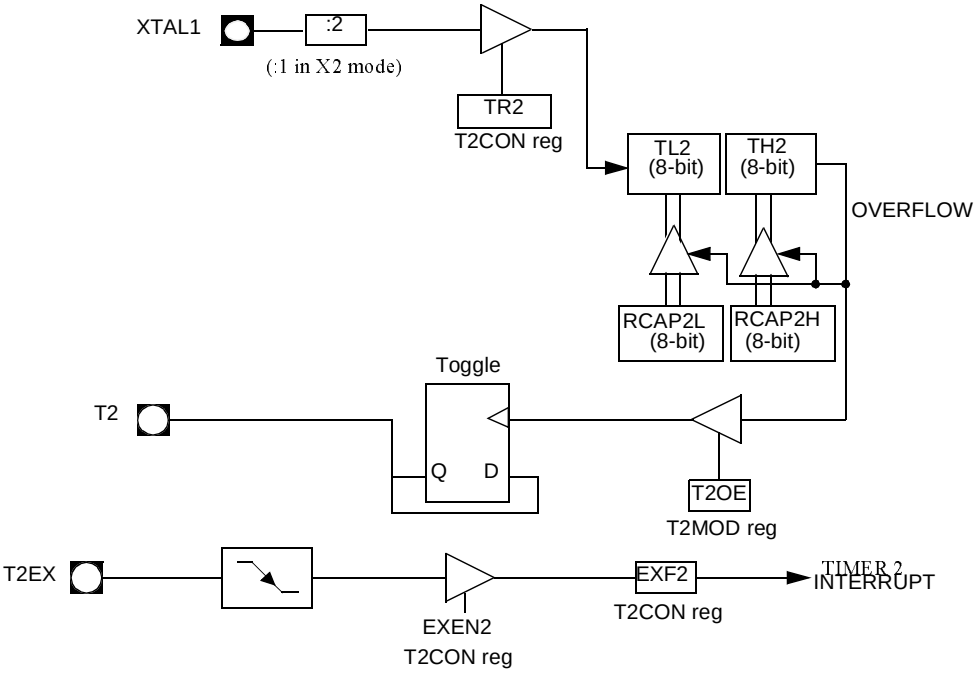


Table 8-1. T2CON Register

T2CON - Timer 2 Control Register (C8h)

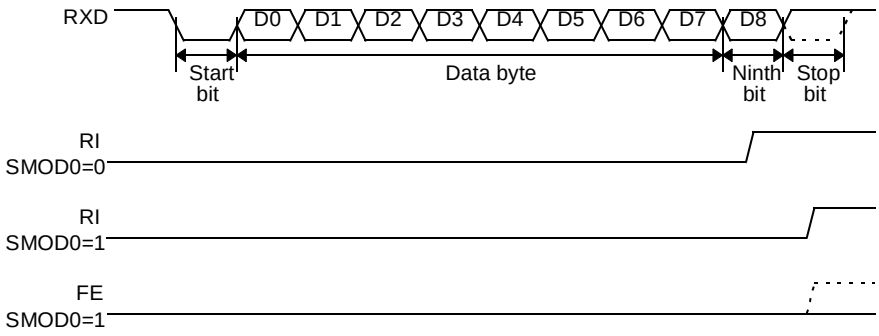
7	6	5	4	3	2	1	0
TF2	**EXF2**	**RCLK**	**TCLK**	**EXEN2**	**TR2**	**C/T2#**	**CP/RL2#**

Bit Number	Bit Mnemonic	Description
7	TF2	**Timer 2 overflow Flag** Must be cleared by software. Set by hardware on timer 2 overflow, if RCLK = 0 and TCLK = 0.
6	EXF2	Timer 2 External Flag Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. When set, causes the CPU to vector to timer 2 interrupt routine when timer 2 interrupt is enabled. Must be cleared by software. EXF2 doesn't cause an interrupt in Up/down counter mode (DCEN = 1)
5	RCLK	Receive Clock bit Clear to use timer 1 overflow as receive clock for serial port in mode 1 or 3. Set to use timer 2 overflow as receive clock for serial port in mode 1 or 3.
4	TCLK	Transmit Clock bit Clear to use timer 1 overflow as transmit clock for serial port in mode 1 or 3. Set to use timer 2 overflow as transmit clock for serial port in mode 1 or 3.
3	EXEN2	Timer 2 External Enable bit Clear to ignore events on T2EX pin for timer 2 operation. Set to cause a capture or reload when a negative transition on T2EX pin is detected, if timer 2 is not used to clock the serial port.
2	TR2	Timer 2 Run control bit Clear to turn off timer 2. Set to turn on timer 2.
1	C/T2#	**Timer/Counter 2 select bit** Clear for timer operation (input from internal clock system: F_{OSC}). Set for counter operation (input from T2 input pin, falling edge trigger). Must be 0 for clock out mode.
0	CP/RL2#	Timer 2 Capture/Reload bit If RCLK=1 or TCLK=1, CP/RL2# is ignored and timer is forced to auto-reload on timer 2 overflow. Clear to auto-reload on timer 2 overflows or negative transitions on T2EX pin if EXEN2=1. Set to capture on negative transitions on T2EX pin if EXEN2=1.

Reset Value = 0000 0000b

Bit addressable

Figure 9-3. UART Timings in Modes 2 and 3



9.1.1 Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.

To support automatic address recognition, a device is identified by a given address and a broadcast address.

NOTE: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).

9.1.2 Given Address

Each device has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don't-care bits (defined by zeros) to form the device's given address. The don't-care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed.

To address a device by its individual address, the SADEN mask byte must be `1111 1111b`.

For example:

```
SADDR       0101 0110b
SADEN       1111 1100b
Given       0101 01XXb
```

Table 9-4. PCON Register

Table 9-5. PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	**SMOD0**	**-**	**POF**	**GF1**	**GF0**	**PD**	**IDL**

Bit Number	Bit Mnemonic	Description
7	SMOD1	**Serial port Mode bit 1** Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	**Serial port Mode bit 0** Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	POF	**Power-Off Flag** Clear to recognize next reset type. Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	**Power-Down mode bit** Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	**Idle mode bit** Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b
Not bit addressable

Power-off flag reset value will be 1 only after a power on (cold reset). A warm reset doesn't affect the value of this bit.

11. Idle mode

An instruction that sets PCON.0 causes that to be the last instruction executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer, and Serial Port functions. The CPU status is preserved in its entirely : the Stack Pointer, Program Counter, Program Status Word, Accumulator and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels.

There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bits GF0 and GF1 can be used to give an indication if an interrupt occured during normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

11.1 Power-Down Mode

To save maximum power, a power-down mode can be invoked by software (Refer to Table 9-4., PCON register).

In power-down mode, the oscillator is stopped and the instruction that invoked power-down mode is the last instruction executed. The internal RAM and SFRs retain their value until the power-down mode is terminated. V_{CC} can be lowered to save further power. Either a hardware reset or an external interrupt can cause an exit from power-down. To properly terminate power-down, the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.

Only external interrupts $\overline{INT0}$ and $\overline{INT1}$ are useful to exit from power-down. For that, interrupt must be enabled and configured as level or edge sensitive interrupt input.
Holding the pin low restarts the oscillator but bringing the pin high completes the exit as detailed in Figure 11-1. When both interrupts are enabled, the oscillator restarts as soon as one of the two inputs is held low and power down exit will be completed when the first input will be released. In this case the higher priority interrupt service routine is executed.
Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put TS80C54/58X2 into power-down mode.

14. Power-Off Flag

The power-off flag allows the user to distinguish between a “cold start” reset and a “warm start” reset.

A cold start reset is the one induced by V_{CC} switch-on. A warm start reset occurs while V_{CC} is still applied to the device and could be generated for example by an exit from power-down.

The power-off flag (POF) is located in PCON register (See Table 14-1.). POF is set by hardware when V_{CC} rises from 0 to its nominal voltage. The POF can be set or cleared by software allowing the user to determine the type of reset.

The POF value is only relevant with a Vcc range from 4.5V to 5.5V. For lower Vcc value, reading POF bit will return indeterminate value.

Table 14-1. PCON Register

PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	**SMOD0**	**-**	**POF**	**GF1**	**GF0**	**PD**	**IDL**

Bit Number	Bit Mnemonic	Description
7	SMOD1	**Serial port Mode bit 1** Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	**Serial port Mode bit 0** Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	POF	**Power-Off Flag** Clear to recognize next reset type. Set by hardware when V_{CC} rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	**Power-Down mode bit** Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	**Idle mode bit** Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b
Not bit addressable

15. Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0. As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

Table 15-1. AUXR Register

AUXR - Auxiliary Register (8Eh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	RESERVED	AO

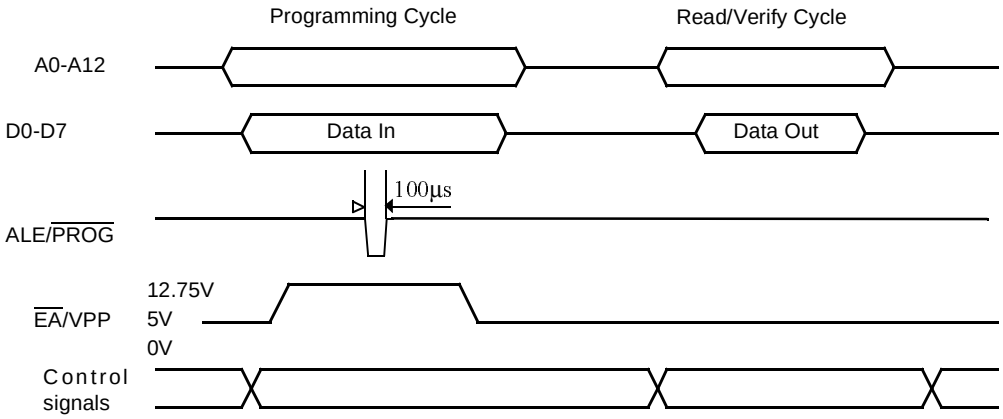
Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	AO	**ALE Output bit** Clear to restore ALE operation during internal fetches. Set to disable ALE operation during internal fetches.

Reset Value = XXXX XXX0b

Not bit addressable

The encryption array cannot be directly verified. Verification of the encryption array is done by observing that the code array is well encrypted.

Figure 17-2. Programming and Verification Signal's Waveform



17.4 EPROM Erasure (Windowed Packages Only)

Erasing the EPROM erases the code array, the encryption array and the lock bits returning the parts to full functionality.

Erasure leaves all the EPROM cells in a 1's state (FF).

17.4.1 Erasure Characteristics

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Å) to an integrated dose at least 15 W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 µW/cm^2 rating for 30 minutes, at a distance of about 25 mm, should be sufficient. An exposure of 1 hour is recommended with most of standard erasers.

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Å. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

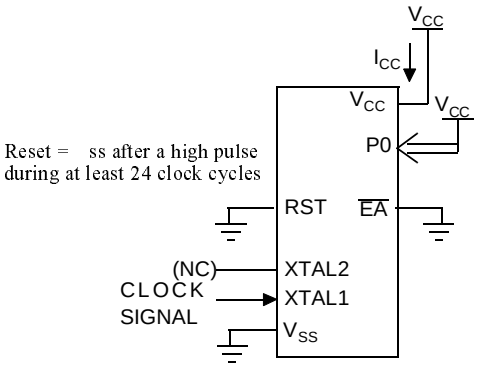
18. Signature Bytes

The TS87C54/58X2 has four signature bytes in location 30h, 31h, 60h and 61h. To read these bytes follow the procedure for EPROM verify but activate the control lines provided in Table 31. for Read Signature Bytes. Table 18-1. shows the content of the signature byte for the TS80C54/58X2.

Table 18-1. Signature Bytes Content

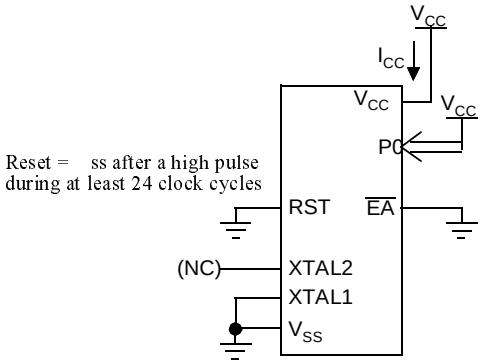
Location	Contents	Comment
30h	58h	Manufacturer Code: Atmel Wireless & Microcontrollers
31h	57h	Family Code: C51 X2
60h	37h	Product name: TS80C58X2
60h	B7h	Product name: TS87C58X2
60h	3Bh	Product name: TS80C54X2
60h	BBh	Product name: TS87C54X2
61h	FFh	Product revision number

Figure 19-3. I_{CC} Test Condition, Idle Mode



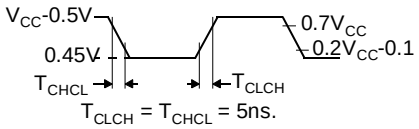
All other pins are disconnected.

Figure 19-4. I_{CC} Test Condition, Power-Down Mode



All other pins are disconnected.

Figure 19-5. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes



19.5.4 External Data Memory Characteristics

Table 19-8. Symbol Description

Symbol	Parameter
T_{RLRH}	$\overline{RD}$ Pulse Width
T_{WLWH}	$\overline{WR}$ Pulse Width
T_{RLDV}	$\overline{RD}$ to Valid Data In
T_{RHDX}	Data Hold After $\overline{RD}$
T_{RHDZ}	Data Float After $\overline{RD}$
T_{LLDV}	ALE to Valid Data In
T_{AVDV}	Address to Valid Data In
T_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$
T_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$
T_{QVWX}	Data Valid to $\overline{WR}$ Transition
T_{QVWH}	Data set-up to $\overline{WR}$ High
T_{WHQX}	Data Hold After $\overline{WR}$
T_{RLAZ}	$\overline{RD}$ Low to Address Float
T_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE high

Table 19-9. AC Parameters for a Fix Clock

Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
T_{RLRH}	130		85		135		125		175		ns
T_{WLWH}	130		85		135		125		175		ns
T_{RLDV}		100		60		102		95		137	ns
T_{RHDX}	0		0		0		0		0		ns
T_{RHDZ}		30		18		35		25		42	ns
T_{LLDV}		160		98		165		155		222	ns
T_{AVDV}		165		100		175		160		235	ns
T_{LLWL}	50	100	30	70	55	95	45	105	70	130	ns
T_{AVWL}	75		47		80		70		103		ns
T_{QVWX}	10		7		15		5		13		ns
T_{QVWH}	160		107		165		155		213		ns
T_{WHQX}	15		9		17		10		18		ns
T_{RLAZ}		0		0		0		0		0	ns
T_{WHLH}	10	40	7	27	15	35	5	45	13	53	ns

Table 19-10. AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
T_{RLRH}	Min	6 T - x	3 T - x	20	15	25	ns
T_{WLWH}	Min	6 T - x	3 T - x	20	15	25	ns
T_{RLDV}	Max	5 T - x	2.5 T - x	25	23	30	ns
T_{RHDX}	Min	x	x	0	0	0	ns
T_{RHDZ}	Max	2 T - x	T - x	20	15	25	ns
T_{LLDV}	Max	8 T - x	4T -x	40	35	45	ns
T_{AVDV}	Max	9 T - x	4.5 T - x	60	50	65	ns
T_{LLWL}	Min	3 T - x	1.5 T - x	25	20	30	ns
T_{LLWL}	Max	3 T + x	1.5 T + x	25	20	30	ns
T_{AVWL}	Min	4 T - x	2 T - x	25	20	30	ns
T_{QVWX}	Min	T - x	0.5 T - x	15	10	20	ns
T_{QVWH}	Min	7 T - x	3.5 T - x	15	10	20	ns
T_{WHQX}	Min	T - x	0.5 T - x	10	8	15	ns
T_{RLAZ}	Max	x	x	0	0	0	ns
T_{WHLH}	Min	T - x	0.5 T - x	15	10	20	ns
T_{WHLH}	Max	T + x	0.5 T + x	15	10	20	ns

19.5.5 External Data Memory Write Cycle

Figure 19-7. External Data Memory Write Cycle

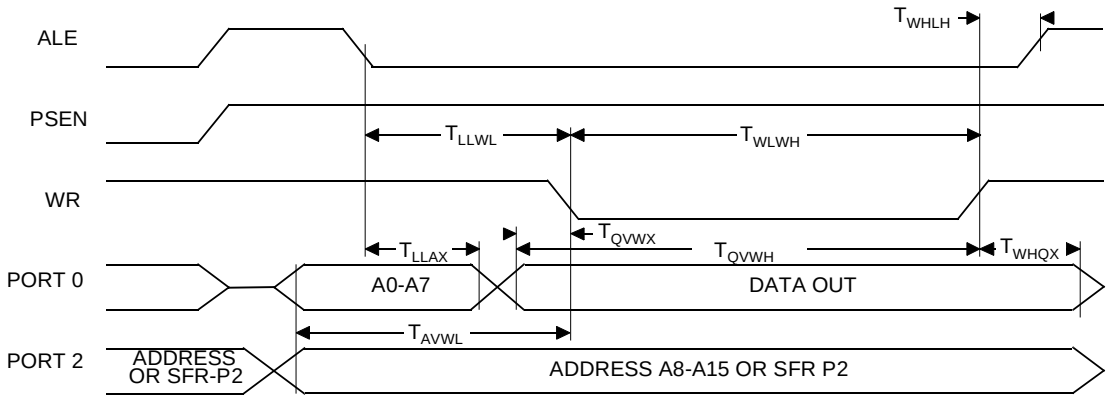
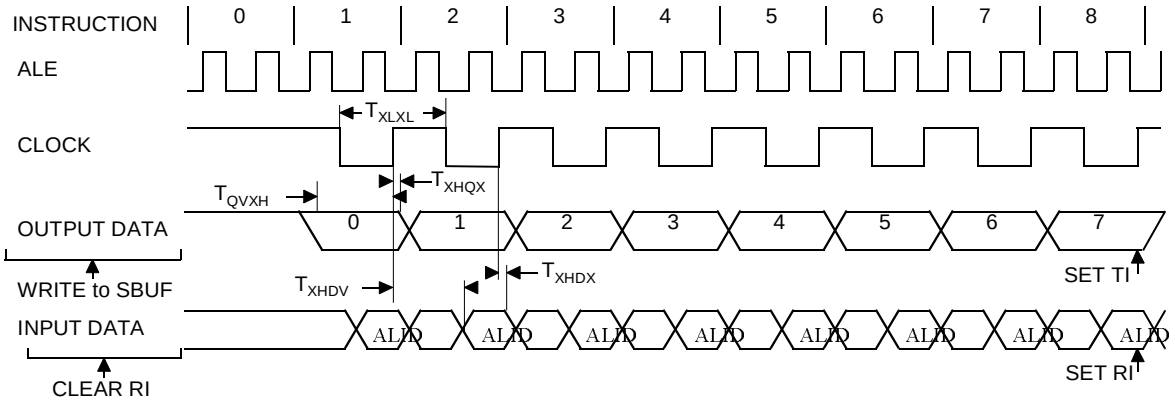


Table 19-13. AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
T_{XLXL}	Min	12 T	6 T				ns
T_{QVHX}	Min	10 T - x	5 T - x	50	50	50	ns
T_{XHQX}	Min	2 T - x	T - x	20	20	20	ns
T_{XHDX}	Min	x	x	0	0	0	ns
T_{XHDV}	Max	10 T - x	5 T- x	133	133	133	ns

19.5.8 Shift Register Timing Waveforms

Figure 19-9. Shift Register Timing Waveforms



Part Number	Supply Voltage	Temperature Range	Package	Packing
TS87C58X2-MCE	5V ±10%	Commercial	VQFP44	Tray
TS87C58X2-VCA	5V ±10%	Commercial	PDIL40	Stick
TS87C58X2-VCB	5V ±10%	Commercial	PLCC44	Stick
TS87C58X2-VCC	5V ±10%	Commercial	PQFP44	Tray
TS87C58X2-VCE	5V ±10%	Commercial	VQFP44	Tray
TS87C58X2-LCA	2.7 to 5.5V	Commercial	PDIL40	Stick
TS87C58X2-LCB	2.7 to 5.5V	Commercial	PLCC44	Stick
TS87C58X2-LCC	2.7 to 5.5V	Commercial	PQFP44	Tray
TS87C58X2-LCE	2.7 to 5.5V	Commercial	VQFP44	Tray
TS87C58X2-MIA	5V ±10%	Industrial	PDIL40	Stick
TS87C58X2-MIB	5V ±10%	Industrial	PLCC44	Stick
TS87C58X2-MIC	5V ±10%	Industrial	PQFP44	Tray
TS87C58X2-MIE	5V ±10%	Industrial	VQFP44	Tray
TS87C58X2-VIA	5V ±10%	Industrial	PDIL40	Stick
TS87C58X2-VIB	5V ±10%	Industrial	PLCC44	Stick
TS87C58X2-VIC	5V ±10%	Industrial	PQFP44	Tray
TS87C58X2-VIE	5V ±10%	Industrial	VQFP44	Tray
TS87C58X2-LIA	2.7 to 5.5V	Industrial	PDIL40	Stick
TS87C58X2-LIB	2.7 to 5.5V	Industrial	PLCC44	Stick
TS87C58X2-LIC	2.7 to 5.5V	Industrial	PQFP44	Tray
TS87C58X2-LIE	2.7 to 5.5V	Industrial	VQFP44	Tray
AT87C58X2-3CSUM	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUM	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUM	5V ±10%	Industrial & Green	VQFP44	Tray
AT87C58X2-3CSUL	2.7 to 5.5V	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUL	2.7 to 5.5V	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUL	2.7 to 5.5V	Industrial & Green	VQFP44	Tray
AT87C58X2-3CSUV	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUV	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUV	5V ±10%	Industrial & Green	VQFP44	Tray

21. Datasheet Revision History

21.1 Changes from Rev. C 01/01 to Rev. D 11/05

1. Added green product Ordering Information.

21.2 Changes from Rev. D 11/05 to Rev. E 04/06

1. Changed value of AUXR register.

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