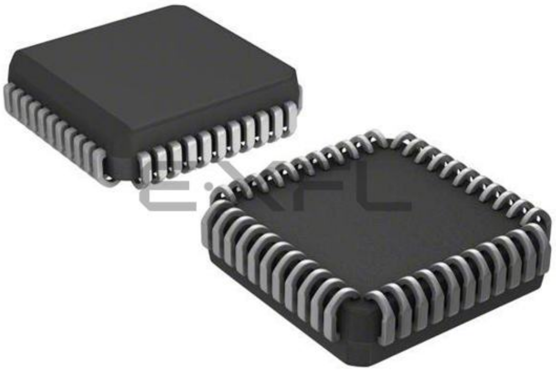

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | 80C51 |
| Core Size | 8-Bit |
| Speed | 30/20MHz |
| Connectivity | UART/USART |
| Peripherals | POR, WDT |
| Number of I/O | 32 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LCC (J-Lead) |
| Supplier Device Package | 44-PLCC (16.6x16.6) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/ts87c54x2-lib |

# 6. TS80C54/58X2 Enhanced Features

In comparison to the original 80C52, the TS80C54/58X2 implements some new features, which are:

- The X2 option.
- The Dual Data Pointer.
- The Watchdog.
- The 4 level interrupt priority system.
- The power-off flag.
- The ONCE mode.
- The ALE disabling.
- Some enhanced features are also located in the UART and the timer 2.

## 6.1 X2 Feature

The TS80C54/58X2 core needs only 6 clock periods per machine cycle. This feature called ”X2” provides the following advantages:

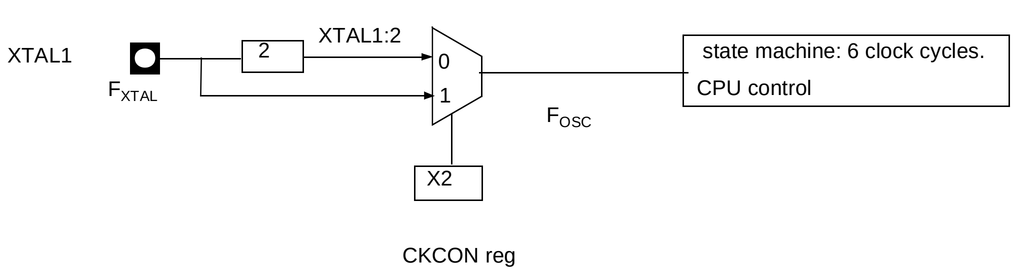
- Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power.
- Save power consumption while keeping same CPU power (oscillator power saving).
- Save power consumption by dividing dynamically operating frequency by 2 in operating and idle modes.
- Increase CPU power by 2 while keeping same crystal frequency.

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

### 6.1.1 Description

The clock for the whole circuit and peripheral is first divided by two before being used by the CPU core and peripherals. This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%. Figure 6-2. shows the clock generation block diagram. X2 bit is validated on XTAL1÷2 rising edge to avoid glitches when switching from X2 to STD mode. Figure 6-2. shows the mode switching waveforms.

**Figure 6-1.** Clock Generation Diagram

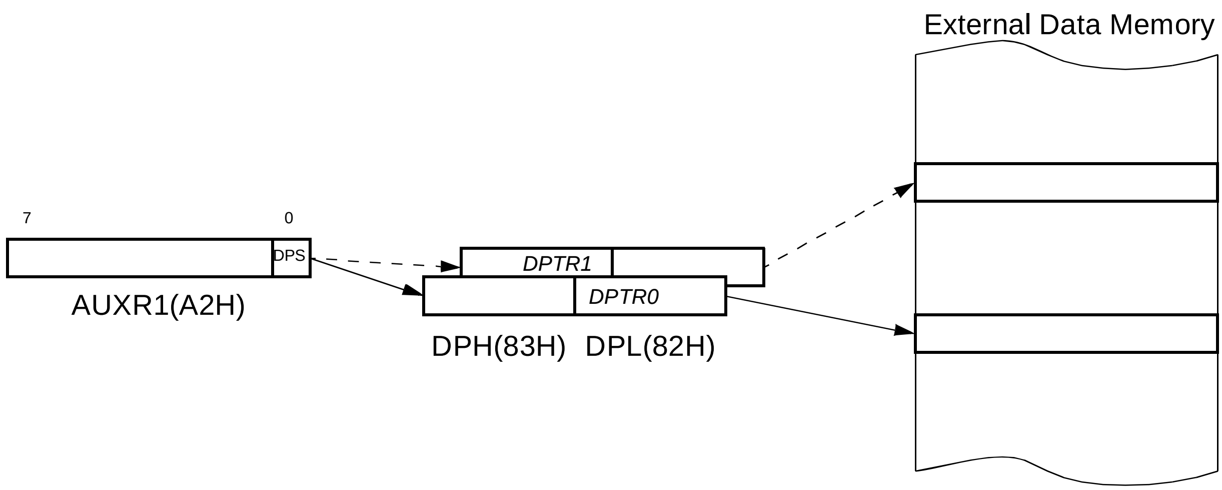


# 7. Dual Data Pointer Register Ddptr

The additional data pointer can be used to speed up code execution and reduce code size in a number of ways.

The dual DPTR structure is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called
DPS = AUXR1/bit0 (See Table 7-1.) that allows the program code to switch between them (Refer to Figure 7-1).

**Figure 7-1.** Use of Dual Pointer



# 8. Timer 2

The timer 2 in the TS80C54/58X2 is compatible with the timer 2 in the 80C52.
It is a 16-bit timer/counter: the count is maintained by two eight-bit timer registers, TH2 and TL2, connected in cascade. It is controlled by T2CON register (See Table 8-1) and T2MOD register (See Table 8-2). Timer 2 operation is similar to Timer 0 and Timer 1. $C/\overline{T2}$ selects $F_{OSC}/12$ (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows TL2 to be incremented by the selected input.

Timer 2 has 3 operating modes: capture, autoreload and Baud Rate Generator. These modes are selected by the combination of RCLK, TCLK and $CP/\overline{RL2}$ (T2CON), as described in the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description.

Refer to the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description for the description of Capture and Baud Rate Generator Modes.

In TS80C54/58X2 Timer 2 includes the following enhancements:

- Auto-reload mode with up or down counter
- Programmable clock-output

## 8.1 Auto-Reload Mode

The auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. If DCEN bit in T2MOD is cleared, timer 2 behaves as in 80C52 (refer to the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description). If DCEN bit is set, timer 2 acts as an Up/down timer/counter as shown in Figure 8-1. In this mode the T2EX pin controls the direction of count.

When T2EX is high, timer 2 counts up. Timer overflow occurs at FFFFh which sets the TF2 flag and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L registers to be loaded into the timer registers TH2 and TL2.

When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers TH2 and TL2 equals the value stored in RCAP2H and RCAP2L registers. The underflow sets TF2 flag and reloads FFFFh into the timer registers.

The EXF2 bit toggles when timer 2 overflows or underflows according to the the direction of the count. EXF2 does not generate any interrupt. This bit can be used to provide 17-bit resolution

**Table 8-2.** T2MOD Register

T2MOD - Timer 2 Mode Control Register (C9h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | - | - | - | - | - | T2OE | DCEN |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 6 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 5 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 4 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 3 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 2 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 1 | T2OE | **Timer 2 Output Enable bit**<br>Clear to program P1.0/T2 as clock input or I/O port.<br>Set to program P1.0/T2 as clock output. |
| 0 | DCEN | **Down Counter Enable bit**<br>Clear to disable timer 2 as up/down counter.<br>Set to enable timer 2 as up/down counter. |

Reset Value = XXXX XX00b

Not bit addressable

# 9. TS80C54/58X2 Serial I/O Port

The serial I/O port in the TS80C54/58X2 is compatible with the serial I/O port in the 80C52.
It provides both synchronous and asynchronous communication modes. It operates as an Universal Asynchronous Receiver and Transmitter (UART) in three full-duplex modes (Modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates

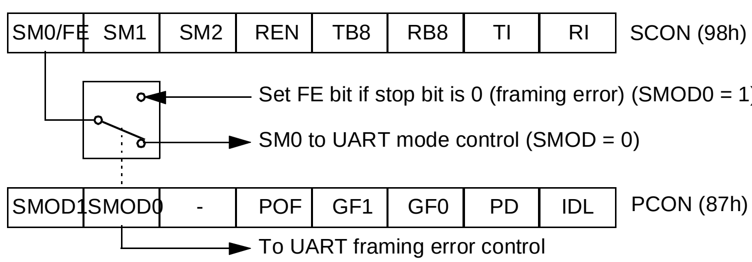
Serial I/O port includes the following enhancements:

- Framing error detection
- Automatic address recognition

## 9.1 Framing Error Detection

Framing bit error detection is provided for the three asynchronous modes (modes 1, 2 and 3). To enable the framing bit error detection feature, set SMOD0 bit in PCON register (See Figure 9-1).

**Figure 9-1.** Framing Error Block Diagram




When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two CPUs. If a valid stop bit is not found, the Framing Error bit (FE) in SCON register (See Table 9-3.) bit is set.
Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset can clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 9-2. and Figure 9-3.).

**Figure 9-2.** UART Timings in Mode 1

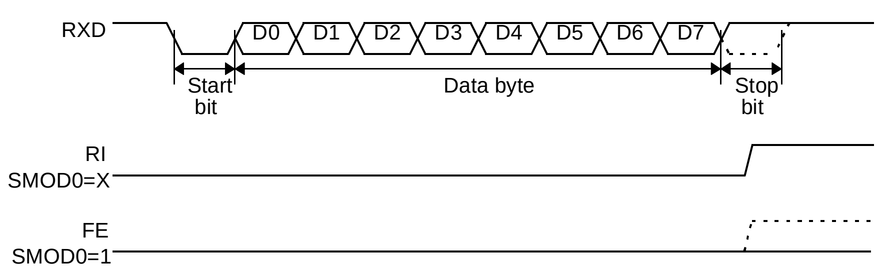
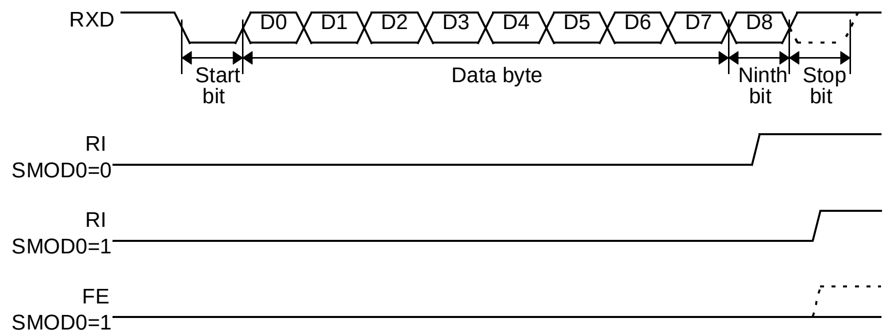


**Figure 9-3.** UART Timings in Modes 2 and 3




### 9.1.1 Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.

To support automatic address recognition, a device is identified by a given address and a broadcast address.

NOTE: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).

### 9.1.2 Given Address

Each device has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don't-care bits (defined by zeros) to form the device's given address. The don't-care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed.

To address a device by its individual address, the SADEN mask byte must be `1111 1111b`.

For example:

```
SADDR   0101 0110b
SADEN   1111 1100b
Given   0101 01XXb
```

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

**Table 10-2.** IE Register

IE - Interrupt Enable Register (A8h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| EA | - | ET2 | ES | ET1 | EX1 | ET0 | EX0 |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | EA | Enable All interrupt bit<br>Clear to disable all interrupts.<br>Set to enable all interrupts.<br>If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its own interrupt enable bit. |
| 6 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 5 | ET2 | Timer 2 overflow interrupt Enable bit<br>Clear to disable timer 2 overflow interrupt.<br>Set to enable timer 2 overflow interrupt. |
| 4 | ES | Serial port Enable bit<br>Clear to disable serial port interrupt.<br>Set to enable serial port interrupt. |
| 3 | ET1 | Timer 1 overflow interrupt Enable bit<br>Clear to disable timer 1 overflow interrupt.<br>Set to enable timer 1 overflow interrupt. |
| 2 | EX1 | External interrupt 1 Enable bit<br>Clear to disable external interrupt 1.<br>Set to enable external interrupt 1. |
| 1 | ET0 | Timer 0 overflow interrupt Enable bit<br>Clear to disable timer 0 overflow interrupt.<br>Set to enable timer 0 overflow interrupt. |
| 0 | EX0 | External interrupt 0 Enable bit<br>Clear to disable external interrupt 0.<br>Set to enable external interrupt 0. |

Reset Value = 0X00 0000b

Bit addressable

## 14. Power-Off Flag

The power-off flag allows the user to distinguish between a “cold start” reset and a “warm start” reset.

A cold start reset is the one induced by $V_{CC}$ switch-on. A warm start reset occurs while $V_{CC}$ is still applied to the device and could be generated for example by an exit from power-down.

The power-off flag (POF) is located in PCON register (See Table 14-1.). POF is set by hardware when $V_{CC}$ rises from 0 to its nominal voltage. The POF can be set or cleared by software allowing the user to determine the type of reset.

The POF value is only relevant with a Vcc range from 4.5V to 5.5V. For lower Vcc value, reading POF bit will return indeterminate value.

**Table 14-1.** PCON Register

PCON - Power Control Register (87h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **SMOD1** | **SMOD0** | **-** | **POF** | **GF1** | **GF0** | **PD** | **IDL** |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | SMOD1 | **Serial port Mode bit 1**<br>Set to select double baud rate in mode 1, 2 or 3. |
| 6 | SMOD0 | **Serial port Mode bit 0**<br>Clear to select SM0 bit in SCON register.<br>Set to to select FE bit in SCON register. |
| 5 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 4 | POF | **Power-Off Flag**<br>Clear to recognize next reset type.<br>Set by hardware when $V_{CC}$ rises from 0 to its nominal voltage. Can also be set by software. |
| 3 | GF1 | **General purpose Flag**<br>Cleared by user for general purpose usage.<br>Set by user for general purpose usage. |
| 2 | GF0 | **General purpose Flag**<br>Cleared by user for general purpose usage.<br>Set by user for general purpose usage. |
| 1 | PD | **Power-Down mode bit**<br>Cleared by hardware when reset occurs.<br>Set to enter power-down mode. |
| 0 | IDL | **Idle mode bit**<br>Clear by hardware when interrupt or reset occurs.<br>Set to enter idle mode. |

Reset Value = 00X1 0000b
Not bit addressable

## 15. Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0. As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

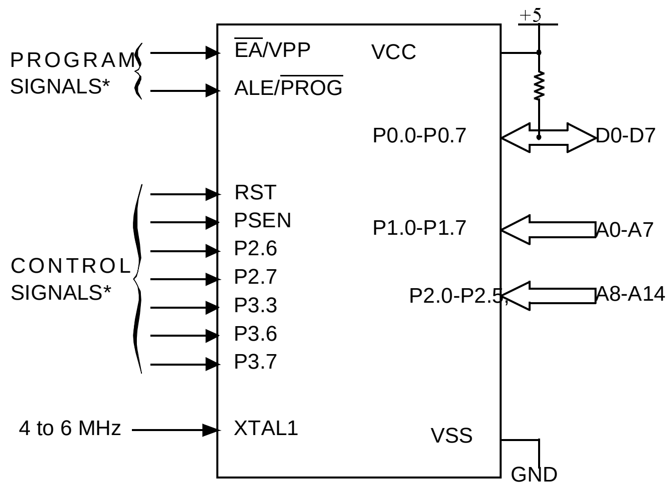
**Table 15-1.** AUXR Register
AUXR - Auxiliary Register (8Eh)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | - | - | - | - | - | RESERVED | AO |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 6 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 5 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 4 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 3 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 2 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 1 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 0 | AO | **ALE Output bit**<br>Clear to restore ALE operation during internal fetches.<br>Set to disable ALE operation during internal fetches. |

Reset Value = XXXX XXX0b
Not bit addressable

**Figure 17-1.** Set-Up Modes Configuration




* See Table 31. for proper value on these inputs

### 17.3.3 Programming Algorithm

The Improved Quick Pulse algorithm is based on the Quick Pulse algorithm and decreases the number of pulses applied during byte programming from 25 to 1.

To program the TS80C54/58X2 the following sequence must be exercised:

- Step 1: Activate the combination of control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Input the appropriate data on the data lines.
- Step 4: Raise $\overline{\text{EA}}$/VPP from VCC to VPP (typical 12.75V).
- Step 5: Pulse ALE/$\overline{\text{PROG}}$ once.
- Step 6: Lower $\overline{\text{EA}}$/VPP from VPP to VCC

Repeat step 2 through 6 changing the address and data for the entire array or until the end of the object file is reached (See Figure 17-2.).

### 17.3.4 Verify algorithm

Code array verify must be done after each byte or block of bytes is programmed. In either case, a complete verify of the programmed array will ensure reliable programming of the TS87C54/58X2.

P 2.7 is used to enable data output.

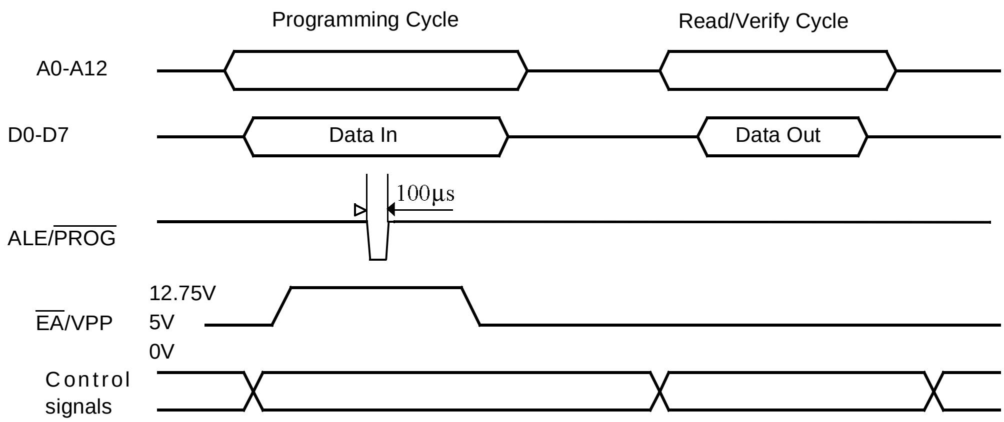
To verify the TS87C54/58X2 code the following sequence must be exercised:

- Step 1: Activate the combination of program and control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Read data on the data lines.

Repeat step 2 through 3 changing the address for the entire array verification (See Figure 17-2.)

The encryption array cannot be directly verified. Verification of the encryption array is done by observing that the code array is well encrypted.

**Figure 17-2.** Programming and Verification Signal's Waveform




## 17.4 EPROM Erasure (Windowed Packages Only)

Erasing the EPROM erases the code array, the encryption array and the lock bits returning the parts to full functionality.

Erasure leaves all the EPROM cells in a 1's state (FF).

### 17.4.1 Erasure Characteristics

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Å) to an integrated dose at least 15 W-sec/cm$^2$. Exposing the EPROM to an ultraviolet lamp of 12,000 $\mu$W/cm$^2$ rating for 30 minutes, at a distance of about 25 mm, should be sufficient. An exposure of 1 hour is recommended with most of standard erasers.

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Å. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

# 18. Signature Bytes

The TS87C54/58X2 has four signature bytes in location 30h, 31h, 60h and 61h. To read these bytes follow the procedure for EPROM verify but activate the control lines provided in Table 31. for Read Signature Bytes. Table 18-1. shows the content of the signature byte for the TS80C54/58X2.

**Table 18-1.** Signature Bytes Content

| Location | Contents | Comment |
|---|---|---|
| 30h | 58h | Manufacturer Code: Atmel Wireless & Microcontrollers |
| 31h | 57h | Family Code: C51 X2 |
| 60h | 37h | Product name: TS80C58X2 |
| 60h | B7h | Product name: TS87C58X2 |
| 60h | 3Bh | Product name: TS80C54X2 |
| 60h | BBh | Product name: TS87C54X2 |
| 61h | FFh | Product revision number |

## 19.4 DC Parameters for Low Voltage

$T_A = 0°C$ to $+70°C$; $V_{SS} = 0$ V; $V_{CC} = 2.7$ V to $5.5$ V $\pm$ 10%; F = 0 to 30 MHz.
$T_A = -40°C$ to $+85°C$; $V_{SS} = 0$ V; $V_{CC} = 2.7$ V to $5.5$ V $\pm$ 10%; F = 0 to 30 MHz.

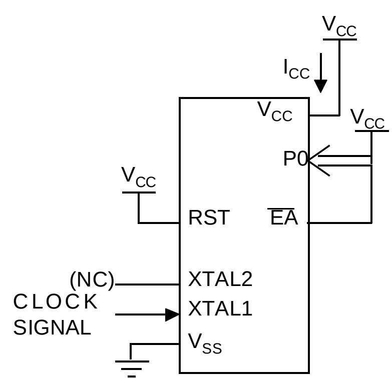
**Table 19-2.** DC Parameters for Low Voltage

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | -0.5 | | $0.2\ V_{CC} - 0.1$ | V | |
| $V_{IH}$ | Input High Voltage except XTAL1, RST | $0.2\ V_{CC} + 0.9$ | | $V_{CC} + 0.5$ | V | |
| $V_{IH1}$ | Input High Voltage, XTAL1, RST | $0.7\ V_{CC}$ | | $V_{CC} + 0.5$ | V | |
| $V_{OL}$ | Output Low Voltage, ports 1, 2, 3 (6) | | | 0.45 | V | $I_{OL} = 0.8$ mA(4) |
| $V_{OL1}$ | Output Low Voltage, port 0, ALE, $\overline{PSEN}$ (6) | | | 0.45 | V | $I_{OL} = 1.6$ mA(4) |
| $V_{OH}$ | Output High Voltage, ports 1, 2, 3 | $0.9\ V_{CC}$ | | | V | $I_{OH} = -10\ \mu A$ |
| $V_{OH1}$ | Output High Voltage, port 0, ALE, $\overline{PSEN}$ | $0.9\ V_{CC}$ | | | V | $I_{OH} = -40\ \mu A$ |
| $I_{IL}$ | Logical 0 Input Current ports 1, 2 and 3 | | | -50 | µA | Vin = 0.45 V |
| $I_{LI}$ | Input Leakage Current | | | ±10 | µA | 0.45 V < Vin < $V_{CC}$ |
| $I_{TL}$ | Logical 1 to 0 Transition Current, ports 1, 2, 3 | | | -650 | µA | Vin = 2.0 V |
| $R_{RST}$ | RST Pulldown Resistor | 50 | 90 (5) | 200 | kΩ | |
| CIO | Capacitance of I/O Buffer | | | 10 | pF | Fc = 1 MHz<br>$T_A = 25°C$ |
| $I_{PD}$ | Power Down Current | | 20 (5)<br>10 (5) | 50<br>30 | µA | $V_{CC} = 2.0$ V to 5.5 V(3)<br>$V_{CC} = 2.0$ V to 3.3 V(3) |
| $I_{CC}$ under RESET | Power Supply Current Maximum values, X1 mode: (7) | | | 1 + 0.2 Freq (MHz)<br>@12MHz 3.4<br>@16MHz 4.2 | mA | $V_{CC} = 3.3$ V(1) |
| $I_{CC}$ operating | Power Supply Current Maximum values, X1 mode: (7) | | | 1 + 0.3 Freq (MHz)<br>@12MHz 4.6<br>@16MHz 5.8 | mA | $V_{CC} = 3.3$ V(8) |
| $I_{CC}$ idle | Power Supply Current Maximum values, X1 mode: (7) | | | 0.15 Freq (MHz) + 0.2<br>@12MHz 2<br>@16MHz 2.6 | mA | $V_{CC} = 3.3$ V(2) |

1. $I_{CC}$ under reset is measured with all output pins disconnected; XTAL1 driven with $T_{CLCH}$, $T_{CHCL}$ = 5 ns (see Figure 19-5.), $V_{IL} = V_{SS} + 0.5$ V, $V_{IH} = V_{CC} - 0.5$V; XTAL2 N.C.; $\overline{EA}$ = RST = Port 0 = $V_{CC}$. $I_{CC}$ would be slightly higher if a crystal oscillator used..
2. Idle $I_{CC}$ is measured with all output pins disconnected; XTAL1 driven with $T_{CLCH}$, $T_{CHCL}$ = 5 ns, $V_{IL} = V_{SS} + 0.5$ V, $V_{IH} = V_{CC} - 0.5$ V; XTAL2 N.C; Port 0 = $V_{CC}$; $\overline{EA}$ = RST = $V_{SS}$ (see Figure 19-3.).
3. Power Down $I_{CC}$ is measured with all output pins disconnected; $\overline{EA} = V_{SS}$, PORT 0 = $V_{CC}$; XTAL2 NC.; RST = $V_{SS}$ (see Figure 19-4.).
4. Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the $V_{OL}$s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100pF), the noise pulse on the ALE line may exceed 0.45V with maxi $V_{OL}$ peak 0.6V. A Schmitt Trigger use is not necessary.

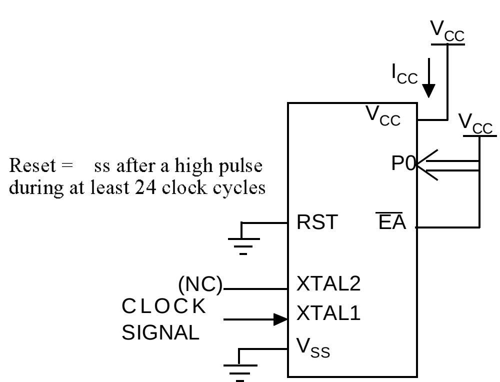
5. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
6. Under steady state (non-transient) conditions, $I_{OL}$ must be externally limited as follows:
   Maximum $I_{OL}$ per port pin: 10 mA
   Maximum $I_{OL}$ per 8-bit port:
   Port 0: 26 mA
   Ports 1, 2 and 3: 15 mA
   Maximum total $I_{OL}$ for all output pins: 71 mA
   If $I_{OL}$ exceeds the test condition, $V_{OL}$ may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
7. For other values, please contact your sales office.
8. Operating $I_{CC}$ is measured with all output pins disconnected; XTAL1 driven with $T_{CLCH}$, $T_{CHCL}$ = 5 ns (see Figure 19-5.), $V_{IL} = V_{SS} + 0.5$ V,
   $V_{IH} = V_{CC}$ - 0.5V; XTAL2 N.C.; $\overline{EA}$ = Port 0 = $V_{CC}$; RST = $V_{SS}$. The internal ROM runs the code 80 FE (label: SJMP label). $I_{CC}$ would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.

**Figure 19-1.** $I_{CC}$ Test Condition, under reset




All other pins are disconnected.

**Figure 19-2.** Operating $I_{CC}$ Test Condition




All other pins are disconnected.

**Table 19-7.** AC Parameters for a Variable Clock: derating formula

| Symbol | Type | Standard Clock | X2 Clock | -M | -V | -L | Units |
|---|---|---|---|---|---|---|---|
| $T_{LHLL}$ | Min | 2 T - x | T - x | 10 | 8 | 15 | ns |
| $T_{AVLL}$ | Min | T - x | 0.5 T - x | 15 | 13 | 20 | ns |
| $T_{LLAX}$ | Min | T - x | 0.5 T - x | 15 | 13 | 20 | ns |
| $T_{LLIV}$ | Max | 4 T - x | 2 T - x | 30 | 22 | 35 | ns |
| $T_{LLPL}$ | Min | T - x | 0.5 T - x | 10 | 8 | 15 | ns |
| $T_{PLPH}$ | Min | 3 T - x | 1.5 T - x | 20 | 15 | 25 | ns |
| $T_{PLIV}$ | Max | 3 T - x | 1.5 T - x | 40 | 25 | 45 | ns |
| $T_{PXIX}$ | Min | x | x | 0 | 0 | 0 | ns |
| $T_{PXIZ}$ | Max | T - x | 0.5 T - x | 7 | 5 | 15 | ns |
| $T_{AVIV}$ | Max | 5 T - x | 2.5 T - x | 40 | 30 | 45 | ns |
| $T_{PLAZ}$ | Max | x | x | 10 | 10 | 10 | ns |

### 19.5.3 External Program Memory Read Cycle

**Figure 19-6.** External Program Memory Read Cycle

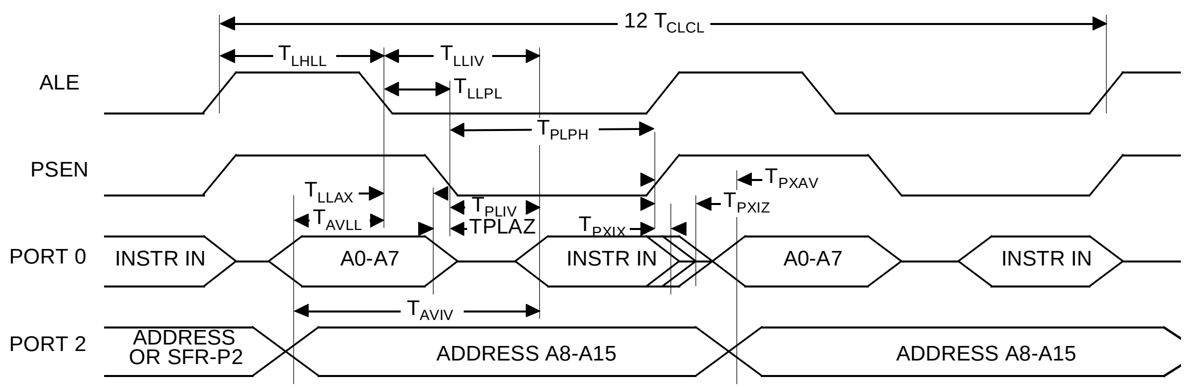
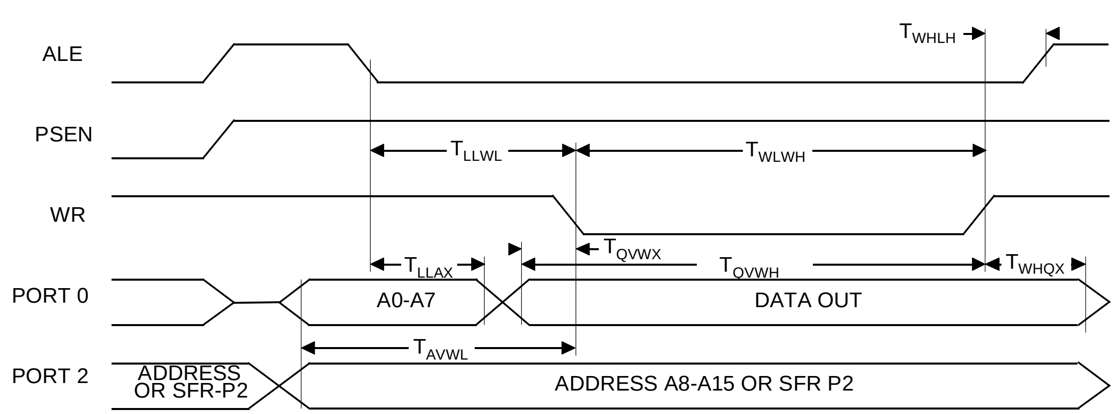


**Table 19-10.** AC Parameters for a Variable Clock: derating formula

| Symbol | Type | Standard Clock | X2 Clock | -M | -V | -L | Units |
|---|---|---|---|---|---|---|---|
| $T_{RLRH}$ | Min | 6 T - x | 3 T - x | 20 | 15 | 25 | ns |
| $T_{WLWH}$ | Min | 6 T - x | 3 T - x | 20 | 15 | 25 | ns |
| $T_{RLDV}$ | Max | 5 T - x | 2.5 T - x | 25 | 23 | 30 | ns |
| $T_{RHDX}$ | Min | x | x | 0 | 0 | 0 | ns |
| $T_{RHDZ}$ | Max | 2 T - x | T - x | 20 | 15 | 25 | ns |
| $T_{LLDV}$ | Max | 8 T - x | 4T -x | 40 | 35 | 45 | ns |
| $T_{AVDV}$ | Max | 9 T - x | 4.5 T - x | 60 | 50 | 65 | ns |
| $T_{LLWL}$ | Min | 3 T - x | 1.5 T - x | 25 | 20 | 30 | ns |
| $T_{LLWL}$ | Max | 3 T + x | 1.5 T + x | 25 | 20 | 30 | ns |
| $T_{AVWL}$ | Min | 4 T - x | 2 T - x | 25 | 20 | 30 | ns |
| $T_{QVWX}$ | Min | T - x | 0.5 T - x | 15 | 10 | 20 | ns |
| $T_{QVWH}$ | Min | 7 T - x | 3.5 T - x | 15 | 10 | 20 | ns |
| $T_{WHQX}$ | Min | T - x | 0.5 T - x | 10 | 8 | 15 | ns |
| $T_{RLAZ}$ | Max | x | x | 0 | 0 | 0 | ns |
| $T_{WHLH}$ | Min | T - x | 0.5 T - x | 15 | 10 | 20 | ns |
| $T_{WHLH}$ | Max | T + x | 0.5 T + x | 15 | 10 | 20 | ns |

### 19.5.5 External Data Memory Write Cycle

**Figure 19-7.** External Data Memory Write Cycle



### 19.5.9 EPROM Programming and Verification Characteristics

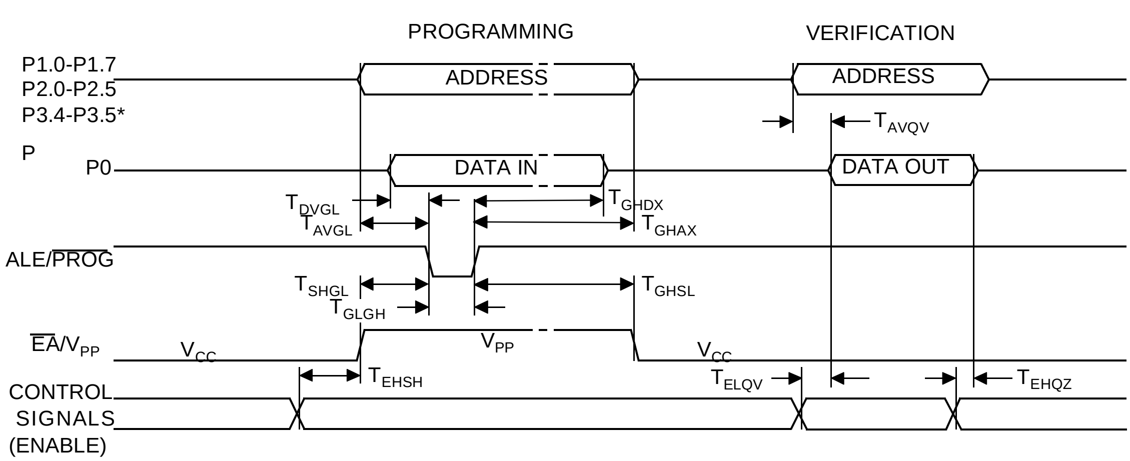
$T_A$ = 21°C to 27°C; $V_{SS}$ = 0V; $V_{CC}$ = 5V ± 10% while programming. $V_{CC}$ = operating range while verifying.

**Table 19-14.** EPROM Programming Parameters

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $V_{PP}$ | Programming Supply Voltage | 12.5 | 13 | V |
| $I_{PP}$ | Programming Supply Current | | 75 | mA |
| $1/T_{CLCL}$ | Oscillator Frquency | 4 | 6 | MHz |
| $T_{AVGL}$ | Address Setup to $\overline{PROG}$ Low | 48 $T_{CLCL}$ | | |
| $T_{GHAX}$ | Adress Hold after $\overline{PROG}$ | 48 $T_{CLCL}$ | | |
| $T_{DVGL}$ | Data Setup to $\overline{PROG}$ Low | 48 $T_{CLCL}$ | | |
| $T_{GHDX}$ | Data Hold after $\overline{PROG}$ | 48 $T_{CLCL}$ | | |
| $T_{EHSH}$ | (Enable) High to $V_{PP}$ | 48 $T_{CLCL}$ | | |
| $T_{SHGL}$ | $V_{PP}$ Setup to $\overline{PROG}$ Low | 10 | | µs |
| $T_{GHSL}$ | $V_{PP}$ Hold after $\overline{PROG}$ | 10 | | µs |
| $T_{GLGH}$ | $\overline{PROG}$ Width | 90 | 110 | µs |
| $T_{AVQV}$ | Address to Valid Data | | 48 $T_{CLCL}$ | |
| $T_{ELQV}$ | ENABLE Low to Data Valid | | 48 $T_{CLCL}$ | |
| $T_{EHQZ}$ | Data Float after ENABLE | 0 | 48 $T_{CLCL}$ | |

### 19.5.10 EPROM Programming and Verification Waveforms

**Figure 19-10.** EPROM Programming and Verification Waveforms




* 8KB: up to P2.4, 16KB: up to P2.5, 32KB: up to P3.4, 64KB: up to P3.5

| Part Number | Supply Voltage | Temperature Range | Package | Packing |
|---|---|---|---|---|
| TS87C54X2-MCC | 5V ±10% | Commercial | PQFP44 | Tray |
| TS87C54X2-MCE | 5V ±10% | Commercial | VQFP44 | Tray |
| TS87C54X2-VCA | 5V ±10% | Commercial | PDIL40 | Stick |
| TS87C54X2-VCB | 5V ±10% | Commercial | PLCC44 | Stick |
| TS87C54X2-VCC | 5V ±10% | Commercial | PQFP44 | Tray |
| TS87C54X2-VCE | 5V ±10% | Commercial | VQFP44 | Tray |
| TS87C54X2-LCA | 2.7 to 5.5V | Commercial | PDIL40 | Stick |
| TS87C54X2-LCB | 2.7 to 5.5V | Commercial | PLCC44 | Stick |
| TS87C54X2-LCC | 2.7 to 5.5V | Commercial | PQFP44 | Tray |
| TS87C54X2-LCE | 2.7 to 5.5V | Commercial | VQFP44 | Tray |
| TS87C54X2-MIA | 5V ±10% | Industrial | PDIL40 | Stick |
| TS87C54X2-MIB | 5V ±10% | Industrial | PLCC44 | Stick |
| TS87C54X2-MIC | 5V ±10% | Industrial | PQFP44 | Tray |
| TS87C54X2-MIE | 5V ±10% | Industrial | VQFP44 | Tray |
| TS87C54X2-VIA | 5V ±10% | Industrial | PDIL40 | Stick |
| TS87C54X2-VIB | 5V ±10% | Industrial | PLCC44 | Stick |
| TS87C54X2-VIC | 5V ±10% | Industrial | PQFP44 | Tray |
| TS87C54X2-VIE | 5V ±10% | Industrial | VQFP44 | Tray |
| TS87C54X2-LIA | 2.7 to 5.5V | Industrial | PDIL40 | Stick |
| TS87C54X2-LIB | 2.7 to 5.5V | Industrial | PLCC44 | Stick |
| TS87C54X2-LIC | 2.7 to 5.5V | Industrial | PQFP44 | Tray |
| TS87C54X2-LIE | 2.7 to 5.5V | Industrial | VQFP44 | Tray |
| | | | | |
| AT87C54X2-3CSUM | 5V ±10% | Industrial & Green | PDIL40 | Stick |
| AT87C54X2-SLSUM | 5V ±10% | Industrial & Green | PLCC44 | Stick |
| AT87C54X2-RLTUM | 5V ±10% | Industrial & Green | VQFP44 | Tray |
| AT87C54X2-3CSUL | 2.7 to 5.5V | Industrial & Green | PDIL40 | Stick |
| AT87C54X2-SLSUL | 2.7 to 5.5V | Industrial & Green | PLCC44 | Stick |
| AT87C54X2-RLTUL | 2.7 to 5.5V | Industrial & Green | VQFP44 | Tray |
| AT87C54X2-3CSUV | 5V ±10% | Industrial & Green | PDIL40 | Stick |
| AT87C54X2-SLSUV | 5V ±10% | Industrial & Green | PLCC44 | Stick |
| AT87C54X2-RLTUV | 5V ±10% | Industrial & Green | VQFP44 | Tray |
| | | | | |

| Part Number | Supply Voltage | Temperature Range | Package | Packing |
|---|---|---|---|---|
| TS87C58X2-MCE | 5V ±10% | Commercial | VQFP44 | Tray |
| TS87C58X2-VCA | 5V ±10% | Commercial | PDIL40 | Stick |
| TS87C58X2-VCB | 5V ±10% | Commercial | PLCC44 | Stick |
| TS87C58X2-VCC | 5V ±10% | Commercial | PQFP44 | Tray |
| TS87C58X2-VCE | 5V ±10% | Commercial | VQFP44 | Tray |
| TS87C58X2-LCA | 2.7 to 5.5V | Commercial | PDIL40 | Stick |
| TS87C58X2-LCB | 2.7 to 5.5V | Commercial | PLCC44 | Stick |
| TS87C58X2-LCC | 2.7 to 5.5V | Commercial | PQFP44 | Tray |
| TS87C58X2-LCE | 2.7 to 5.5V | Commercial | VQFP44 | Tray |
| TS87C58X2-MIA | 5V ±10% | Industrial | PDIL40 | Stick |
| TS87C58X2-MIB | 5V ±10% | Industrial | PLCC44 | Stick |
| TS87C58X2-MIC | 5V ±10% | Industrial | PQFP44 | Tray |
| TS87C58X2-MIE | 5V ±10% | Industrial | VQFP44 | Tray |
| TS87C58X2-VIA | 5V ±10% | Industrial | PDIL40 | Stick |
| TS87C58X2-VIB | 5V ±10% | Industrial | PLCC44 | Stick |
| TS87C58X2-VIC | 5V ±10% | Industrial | PQFP44 | Tray |
| TS87C58X2-VIE | 5V ±10% | Industrial | VQFP44 | Tray |
| TS87C58X2-LIA | 2.7 to 5.5V | Industrial | PDIL40 | Stick |
| TS87C58X2-LIB | 2.7 to 5.5V | Industrial | PLCC44 | Stick |
| TS87C58X2-LIC | 2.7 to 5.5V | Industrial | PQFP44 | Tray |
| TS87C58X2-LIE | 2.7 to 5.5V | Industrial | VQFP44 | Tray |
| | | | | |
| AT87C58X2-3CSUM | 5V ±10% | Industrial & Green | PDIL40 | Stick |
| AT87C58X2-SLSUM | 5V ±10% | Industrial & Green | PLCC44 | Stick |
| AT87C58X2-RLTUM | 5V ±10% | Industrial & Green | VQFP44 | Tray |
| AT87C58X2-3CSUL | 2.7 to 5.5V | Industrial & Green | PDIL40 | Stick |
| AT87C58X2-SLSUL | 2.7 to 5.5V | Industrial & Green | PLCC44 | Stick |
| AT87C58X2-RLTUL | 2.7 to 5.5V | Industrial & Green | VQFP44 | Tray |
| AT87C58X2-3CSUV | 5V ±10% | Industrial & Green | PDIL40 | Stick |
| AT87C58X2-SLSUV | 5V ±10% | Industrial & Green | PLCC44 | Stick |
| AT87C58X2-RLTUV | 5V ±10% | Industrial & Green | VQFP44 | Tray |

# 21. Datasheet Revision History

## 21.1 Changes from Rev. C 01/01 to Rev. D 11/05

1. Added green product Ordering Information.

## 21.2 Changes from Rev. D 11/05 to Rev. E 04/06

1. Changed value of AUXR register.

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