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Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40/20MHz
Connectivity	UART/USART
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIL
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts87c54x2-mca

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

5. Pin Configuration



*NIC: No Internal Connection





6. TS80C54/58X2 Enhanced Features

In comparison to the original 80C52, the TS80C54/58X2 implements some new features, which are:

- The X2 option.
- The Dual Data Pointer.
- The Watchdog.
- The 4 level interrupt priority system.
- The power-off flag.
- The ONCE mode.
- The ALE disabling.
- Some enhanced features are also located in the UART and the timer 2.

6.1 X2 Feature

The TS80C54/58X2 core needs only 6 clock periods per machine cycle. This feature called "X2" provides the following advantages:

- Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power.
- Save power consumption while keeping same CPU power (oscillator power saving).
- Save power consumption by dividing dynamically operating frequency by 2 in operating and idle modes.
- Increase CPU power by 2 while keeping same crystal frequency.

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

6.1.1 Description

The clock for the whole circuit and peripheral is first divided by two before being used by the CPU core and peripherals. This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%. Figure 6-2. shows the clock generation block diagram. X2 bit is validated on XTAL1÷2 rising edge to avoid glitches when switching from X2 to STD mode. Figure 6-2. shows the mode switching waveforms.

Figure 6-1. Clock Generation Diagram



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Figure 6-2. Mode Switching Waveforms

The X2 bit in the CKCON register (See Table 6-1.) allows to switch from 12 clock cycles per instruction to 6 clock cycles and vice versa. At reset, the standard speed is activated (STD mode). Setting this bit activates the X2 feature (X2 mode).

CAUTION

In order to prevent any incorrect operation while operating in X2 mode, user must be aware that all peripherals using clock frequency as time reference (UART, timers) will have their time reference divided by two. For example a free running timer generating an interrupt every 20 ms will then generate an interrupt every 10 ms. UART with 4800 baud rate will have 9600 baud rate.



7. Dual Data Pointer Register Ddptr

The additional data pointer can be used to speed up code execution and reduce code size in a number of ways.

The dual DPTR structure is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called

DPS = AUXR1/bit0 (See Table 7-1.) that allows the program code to switch between them (Refer to Figure 7-1).



Figure 7-1. Use of Dual Pointer







8.1.1 Programmable Clock-Output

In the clock-out mode, timer 2 operates as a 50%-duty-cycle, programmable clock generator (See Figure 8-2) . The input clock increments TL2 at frequency $F_{OSC}/2$. The timer repeatedly counts to overflow from a loaded value. At overflow, the contents of RCAP2H and RCAP2L registers are loaded into TH2 and TL2. In this mode, timer 2 overflows do not generate interrupts. The formula gives the clock-out frequency as a function of the system oscillator frequency and the value in the RCAP2H and RCAP2L registers :

$$Clock - OutFrequency = \frac{F_{osc}}{4 \times (65536 - RCAP2H/RCAP2L)}$$

For a 16 MHz system clock, timer 2 has a programmable frequency range of 61 Hz $(F_{OSC}/2^{16})$ to 4 MHz $(F_{OSC}/4)$. The generated clock signal is brought out to T2 pin (P1.0).

Timer 2 is programmed for the clock-out mode as follows:

- Set T2OE bit in T2MOD register.
- Clear C/T2 bit in T2CON register.
- Determine the 16-bit reload value from the formula and enter it in RCAP2H/RCAP2L registers.



Table 8-1.	T2CON Register
------------	----------------

T2CON - Timer 2 Control Register (C8h)

7	6	5	4	5 4 3 2 1 0						
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#			
Bit Number	Bit Mnemonic			Descrip	otion					
7	TF2	Timer 2 overflow Must be cleared b Set by hardware c	r Flag by software. on timer 2 over	flow, if RCLK =	0 and TCLK =	0.				
6	EXF2	Timer 2 External Flag Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. When set, causes the CPU to vector to timer 2 interrupt routine when timer 2 interrupt is enabled. Must be cleared by software. EXF2 doesn't cause an interrupt in Up/down counter mode (DCEN = 1)								
5	RCLK	Receive Clock bit Clear to use timer Set to use timer 2	1 overflow as overflow as re	receive clock fo ceive clock for s	r serial port in serial port in mo	mode 1 or 3. ode 1 or 3.				
4	TCLK	Transmit Clock bit Clear to use timer Set to use timer 2	1 overflow as overflow as tra	transmit clock for	or serial port in serial port in m	mode 1 or 3. node 1 or 3.				
3	EXEN2	Timer 2 External Enable bit Clear to ignore events on T2EX pin for timer 2 operation. Set to cause a capture or reload when a negative transition on T2EX pin is detected, if timer 2 is not used to clock the serial port.					tected, if timer			
2	TR2	Timer 2 Run control bit Clear to turn off timer 2. Set to turn on timer 2.								
1	C/T2#	Timer/Counter 2 select bit Clear for timer operation (input from internal clock system: F _{OSC}). Set for counter operation (input from T2 input pin, falling edge trigger). Must be 0 for clock out mode.					e 0 for clock			
0	CP/RL2#	Timer 2 Capture/F If RCLK=1 or TCL overflow. Clear to auto-reloa Set to capture on	Reload bit K=1, CP/RL2# ad on timer 2 o negative transi	is ignored and verflows or neg tions on T2EX p	timer is forced ative transition pin if EXEN2=1	to auto-reload s on T2EX pin	on timer 2 if EXEN2=1.			

Reset Value = 0000 0000b Bit addressable





Table 8-2.	T2MOD Register	
	TOMOD TO ON LO V	

T2MOD	- Timer 2	2 Mode	Control	Register	(C9h)
-------	-----------	--------	---------	----------	-------

7	6	5	4	3	2	1	0			
-	-	-	-	-	-	T2OE	DCEN			
Bit Number	Bit Mnemonic		Description							
7	-	Reserved The value read	from this bit is in	determinate. Do	o not set this bit					
6	-	Reserved The value read	from this bit is in	determinate. Do	o not set this bit					
5	-	Reserved The value read	from this bit is in	determinate. Do	o not set this bit					
4	-	Reserved The value read	from this bit is in	determinate. Do	o not set this bit					
3	-	Reserved The value read	from this bit is in	determinate. Do	o not set this bit					
2	-	Reserved The value read	eserved The value read from this bit is indeterminate. Do not set this bit.							
1	T2OE	Timer 2 Output Clear to progra Set to program	Timer 2 Output Enable bit Clear to program P1.0/T2 as clock input or I/O port. Set to program P1.0/T2 as clock output.							
0	DCEN	Down Counter Clear to disable Set to enable ti	Enable bit timer 2 as up/do mer 2 as up/down	own counter. n counter.						

Reset Value = XXXX XX00b Not bit addressable The following is an example of how to use given addresses to address different slaves:

Slave A:	SADDR <u>SADEN</u> Given	1111 0001b <u>1111 1010b</u> 1111 0X0Xb
Slave B:	SADDR <u>SADEN</u> Given	1111 0011b <u>1111 1001b</u> 1111 0XX1b
Slave C:	SADDR <u>SADEN</u> Given	1111 0010b <u>1111 1101b</u> 1111 00X1b

The SADEN byte is selected so that each slave may be addressed separately.

For slave A, bit 0 (the LSB) is a don't-care bit; for slaves B and C, bit 0 is a 1. To communicate with slave A only, the master must send an address where bit 0 is clear (e.g. 1111 0000b). For slave A, bit 1 is a 1; for slaves B and C, bit 1 is a don't care bit. To communicate with slaves B and C, but not slave A, the master must send an address with bits 0 and 1 both set (e.g. 1111

0011b).

To communicate with slaves A, B and C, the master must send an address with bit 0 set, bit 1 clear, and bit 2 clear (e.g. 1111 0001b).

9.1.3 Broadcast Address

A broadcast address is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't-care bits, e.g.:

SADDR	0101 0110b	
SADEN	1111 1100b	
Broadcast =SADDR OR SADEN	1111 111Xb	

The use of don't-care bits provides flexibility in defining the broadcast address, however in most applications, a broadcast address is FFh. The following is an example of using broadcast addresses:

Slave A:	SADDR <u>SADEN</u> Broadcast	1111 0001b <u>1111 1010b</u> 1111 1X11b,
Slave B:	SADDR <u>SADEN</u> Broadcast	1111 0011b <u>1111 1001b</u> 1111 1X11B,
Slave C:	SADDR= <u>SADEN</u> Broadcast	1111 0010b <u>1111 1101b</u> 1111 1111b

For slaves A and B, bit 2 is a don't care bit; for slave C, bit 2 is set. To communicate with all of the slaves, the master must send an address FFh. To communicate with slaves A and B, but not slave C, the master can send and address FBh.

9.1.4 Reset Addresses

On reset, the SADDR and SADEN registers are initialized to 00h, i.e. the given and broadcast addresses are XXXX XXXb (all don't-care bits). This ensures that the serial port will reply to any address, and so, that it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition.





Table 9-1. SADEN - Slave Address Mask Register (B9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

Not bit addressable

Table 9-2. SADDR - Slave Address Register (A9h)

				()	-	-	-
7	6	5	4	3	2	1	0

Reset Value = 0000 0000b Not bit addressable

Table 9-3.

SCON Register SCON - Serial Control Register (98h)

7	6		5	4	3	2	1	0
FE/SM0	SM1		SM2	REN	TB8	RB8	TI	RI
Bit Number	Bit Mnemonic				Descrip	otion		
7	FE	Fran Clea Set SMC	ning Error bit ar to reset the by hardware v DD0 must be s	t (SMOD0=1) error state, no when an invalic set to enable ac	t cleared by a v I stop bit is dete ccess to the FE	alid stop bit. ected. bit		
	SM0	Seria Refe SMC	al port Mode er to SM1 for s DD0 must be c	bit 0 serial port mod cleared to enab	e selection. le access to the	e SM0 bit		
6	SM1	Seri SMC 0 1 1	Serial port Mode bit 1 Serial port Mode Description Baud Rate SM0 SM1Mode Description Baud Rate 0 0 Shift RegisterF _{XTAL} /12 (/6 in X2 mode) 0 1 1 8-bit UARTVariable 1 0 2 9-bit UARTF _{XTAL} /64 or F _{XTAL} /32 (/32, /16 in X2 mode) 1 1 3 9-bit UARTF _{XTAL} /64 or F _{XTAL} /32 (/32, /16 in X2 mode)					in X2 mode)
5	SM2	Seria Clea Set 1 1. Th	al port Mode ar to disable m to enable mul his bit should l	2 bit / Multipr nultiprocessor of tiprocessor con be cleared in m	ocessor Comm communication mmunication fea node 0.	nunication Ena feature. ature in mode 2	able bit ? and 3, and eve	entually mode
4	REN	Rece Clea Set 1	eption Enable ar to disable so to enable seri	e bit erial reception. al reception.				
3	TB8	Tran Clea Set	smitter Bit 8 / ar to transmit a to transmit a l	Ninth bit to tra a logic 0 in the ogic 1 in the 9t	nsmit in modes 9th bit. h bit.	2 and 3.		
2	RB8	Receiver Bit 8 / Ninth bit received in modes 2 and 3 Cleared by hardware if 9th bit received is a logic 0. Set by hardware if 9th bit received is a logic 1. In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used.						
1	TI	Tran Clea Set I the c	Transmit Interrupt flag Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes.					
0	RI	Rece Clea Set the c	eive Interrupt ar to acknowle by hardware a other modes.	t flag edge interrupt. at the end of th	e 8th bit time in	mode 0, see F	igure 9-2. and	Figure 9-3. in

Reset Value = 0000 0000b Bit addressable





Figure 11-1. Power-Down Exit Waveform



Exit from power-down by reset redefines all the SFRs, exit from power-down by external interrupt does no affect the SFRs.

Exit from power-down by either reset or external interrupt does not affect the internal RAM content.

NOTE: If idle mode is activated with power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data*	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data*	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

 Table 11-1.
 The state of ports during idle and power-down modes

* Port 0 can force a "zero" level A "one" Level will leave port floating.

12. Hardware Watchdog Timer

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upset. The WDT consists of a 14-bit counter and the WatchDog Timer ReSeT (WDTRST) SFR. The WDT is by default disabled from exiting reset. To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, it will increment every machine cycle while the oscillator is running and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST-pin.

12.1 Using the WDT

To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, the user needs to service it by writing to 01EH and 0E1H to WDTRST to avoid WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH) and this will reset the device. When WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycle. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST-pin. The RESET pulse duration is 96 x $T_{\rm OSC}$, where $T_{\rm OSC}$ = $1/F_{\rm OSC}$. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

To have a more powerful WDT, a 2^7 counter has been added to extend the Time-out capability, ranking from 16ms to 2s @ F_{OSC} = 12MHz. To manage this feature, refer to WDTPRG register description, Table 12-2. (SFR0A7h).

Table 12-1.WDTRST RegisterWDTRST Address (0A6h)

	7	6	5	4	3	2	1
Reset value	Х	Х	Х	Х	Х	Х	Х

Write only, this SFR is used to reset/enable the WDT by writing 01EH then 0E1H in sequence.





7	6		5	4	3	2	1	0	
T4	T4 T3		T2 T1 T0 S2		S1	S0			
Bit Number	Bit Mnemonic		Description						
7	T4								
6	Т3								
5	T2	Reserve Do not	ved try to set o	or clear this bit					
4	T1		,						
3	Т0								
2	S2	WDT T	īme-out se	lect bit 2					
1	S1	WDT T	īme-out se	lect bit 1					
0	S0	WDT T	īme-out se	lect bit 0					
		<u>S2S1</u> 0 0 0 1 1 1 1	<u>S0</u> 0 1 1 0 0 1	<u>Selected Tr</u> 0 1 0 1 0 1 0 1	<u>me-out</u> (2 ¹⁴ - 1) machine (2 ¹⁵ - 1) machine (2 ¹⁶ - 1) machine (2 ¹⁷ - 1) machine (2 ¹⁸ - 1) machine (2 ¹⁹ - 1) machine (2 ²⁰ - 1) machine (2 ²¹ - 1) machine	e cycles, 16.3 r e cycles, 32.7 r e cycles, 65.5 r e cycles, 131 m e cycles, 262 m e cycles, 542 m e cycles, 1.05 s e cycles, 2.09 s	ns @ 12 MHz ns @ 12 MHz ns @ 12 MHz is @ 12 MHz		

Table 12-2. WDTPRG Register WDTPRG Address (0A7h)

Reset value XXXX X000

12.1.1 WDT during Power Down and Idle

In Power Down mode the oscillator stops, which means the WDT also stops. While in Power Down mode the user does not need to service the WDT. There are 2 methods of exiting Power Down mode: by a hardware reset or via a level activated external interrupt which is enabled prior to entering Power Down mode. When Power Down is exited with hardware reset, servicing the WDT should occur as it normally should whenever the TS80C54/58X2 is reset. Exiting Power Down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service routine.

To ensure that the WDT does not overflow within a few states of exiting of powerdown, it is best to reset the WDT just before entering powerdown.

In the Idle mode, the oscillator continues to run. To prevent the WDT from resetting the TS80C54/58X2 while in Idle mode, the user should always set up a timer that will periodically exit Idle, service the WDT, and re-enter Idle mode.

13. ONCE[™] Mode (ON Chip Emulation)

The ONCE mode facilitates testing and debugging of systems using TS80C54/58X2 without removing the circuit from the board. The ONCE mode is invoked by driving certain pins of the TS80C54/58X2; the following sequence must be exercised:

- Pull ALE low while the device is in reset (RST high) and PSEN is high.
- Hold ALE low as RST is deactivated.

While the TS80C54/58X2 is in ONCE mode, an emulator or test CPU can be used to drive the circuit Table 13-1 shows the status of the port pins during ONCE mode.

Normal operation is restored when normal reset is applied.

Table 13-1. External Pin Status during ONCE Mode

ALE	PSEN	Port 0	Port 1	Port 2	Port 3	XTAL1/2
Weak pull-up	Weak pull-up	Float	Weak pull-up	Weak pull-up	Weak pull-up	Active





14. Power-Off Flag

The power-off flag allows the user to distinguish between a "cold start" reset and a "warm start" reset.

A cold start reset is the one induced by V_{CC} switch-on. A warm start reset occurs while V_{CC} is still applied to the device and could be generated for example by an exit from power-down.

The power-off flag (POF) is located in PCON register (See Table 14-1.). POF is set by hardware when V_{CC} rises from 0 to its nominal voltage. The POF can be set or cleared by software allowing the user to determine the type of reset.

The POF value is only relevant with a Vcc range from 4.5V to 5.5V. For lower Vcc value, reading POF bit will return indeterminate value.

	6	6 5 4 3	2	1	0					
SMOD1	SMOD) -	POF	GF0	PD	IDL				
Bit Number	Bit Mnemonic		Description							
7	SMOD1	Serial port M Set to select	erial port Mode bit 1 et to select double baud rate in mode 1, 2 or 3.							
6	SMOD0	Serial port M Clear to selec Set to to selec	Serial port Mode bit 0 Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.							
5	-	Reserved The value rea	Reserved The value read from this bit is indeterminate. Do not set this bit.							
4	POF	Power-Off Fla Clear to recog Set by hardwa	Power-Off Flag Clear to recognize next reset type. Set by hardware when V _{CC} rises from 0 to its nominal voltage. Can also be set by software.							
3	GF1	General purp Cleared by us Set by user fo	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.							
2	GF0	General purp Cleared by us Set by user fo	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.							
1	PD	Power-Down Cleared by ha Set to enter p	Power-Down mode bit Cleared by hardware when reset occurs. Set to enter power-down mode.							
0	IDL	Idle mode bit Clear by hard Set to enter id	dle mode bit Clear by hardware when interrupt or reset occurs. Set to enter idle mode.							

Table 14-1. PCON Register PCON - Power Control Register (87h)

Reset Value = 00X1 0000b Not bit addressable

Table 18-1.	Signature B	ytes Content
-------------	-------------	--------------

Location	Contents	Comment					
30h	58h	Manufacturer Code: Atmel Wireless & Microcontrollers					
31h	57h	Family Code: C51 X2					
60h	37h	Product name: TS80C58X2					
60h	B7h	Product name: TS87C58X2					
60h	3Bh	Product name: TS80C54X2					
60h	BBh	Product name: TS87C54X2					
61h	FFh	Product revision number					



Symbol	Туре	Standard Clock	X2 Clock	-М	-V	-L	Units
T _{RLRH}	Min	6 T - x	3 T - x	20	15	25	ns
T _{WLWH}	Min	6 T - x	3 T - x	20	15	25	ns
T _{RLDV}	Max	5 T - x	2.5 T - x	25	23	30	ns
T _{RHDX}	Min	x	х	0	0	0	ns
T _{RHDZ}	Max	2 T - x	T - x	20	15	25	ns
T _{LLDV}	Max	8 T - x	4T -x	40	35	45	ns
T _{AVDV}	Max	9 T - x	4.5 T - x	60	50	65	ns
T _{LLWL}	Min	3 T - x	1.5 T - x	25	20	30	ns
T _{LLWL}	Max	3 T + x	1.5 T + x	25	20	30	ns
T _{AVWL}	Min	4 T - x	2 T - x	25	20	30	ns
T _{QVWX}	Min	T - x	0.5 T - x	15	10	20	ns
T _{QVWH}	Min	7 T - x	3.5 T - x	15	10	20	ns
T _{WHQX}	Min	T - x	0.5 T - x	10	8	15	ns
T _{RLAZ}	Max	х	х	0	0	0	ns
T _{WHLH}	Min	T - x	0.5 T - x	15	10	20	ns
T _{WHLH}	Max	T + x	0.5 T + x	15	10	20	ns

Table 19-10. AC Parameters for a Variable Clock: derating formula

19.5.5 External Data Memory Write Cycle









19.5.9 EPROM Programming and Verification Characteristics

 T_A = 21°C to 27°C; V_{SS} = 0V; V_{CC} = 5V \pm 10% while programming. V_{CC} = operating range while verifying.

Symbol	Parameter	Min	Мах	Units
V _{PP}	Programming Supply Voltage	12.5	13	V
I _{PP}	Programming Supply Current		75	mA
1/T _{CLCL}	Oscillator Frquency	4	6	MHz
T _{AVGL}	Address Setup to PROG Low	48 T _{CLCL}		
T _{GHAX}	Adress Hold after PROG	48 T _{CLCL}		
T _{DVGL}	Data Setup to PROG Low	48 T _{CLCL}		
T_{GHDX}	Data Hold after PROG	48 T _{CLCL}		
T _{EHSH}	(Enable) High to V _{PP}	48 T _{CLCL}		
T _{SHGL}	V _{PP} Setup to PROG Low	10		μs
T _{GHSL}	V _{PP} Hold after PROG	10		μs
T _{GLGH}	PROG Width	90	110	μs
T _{AVQV}	Address to Valid Data		48 T _{CLCL}	
T _{ELQV}	ENABLE Low to Data Valid		48 T _{CLCL}	
T _{EHQZ}	Data Float after ENABLE	0	48 T _{CLCL}	

Table 19-14. EPROM Programming Parameters

19.5.10 EPROM Programming and Verification Waveforms





* 8KB: up to P2.4, 16KB: up to P2.5, 32KB: up to P3.4, 64KB: up to P3.5

Part Number	Supply Voltage	Temperature Range	Package	Packing
TS87C58X2-MCE	5V ±10%	Commercial	VQFP44	Tray
TS87C58X2-VCA	5V ±10%	Commercial	PDIL40	Stick
TS87C58X2-VCB	5V ±10%	Commercial	PLCC44	Stick
TS87C58X2-VCC	5V ±10%	Commercial	PQFP44	Tray
TS87C58X2-VCE	5V ±10%	Commercial	VQFP44	Tray
TS87C58X2-LCA	2.7 to 5.5V	Commercial	PDIL40	Stick
TS87C58X2-LCB	2.7 to 5.5V	Commercial	PLCC44	Stick
TS87C58X2-LCC	2.7 to 5.5V	Commercial	PQFP44	Tray
TS87C58X2-LCE	2.7 to 5.5V	Commercial	VQFP44	Tray
TS87C58X2-MIA	5V ±10%	Industrial	PDIL40	Stick
TS87C58X2-MIB	5V ±10%	Industrial	PLCC44	Stick
TS87C58X2-MIC	5V ±10%	Industrial	PQFP44	Tray
TS87C58X2-MIE	5V ±10%	Industrial	VQFP44	Tray
TS87C58X2-VIA	5V ±10%	Industrial	PDIL40	Stick
TS87C58X2-VIB	5V ±10%	Industrial	PLCC44	Stick
TS87C58X2-VIC	5V ±10%	Industrial	PQFP44	Tray
TS87C58X2-VIE	5V ±10%	Industrial	VQFP44	Tray
TS87C58X2-LIA	2.7 to 5.5V	Industrial	PDIL40	Stick
TS87C58X2-LIB	2.7 to 5.5V	Industrial	PLCC44	Stick
TS87C58X2-LIC	2.7 to 5.5V	Industrial	PQFP44	Tray
TS87C58X2-LIE	2.7 to 5.5V	Industrial	VQFP44	Tray
	•			
AT87C58X2-3CSUM	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUM	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUM	5V ±10%	Industrial & Green	VQFP44	Tray
AT87C58X2-3CSUL	2.7 to 5.5V	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUL	2.7 to 5.5V	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUL	2.7 to 5.5V	Industrial & Green	VQFP44	Tray
AT87C58X2-3CSUV	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUV	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUV	5V ±10%	Industrial & Green	VQFP44	Tray

21. Datasheet Revision History

21.1 Changes from Rev. C 01/01 to Rev. D 11/05

1. Added green product Ordering Information.

21.2 Changes from Rev. D 11/05 to Rev. E 04/06

1. Changed value of AUXR register.





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