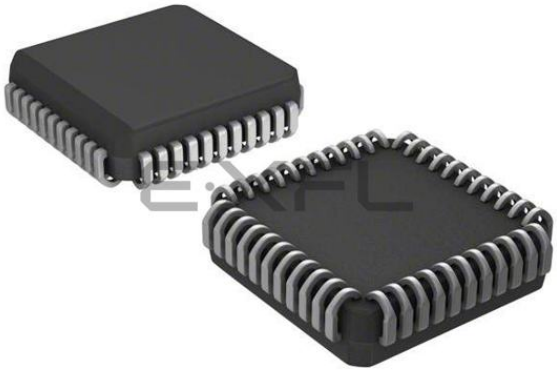

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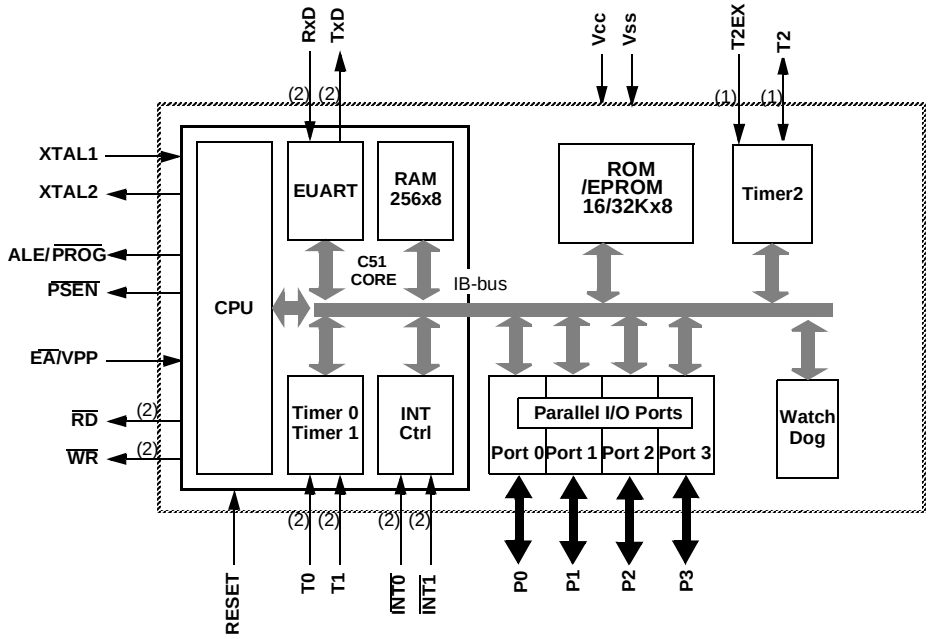
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40/20MHz
Connectivity	UART/USART
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts87c54x2-mib

The TS80C54/58X2 has 2 software-selectable modes of reduced activity for further reduction in power consumption. In the idle mode the CPU is frozen while the timers, the serial port and the interrupt system are still operating. In the power-down mode the RAM is saved and all other functions are inoperative.

PDIL40 PLCC44 PQFP44 F1 VQFP44 1.4	ROM (bytes)	EPROM (bytes)
TS80C54X2 TS80C58X2	16k 32k	0 0
TS87C54X2 TS87C58X2	0 0	16k 32k

2. Block Diagram



(1): Alternate function of Port 1

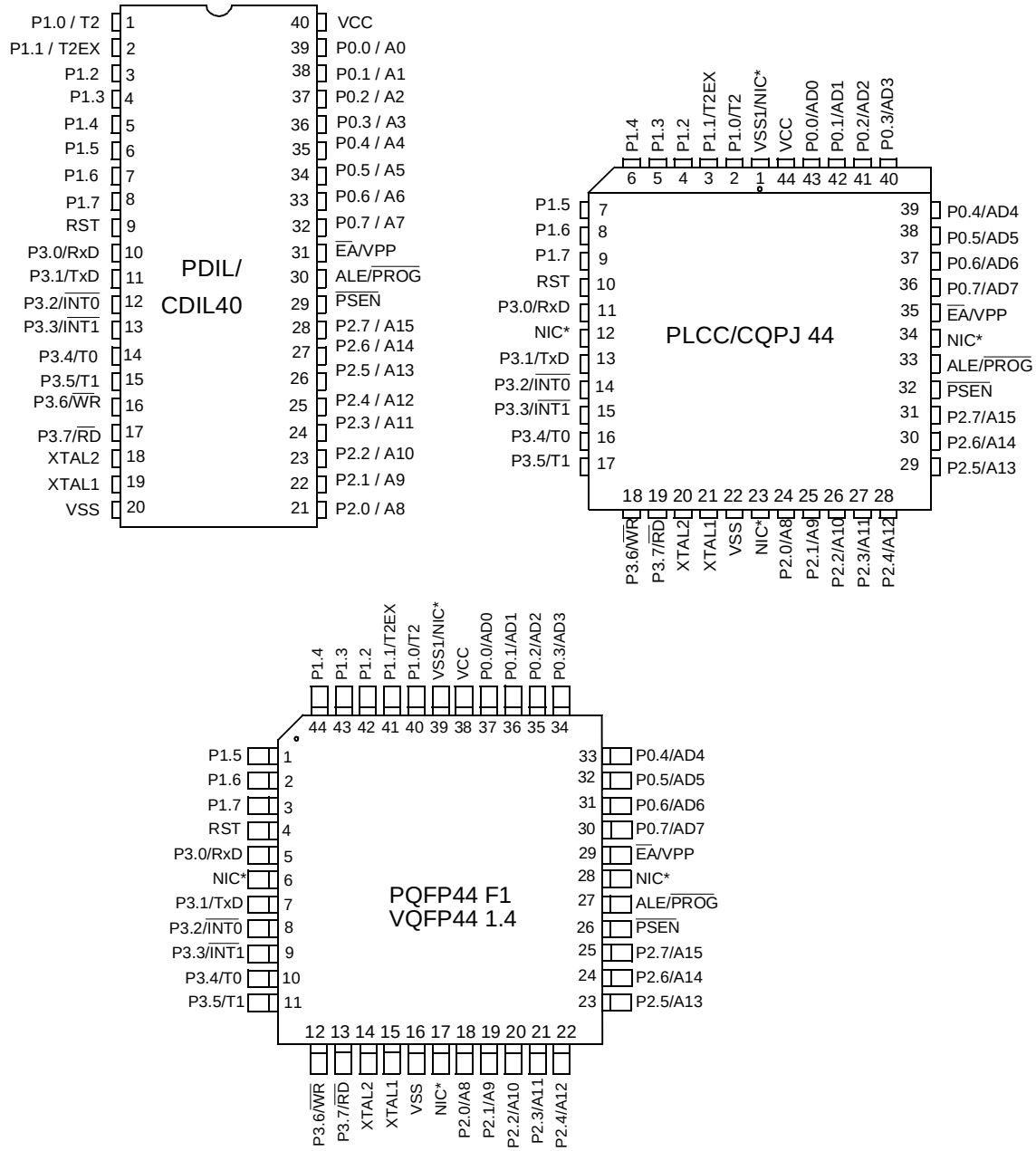
(2): Alternate function of Port 3

Table 4-1. All SFRs with their address and their reset value

	Bit address-able	**Non Bit addressable**							
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h									FFh
F0h	B 0000 0000								F7h
E8h									EFh
E0h	ACC 0000 0000								E7h
D8h									DFh
D0h	PSW 0000 0000								D7h
C8h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			CFh
C0h									C7h
B8h	IP XX00 0000	SADEN 0000 0000							BFh
B0h	P3 1111 1111							IPH XX00 0000	B7h
A8h	IE 0X00 0000	SADDR 0000 0000							AFh
A0h	P2 1111 1111		AUXR1 XXXX 0XX0				WDTRST XXXX XXXX	WDTPRG XXXX X000	A7h
98h	SCON 0000 0000	SBUF XXXX XXXX							9Fh
90h	P1 1111 1111								97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XXXX XXX0	CKCON XXXX XXX0	8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00X1 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

reserved

5. Pin Configuration



*NIC: No Internal Connection

Table 5-1. Pin Description for 40/44 pin packages

MNEMONIC	PIN NUMBER			TYPE	Name And Function
	DIL	LCC	VQFP 1.4		
V_{SS}	20	22	16	I	**Ground:** 0V reference
Vss1		1	39	I	Optional Ground: **Contact the Sales Office for ground connection.**
V_{CC}	40	44	38	I	**Power Supply:** This is the power supply voltage for normal, idle and power-down operation
P0.0-P0.7	39-32	43-36	37-30	I/O	**Port 0**: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. Port 0 pins must be polarized to Vcc or Vss in order to prevent any parasitic current consumption. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-up when emitting 1s. Port 0 also inputs the code bytes during EPROM programming. External pull-ups are required during program verification during which P0 outputs the code bytes.
P1.0-P1.7	1-8	2-9	40-44 1-3	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups. Port 1 also receives the low-order address byte during memory programming and verification. Alternate functions for Port 1 include:
	1	2	40	I/O	**T2 (P1.0):** Timer/Counter 2 external count input/Clockout
	2	3	41	I	**T2EX (P1.1):** Timer/Counter 2 Reload/Capture/Direction Control
P2.0-P2.7	21-28	24-31	18-25	I/O	**Port 2**: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR).In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 emits the contents of the P2 SFR. Some Port 2 pins receive the high order address bits during EPROM programming and verification: P2.0 to P2.5 for A8 to A13
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Some Port 3 pin P3.4 receive the high order address bits during EPROM programming and verification for TS8xC58X2 devices. Port 3 also serves the special features of the 80C51 family, as listed below.
	10	11	5	I	**RXD (P3.0):** Serial input port
	11	13	7	O	**TXD (P3.1):** Serial output port
	12	14	8	I	**$\overline{\text{INT0}}$ (P3.2):** External interrupt 0
	13	15	9	I	**$\overline{\text{INT1}}$ (P3.3):** External interrupt 1
	14	16	10	I	**T0 (P3.4):** Timer 0 external input
	15	17	11	I	**T1 (P3.5):** Timer 1 external input
	16	18	12	O	**$\overline{\text{WR}}$ (P3.6):** External data memory write strobe
	17	19	13	O	**$\overline{\text{RD}}$ (P3.7):** External data memory read strobe P3.4 also receives A14 during TS87C58X2 EPROM Programming.
Reset	9	10	4	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC}.

Table 7-1. AUXR1: Auxiliary Register 1

7	6	5	4	3	2	1	0
-	-	-	-	GF3	0	-	DPS

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	GF3	This bit is a general purpose user flag
2	0	**Reserved** Always stuck at 0.
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	DPS	**Data Pointer Selection** Clear to select DPTR0. Set to select DPTR1.

Reset Value = XXXX 00X0
Not bit addressable

User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new feature. In that case, the reset value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

8. Timer 2

The timer 2 in the TS80C54/58X2 is compatible with the timer 2 in the 80C52.
It is a 16-bit timer/counter: the count is maintained by two eight-bit timer registers, TH2 and TL2, connected in cascade. It is controlled by T2CON register (See Table 8-1) and T2MOD register (See Table 8-2). Timer 2 operation is similar to Timer 0 and Timer 1. C/$\overline{T2}$ selects F_{OSC}/12 (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows TL2 to be incremented by the selected input.

Timer 2 has 3 operating modes: capture, autoreload and Baud Rate Generator. These modes are selected by the combination of RCLK, TCLK and CP/$\overline{RL2}$ (T2CON), as described in the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description.

Refer to the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description for the description of Capture and Baud Rate Generator Modes.

In TS80C54/58X2 Timer 2 includes the following enhancements:

- Auto-reload mode with up or down counter
- Programmable clock-output

8.1 Auto-Reload Mode

The auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. If DCEN bit in T2MOD is cleared, timer 2 behaves as in 80C52 (refer to the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description). If DCEN bit is set, timer 2 acts as an Up/down timer/counter as shown in Figure 8-1. In this mode the T2EX pin controls the direction of count.

When T2EX is high, timer 2 counts up. Timer overflow occurs at FFFFh which sets the TF2 flag and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L registers to be loaded into the timer registers TH2 and TL2.

When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers TH2 and TL2 equals the value stored in RCAP2H and RCAP2L registers. The underflow sets TF2 flag and reloads FFFFh into the timer registers.

The EXF2 bit toggles when timer 2 overflows or underflows according to the the direction of the count. EXF2 does not generate any interrupt. This bit can be used to provide 17-bit resolution

Table 10-4. IPH Register

IPH - Interrupt Priority High Register (B7h)

7	6	5	4	3	2	1	0
-	-	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	PT2H	Timer 2 overflow interrupt Priority High bit PT2H PT2 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
4	PSH	Serial port Priority High bit PSH PS Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
3	PT1H	Timer 1 overflow interrupt Priority High bit PT1H PT1 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
2	PX1H	External interrupt 1 Priority High bit PX1H PX1 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
1	PT0H	Timer 0 overflow interrupt Priority High bit PT0H PT0 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
0	PX0H	External interrupt 0 Priority High bit PX0H PX0 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest

Reset Value = XX00 0000b

Not bit addressable

11. Idle mode

An instruction that sets PCON.0 causes that to be the last instruction executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer, and Serial Port functions. The CPU status is preserved in its entirely : the Stack Pointer, Program Counter, Program Status Word, Accumulator and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels.

There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bits GF0 and GF1 can be used to give an indication if an interrupt occured during normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

11.1 Power-Down Mode

To save maximum power, a power-down mode can be invoked by software (Refer to Table 9-4., PCON register).

In power-down mode, the oscillator is stopped and the instruction that invoked power-down mode is the last instruction executed. The internal RAM and SFRs retain their value until the power-down mode is terminated. V_{CC} can be lowered to save further power. Either a hardware reset or an external interrupt can cause an exit from power-down. To properly terminate power-down, the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.

Only external interrupts $\overline{INT0}$ and $\overline{INT1}$ are useful to exit from power-down. For that, interrupt must be enabled and configured as level or edge sensitive interrupt input.
Holding the pin low restarts the oscillator but bringing the pin high completes the exit as detailed in Figure 11-1. When both interrupts are enabled, the oscillator restarts as soon as one of the two inputs is held low and power down exit will be completed when the first input will be released. In this case the higher priority interrupt service routine is executed.
Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put TS80C54/58X2 into power-down mode.

Table 12-2. WDTPRG Register
WDTPRG Address (0A7h)

7	6	5	4	3	2	1	0
T4	T3	T2	T1	T0	S2	S1	S0

Bit Number	Bit Mnemonic	Description
7	T4	**Reserved** Do not try to set or clear this bit.
6	T3	
5	T2	
4	T1	
3	T0	
2	S2	WDT Time-out select bit 2
1	S1	WDT Time-out select bit 1
0	S0	WDT Time-out select bit 0
		S2S1 S0 Selected Time-out 0 0 0 (2^{14} - 1) machine cycles, 16.3 ms @ 12 MHz 0 0 1 (2^{15} - 1) machine cycles, 32.7 ms @ 12 MHz 0 1 0 (2^{16} - 1) machine cycles, 65.5 ms @ 12 MHz 0 1 1 (2^{17} - 1) machine cycles, 131 ms @ 12 MHz 1 0 0 (2^{18} - 1) machine cycles, 262 ms @ 12 MHz 1 0 1 (2^{19} - 1) machine cycles, 542 ms @ 12 MHz 1 1 0 (2^{20} - 1) machine cycles, 1.05 s @ 12 MHz 1 1 1 (2^{21} - 1) machine cycles, 2.09 s @ 12 MHz

Reset value XXXX X000

12.1.1 WDT during Power Down and Idle

In Power Down mode the oscillator stops, which means the WDT also stops. While in Power Down mode the user does not need to service the WDT. There are 2 methods of exiting Power Down mode: by a hardware reset or via a level activated external interrupt which is enabled prior to entering Power Down mode. When Power Down is exited with hardware reset, servicing the WDT should occur as it normally should whenever the TS80C54/58X2 is reset. Exiting Power Down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service routine.

To ensure that the WDT does not overflow within a few states of exiting of powerdown, it is best to reset the WDT just before entering powerdown.

In the Idle mode, the oscillator continues to run. To prevent the WDT from resetting the TS80C54/58X2 while in Idle mode, the user should always set up a timer that will periodically exit Idle, service the WDT, and re-enter Idle mode.

17.2.3 Signature bytes

The TS87C54/58X2 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in section 8.3.

17.3 EPROM Programming

17.3.1 Set-up modes

In order to program and verify the EPROM or to read the signature bytes, the TS87C54/58X2 is placed in specific set-up modes (See Figure 17-1.).

Control and program signals must be held at the levels indicated in Table 17-2.

17.3.2 Definition of terms

Address Lines:P1.0-P1.7, P2.0-P2.5, P3.4 respectively for A0-A14 (P2.5 (A13) for TS87C54X2, P3.4 (A14) for TS87C58X2).

Data Lines:P0.0-P0.7 for D0-D7

Control Signals:RST, $\overline{\text{PSEN}}$, P2.6, P2.7, P3.3, P3.6, P3.7.

Program Signals:ALE/$\overline{\text{PROG}}$, $\overline{\text{EA}}$/VPP.

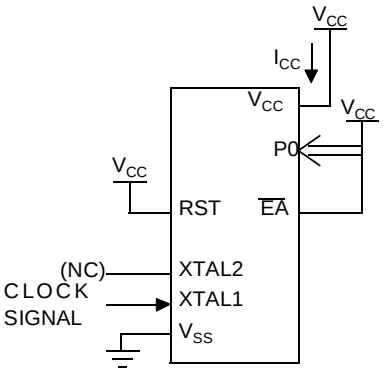
Table 17-2. EPROM Set-Up Modes

Mode	RST	PSEN	ALE/$\overline{\text{PROG}}$	$\overline{\text{EA}}$/VPP	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code data	1	0		12.75	0	1	1	1	1
Verify Code data	1	0	1	1	0		0	1	1
Program Encryption Array Address 0-3Fh	1	0		12.75	0	1	1	0	1
Read Signature Bytes	1	0	1	1	0		0	0	0
Program Lock bit 1	1	0		12.75	1	1	1	1	1
Program Lock bit 2	1	0		12.75	1	1	1	0	0
Program Lock bit 3	1	0		12.75	1	0	1	1	0

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL1}	Output Low Voltage, port 0 (6)			0.3 0.45 1.0	V V V	I_{OL} = 200 µA(4) I_{OL} = 3.2 mA(4) I_{OL} = 7.0 mA(4)
V_{OL2}	Output Low Voltage, ALE, $\overline{PSEN}$			0.3 0.45 1.0	V V V	I_{OL} = 100 µA(4) I_{OL} = 1.6 mA(4) I_{OL} = 3.5 mA(4)
V_{OH}	Output High Voltage, ports 1, 2, 3	V_{CC} - 0.3 V_{CC} - 0.7 V_{CC} - 1.5			V V V	I_{OH} = -10 µA I_{OH} = -30 µA I_{OH} = -60 µA V_{CC} = 5 V ± 10%
V_{OH1}	Output High Voltage, port 0	V_{CC} - 0.3 V_{CC} - 0.7 V_{CC} - 1.5			V V V	I_{OH} = -200 µA I_{OH} = -3.2 mA I_{OH} = -7.0 mA V_{CC} = 5 V ± 10%
V_{OH2}	Output High Voltage,ALE, $\overline{PSEN}$	V_{CC} - 0.3 V_{CC} - 0.7 V_{CC} - 1.5			V V V	I_{OH} = -100 µA I_{OH} = -1.6 mA I_{OH} = -3.5 mA V_{CC} = 5 V ± 10%
R_{RST}	RST Pulldown Resistor	50	90 (5)	200	kΩ	
I_{IL}	Logical 0 Input Current ports 1, 2 and 3			-50	µA	Vin = 0.45 V
I_{LI}	Input Leakage Current			±10	µA	0.45 V < Vin < V_{CC}
I_{TL}	Logical 1 to 0 Transition Current, ports 1, 2, 3			-650	µA	Vin = 2.0 V
C_{IO}	Capacitance of I/O Buffer			10	pF	Fc = 1 MHz T_A = 25°C
I_{PD}	Power Down Current		20 (5)	50	µA	2.0 V < V_{CC} < 5.5 V(3)
I_{CC} under RESET	Power Supply Current Maximum values, X1 mode: (7)			1 + 0.4 Freq (MHz) @12MHz 5.8 @16MHz 7.4	mA	V_{CC} = 5.5 V(1)
I_{CC} operating	Power Supply Current Maximum values, X1 mode: (7)			3 + 0.6 Freq (MHz) @12MHz 10.2 @16MHz 12.6	mA	V_{CC} = 5.5 V(8)
I_{CC} idle	Power Supply Current Maximum values, X1 mode: (7)			0.25+0.3 Freq (MHz) @12MHz 3.9 @16MHz 5.1	mA	V_{CC} = 5.5 V(2)

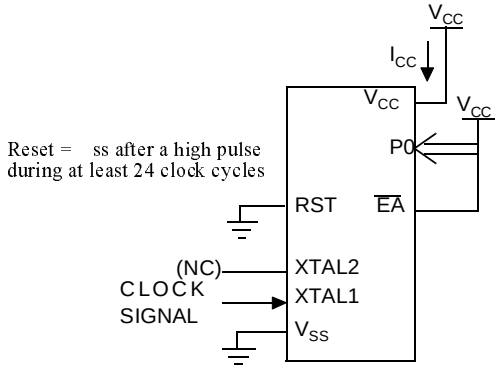
5. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
6. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:
   Port 0: 26 mA
   Ports 1, 2 and 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
7. For other values, please contact your sales office.
8. Operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH}, T_{CHCL} = 5 ns (see Figure 19-5.), $V_{IL} = V_{SS} + 0.5$ V,
   $V_{IH} = V_{CC} - 0.5$V; XTAL2 N.C.; $\overline{EA}$ = Port 0 = V_{CC}; RST = V_{SS}. The internal ROM runs the code 80 FE (label: SJMP label). I_{CC} would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.

Figure 19-1. I_{CC} Test Condition, under reset



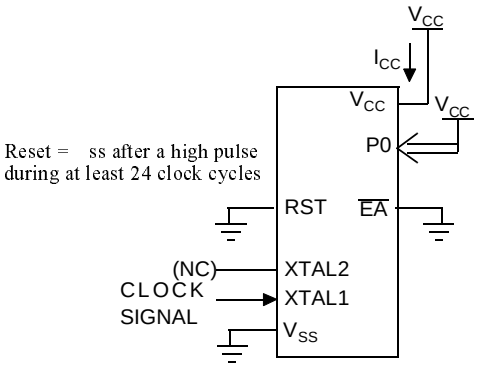
All other pins are disconnected.

Figure 19-2. Operating I_{CC} Test Condition



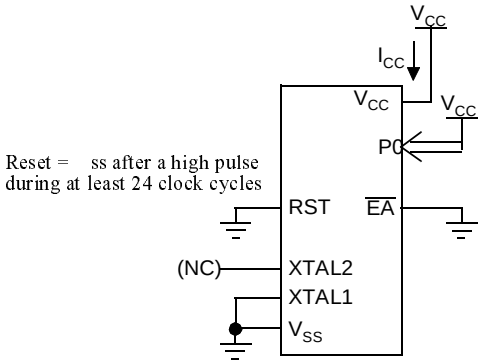
All other pins are disconnected.

Figure 19-3. I_{CC} Test Condition, Idle Mode



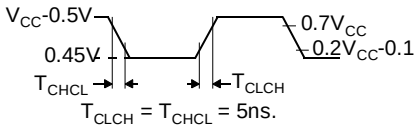
All other pins are disconnected.

Figure 19-4. I_{CC} Test Condition, Power-Down Mode



All other pins are disconnected.

Figure 19-5. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes



19.5.2 External Program Memory Characteristics

Table 19-5. Symbol Description

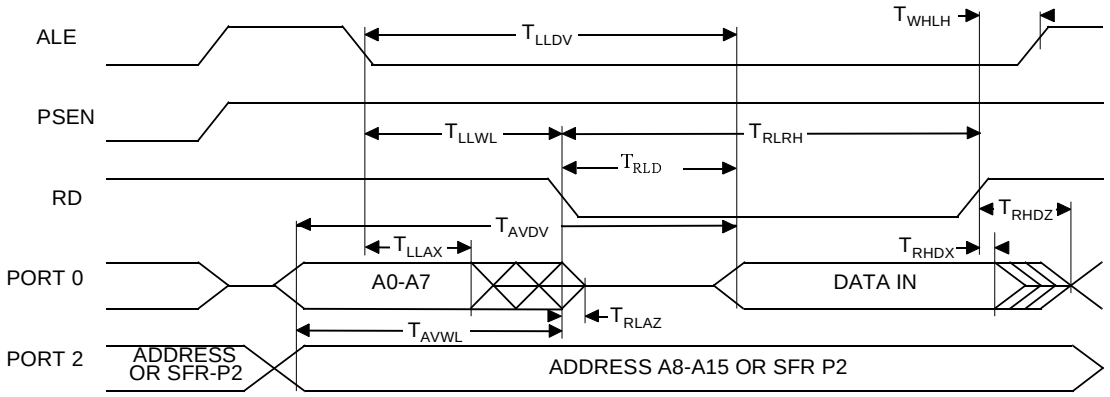
Symbol	Parameter
T	Oscillator clock period
T_{LHLL}	ALE pulse width
T_{AVLL}	Address Valid to ALE
T_{LLAX}	Address Hold After ALE
T_{LLIV}	ALE to Valid Instruction In
T_{LLPL}	ALE to $\overline{PSEN}$
T_{PLPH}	$\overline{PSEN}$ Pulse Width
T_{PLIV}	$\overline{PSEN}$ to Valid Instruction In
T_{PXIX}	Input Instruction Hold After $\overline{PSEN}$
T_{PXIZ}	Input Instruction FloatAfter $\overline{PSEN}$
T_{PXAV}	$\overline{PSEN}$ to Address Valid
T_{AVIV}	Address to Valid Instruction In
T_{PLAZ}	$\overline{PSEN}$ Low to Address Float

Table 19-6. AC Parameters for Fix Clock

Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
Symbol	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
T	25		33		25		50		33		ns
T_{LHLL}	40		25		42		35		52		ns
T_{AVLL}	10		4		12		5		13		ns
T_{LLAX}	10		4		12		5		13		ns
T_{LLIV}		70		45		78		65		98	ns
T_{LLPL}	15		9		17		10		18		ns
T_{PLPH}	55		35		60		50		75		ns
T_{PLIV}		35		25		50		30		55	ns
T_{PXIX}	0		0		0		0		0		ns
T_{PXIZ}		18		12		20		10		18	ns
T_{AVIV}		85		53		95		80		122	ns
T_{PLAZ}		10		10		10		10		10	ns

19.5.6 External Data Memory Read Cycle

Figure 19-8. External Data Memory Read Cycle



19.5.7 Serial Port Timing - Shift Register Mode

Table 19-11. Symbol Description

Symbol	Parameter
T_{XLXL}	Serial port clock cycle time
T_{QVHX}	Output data set-up to clock rising edge
T_{XHQX}	Output data hold after clock rising edge
T_{XHDX}	Input data hold after clock rising edge
T_{XHDV}	Clock rising edge to input data valid

Table 19-12. AC Parameters for a Fix Clock

Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
Symbol	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
T_{XLXL}	300		200		300		300		400		ns
T_{QVHX}	200		117		200		200		283		ns
T_{XHQX}	30		13		30		30		47		ns
T_{XHDX}	0		0		0		0		0		ns
T_{XHDV}		117		34		117		117		200	ns

19.5.9 EPROM Programming and Verification Characteristics

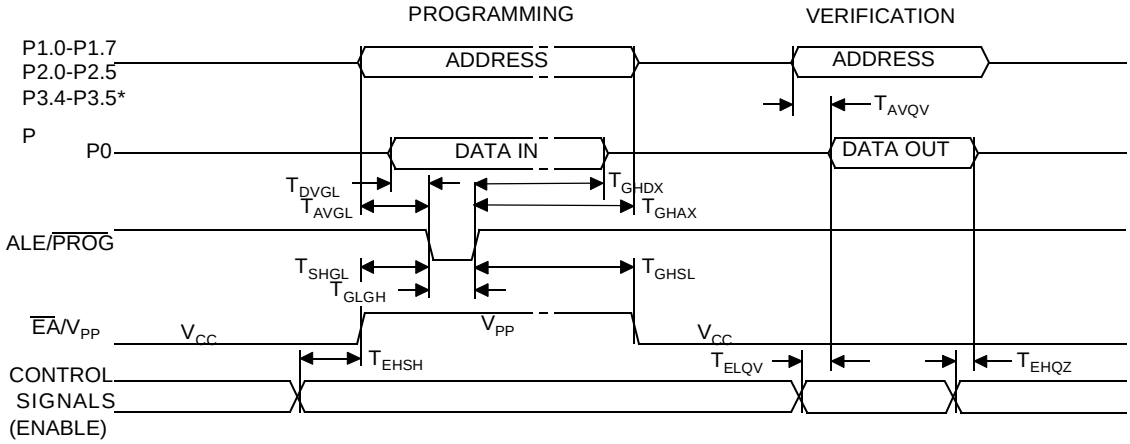
T_A = 21°C to 27°C; V_{SS} = 0V; V_{CC} = 5V ± 10% while programming. V_{CC} = operating range while verifying.

Table 19-14. EPROM Programming Parameters

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13	V
I_{PP}	Programming Supply Current		75	mA
$1/T_{CLCL}$	Oscillator Frquency	4	6	MHz
T_{AVGL}	Address Setup to $\overline{PROG}$ Low	48 T_{CLCL}		
T_{GHAX}	Adress Hold after $\overline{PROG}$	48 T_{CLCL}		
T_{DVGL}	Data Setup to $\overline{PROG}$ Low	48 T_{CLCL}		
T_{GHDX}	Data Hold after $\overline{PROG}$	48 T_{CLCL}		
T_{EHSH}	(Enable) High to V_{PP}	48 T_{CLCL}		
T_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
T_{GHSL}	V_{PP} Hold after $\overline{PROG}$	10		µs
T_{GLGH}	$\overline{PROG}$ Width	90	110	µs
T_{AVQV}	Address to Valid Data		48 T_{CLCL}	
T_{ELQV}	ENABLE Low to Data Valid		48 T_{CLCL}	
T_{EHQZ}	Data Float after ENABLE	0	48 T_{CLCL}	

19.5.10 EPROM Programming and Verification Waveforms

Figure 19-10. EPROM Programming and Verification Waveforms



* 8KB: up to P2.4, 16KB: up to P2.5, 32KB: up to P3.4, 64KB: up to P3.5

20. Ordering Information

Table 20-1. Possible Ordering Entries

Part Number	Supply Voltage	Temperature Range	Package	Packing
TS80C54X2xxx-MCA	-5 to +/-10%	Commercial	PDIL40	Stick
TS80C54X2xxx-MCB	-5 to +/-10%	Commercial	PLCC44	Stick
TS80C54X2xxx-MCC	-5 to +/-10%	Commercial	PQFP44	Tray
TS80C54X2xxx-MCE	-5 to +/-10%	Commercial	VQFP44	Tray
TS80C54X2xxx-VCA	-5 to +/-10%	Commercial	PDIL40	Stick
TS80C54X2xxx-VCB	-5 to +/-10%	Commercial	PLCC44	Stick
TS80C54X2xxx-VCC	-5 to +/-10%	Commercial	PQFP44	Tray
TS80C54X2xxx-VCE	-5 to +/-10%	Commercial	VQFP44	Tray
TS80C54X2xxx-LCA	-5 to +/-10%	Commercial	PDIL40	Stick
TS80C54X2xxx-LCB	-5 to +/-10%	Commercial	PLCC44	Stick
TS80C54X2xxx-LCC	-5 to +/-10%	Commercial	PQFP44	Tray
TS80C54X2xxx-LCE	-5 to +/-10%	Commercial	VQFP44	Tray
TS80C54X2xxx-MIA	-5 to +/-10%	Industrial	PDIL40	Stick
TS80C54X2xxx-MIB	-5 to +/-10%	Industrial	PLCC44	Stick
TS80C54X2xxx-MIC	-5 to +/-10%	Industrial	PQFP44	Tray
TS80C54X2xxx-MIE	-5 to +/-10%	Industrial	VQFP44	Tray
TS80C54X2xxx-VIA	-5 to +/-10%	Industrial	PDIL40	Stick
TS80C54X2xxx-VIB	-5 to +/-10%	Industrial	PLCC44	Stick
TS80C54X2xxx-VIC	-5 to +/-10%	Industrial	PQFP44	Tray
TS80C54X2xxx-VIE	-5 to +/-10%	Industrial	VQFP44	Tray
TS80C54X2xxx-LIA	-5 to +/-10%	Industrial	PDIL40	Stick
TS80C54X2xxx-LIB	-5 to +/-10%	Industrial	PLCC44	Stick
TS80C54X2xxx-LIC	-5 to +/-10%	Industrial	PQFP44	Tray
TS80C54X2xxx-LIE	-5 to +/-10%	Industrial	VQFP44	Tray
AT80C54X2zzz-3CSUM	-5 to +/-10%	Industrial & Green	PDIL40	Stick
AT80C54X2zzz-SLSUM	-5 to +/-10%	Industrial & Green	PLCC44	Stick
AT80C54X2zzz-RLTUM	-5 to +/-10%	Industrial & Green	VQFP44	Tray
AT80C54X2zzz-3CSUL	-5 to +/-10%	Industrial & Green	PDIL40	Stick
AT80C54X2zzz-SLSUL	-5 to +/-10%	Industrial & Green	PLCC44	Stick
AT80C54X2zzz-RLTUL	-5 to +/-10%	Industrial & Green	VQFP44	Tray
AT80C54X2zzz-3CSUV	-5 to +/-10%	Industrial & Green	PDIL40	Stick
AT80C54X2zzz-SLSUV	-5 to +/-10%	Industrial & Green	PLCC44	Stick
AT80C54X2zzz-RLTUV	-5 to +/-10%	Industrial & Green	VQFP44	Tray
TS87C54X2-MCA	5V ±10%	Commercial	PDIL40	Stick
TS87C54X2-MCB	5V ±10%	Commercial	PLCC44	Stick

Part Number	Supply Voltage	Temperature Range	Package	Packing
TS87C54X2-MCC	5V ±10%	Commercial	PQFP44	Tray
TS87C54X2-MCE	5V ±10%	Commercial	VQFP44	Tray
TS87C54X2-VCA	5V ±10%	Commercial	PDIL40	Stick
TS87C54X2-VCB	5V ±10%	Commercial	PLCC44	Stick
TS87C54X2-VCC	5V ±10%	Commercial	PQFP44	Tray
TS87C54X2-VCE	5V ±10%	Commercial	VQFP44	Tray
TS87C54X2-LCA	2.7 to 5.5V	Commercial	PDIL40	Stick
TS87C54X2-LCB	2.7 to 5.5V	Commercial	PLCC44	Stick
TS87C54X2-LCC	2.7 to 5.5V	Commercial	PQFP44	Tray
TS87C54X2-LCE	2.7 to 5.5V	Commercial	VQFP44	Tray
TS87C54X2-MIA	5V ±10%	Industrial	PDIL40	Stick
TS87C54X2-MIB	5V ±10%	Industrial	PLCC44	Stick
TS87C54X2-MIC	5V ±10%	Industrial	PQFP44	Tray
TS87C54X2-MIE	5V ±10%	Industrial	VQFP44	Tray
TS87C54X2-VIA	5V ±10%	Industrial	PDIL40	Stick
TS87C54X2-VIB	5V ±10%	Industrial	PLCC44	Stick
TS87C54X2-VIC	5V ±10%	Industrial	PQFP44	Tray
TS87C54X2-VIE	5V ±10%	Industrial	VQFP44	Tray
TS87C54X2-LIA	2.7 to 5.5V	Industrial	PDIL40	Stick
TS87C54X2-LIB	2.7 to 5.5V	Industrial	PLCC44	Stick
TS87C54X2-LIC	2.7 to 5.5V	Industrial	PQFP44	Tray
TS87C54X2-LIE	2.7 to 5.5V	Industrial	VQFP44	Tray
AT87C54X2-3CSUM	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C54X2-SLSUM	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C54X2-RLTUM	5V ±10%	Industrial & Green	VQFP44	Tray
AT87C54X2-3CSUL	2.7 to 5.5V	Industrial & Green	PDIL40	Stick
AT87C54X2-SLSUL	2.7 to 5.5V	Industrial & Green	PLCC44	Stick
AT87C54X2-RLTUL	2.7 to 5.5V	Industrial & Green	VQFP44	Tray
AT87C54X2-3CSUV	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C54X2-SLSUV	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C54X2-RLTUV	5V ±10%	Industrial & Green	VQFP44	Tray

Part Number	Supply Voltage	Temperature Range	Package	Packing
TS87C58X2-MCE	5V ±10%	Commercial	VQFP44	Tray
TS87C58X2-VCA	5V ±10%	Commercial	PDIL40	Stick
TS87C58X2-VCB	5V ±10%	Commercial	PLCC44	Stick
TS87C58X2-VCC	5V ±10%	Commercial	PQFP44	Tray
TS87C58X2-VCE	5V ±10%	Commercial	VQFP44	Tray
TS87C58X2-LCA	2.7 to 5.5V	Commercial	PDIL40	Stick
TS87C58X2-LCB	2.7 to 5.5V	Commercial	PLCC44	Stick
TS87C58X2-LCC	2.7 to 5.5V	Commercial	PQFP44	Tray
TS87C58X2-LCE	2.7 to 5.5V	Commercial	VQFP44	Tray
TS87C58X2-MIA	5V ±10%	Industrial	PDIL40	Stick
TS87C58X2-MIB	5V ±10%	Industrial	PLCC44	Stick
TS87C58X2-MIC	5V ±10%	Industrial	PQFP44	Tray
TS87C58X2-MIE	5V ±10%	Industrial	VQFP44	Tray
TS87C58X2-VIA	5V ±10%	Industrial	PDIL40	Stick
TS87C58X2-VIB	5V ±10%	Industrial	PLCC44	Stick
TS87C58X2-VIC	5V ±10%	Industrial	PQFP44	Tray
TS87C58X2-VIE	5V ±10%	Industrial	VQFP44	Tray
TS87C58X2-LIA	2.7 to 5.5V	Industrial	PDIL40	Stick
TS87C58X2-LIB	2.7 to 5.5V	Industrial	PLCC44	Stick
TS87C58X2-LIC	2.7 to 5.5V	Industrial	PQFP44	Tray
TS87C58X2-LIE	2.7 to 5.5V	Industrial	VQFP44	Tray
AT87C58X2-3CSUM	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUM	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUM	5V ±10%	Industrial & Green	VQFP44	Tray
AT87C58X2-3CSUL	2.7 to 5.5V	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUL	2.7 to 5.5V	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUL	2.7 to 5.5V	Industrial & Green	VQFP44	Tray
AT87C58X2-3CSUV	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUV	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUV	5V ±10%	Industrial & Green	VQFP44	Tray

21. Datasheet Revision History

21.1 Changes from Rev. C 01/01 to Rev. D 11/05

1. Added green product Ordering Information.

21.2 Changes from Rev. D 11/05 to Rev. E 04/06

1. Changed value of AUXR register.

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