

Welcome to [E-XFL.COM](https://www.e-xfl.com)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

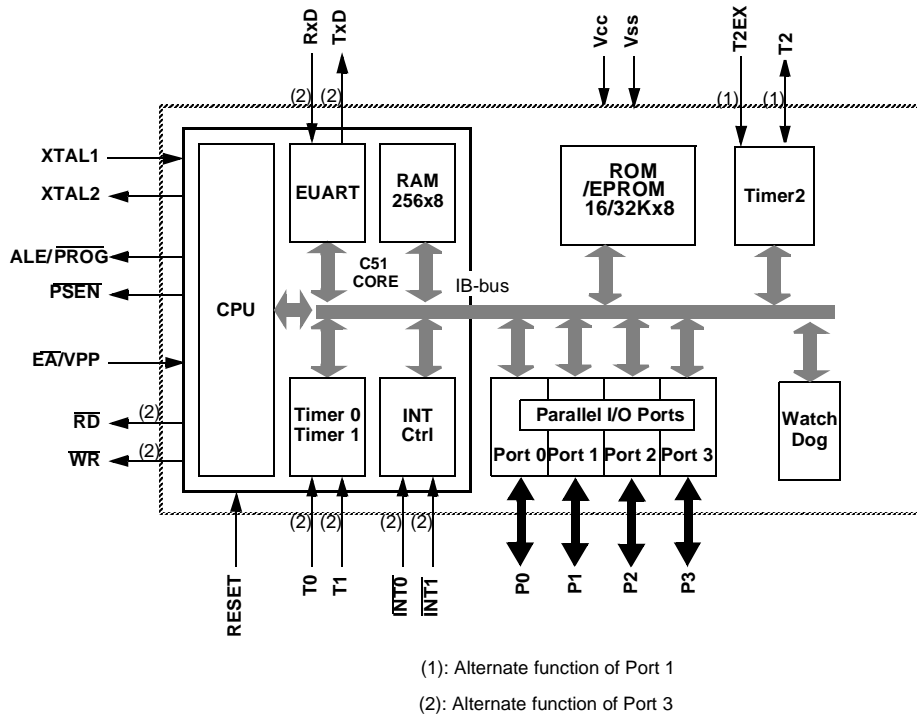
#### Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40/30MHz
Connectivity	UART/USART
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-VQFP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/ts87c54x2-vce">https://www.e-xfl.com/product-detail/microchip-technology/ts87c54x2-vce</a>

The TS80C54/58X2 has 2 software-selectable modes of reduced activity for further reduction in power consumption. In the idle mode the CPU is frozen while the timers, the serial port and the interrupt system are still operating. In the power-down mode the RAM is saved and all other functions are inoperative.

PDIL40 PLCC44 PQFP44 F1 VQFP44 1.4	ROM (bytes)	EPROM (bytes)
TS80C54X2	16k	0
TS80C58X2	32k	0
TS87C54X2	0	16k
TS87C58X2	0	32k

## 2. Block Diagram

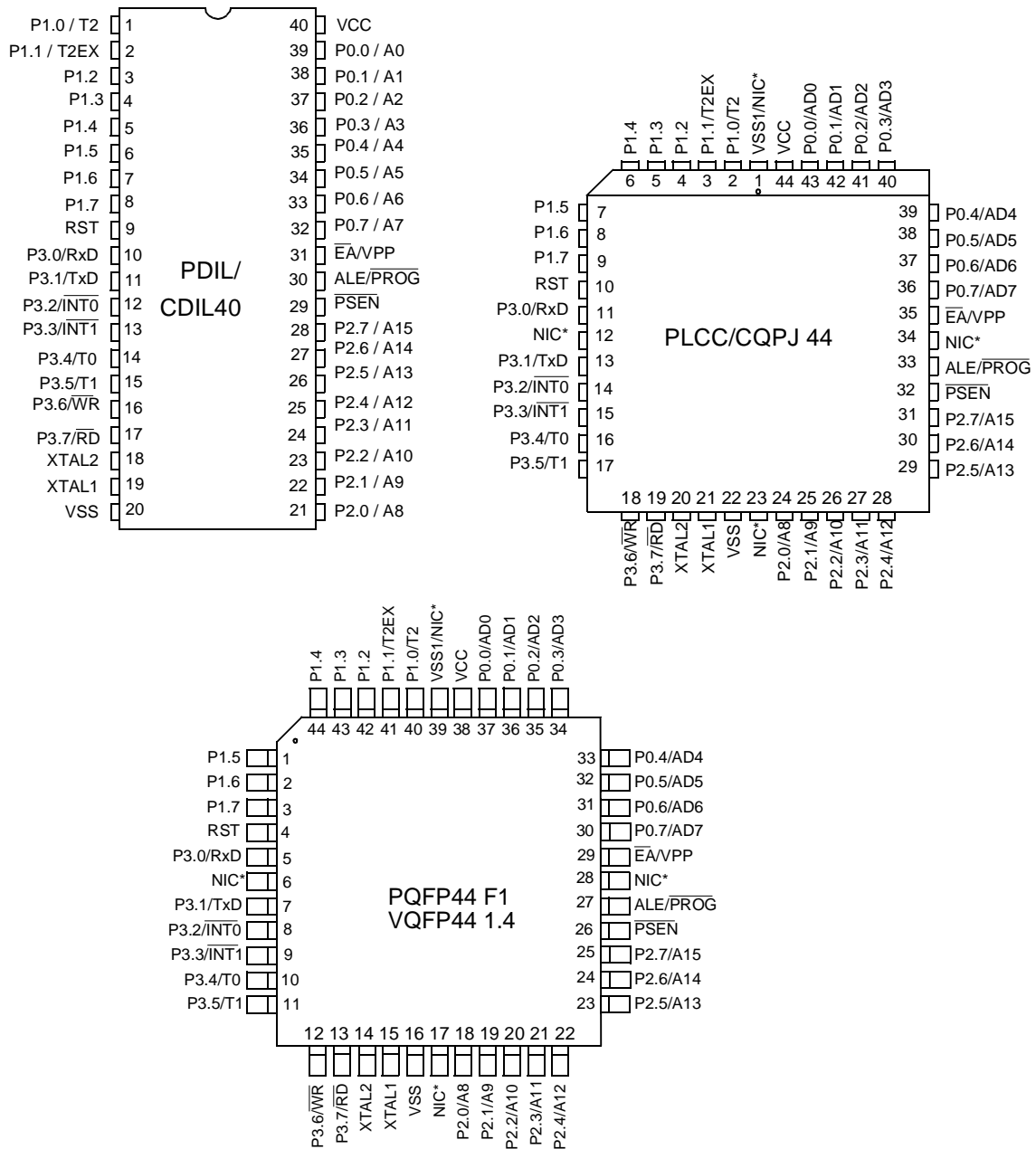


## **4. SFR Mapping**

The Special Function Registers (SFRs) of the TS80C54/58X2 fall into the following categories:

- C51 core registers: ACC, B, DPH, DPL, PSW, SP, AUXR1
- I/O port registers: P0, P1, P2, P3
- Timer registers: T2CON, T2MOD, TCON, TH0, TH1, TH2, TMOD, TL0, TL1, TL2, RCAP2L, RCAP2H
- Serial I/O port registers: SADDR, SADEN, SBUF, SCON
- Power and clock control registers: PCON
- HDW Watchdog Timer Reset: WDTRST, WDTPRG
- Interrupt system registers: IE, IP, IPH
- Others: AUXR, CKCON

## 5. Pin Configuration



\*NIC: No Internal Connection

**Table 5-1.** Pin Description for 40/44 pin packages

MNEMONIC	PIN NUMBER			TYPE	Name And Function
	DIL	LCC	VQFP 1.4		
MNEMONIC	PIN NUMBER			TYPE	NAME AND FUNCTION
ALE/ $\overline{\text{PROG}}$	30	33	27	O (I)	<b>Address Latch Enable/Program Pulse:</b> Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (1/3 in X2 mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input ( $\overline{\text{PROG}}$ ) during EPROM programming. ALE can be disabled by setting SFR's AUXR.0 bit. With this bit set, ALE will be inactive during internal fetches.
PSEN	29	32	26	O	<b>Program Store ENable:</b> The read strobe to external program memory. When executing code from the external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory.
$\overline{\text{EA}}/\text{V}_{\text{PP}}$	31	35	29	I	<b>External Access Enable/Programming Supply Voltage:</b> $\overline{\text{EA}}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H and 3FFFFH (54X2) or 7FFFFH (58X2). If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 3FFFFH (54X2) or 7FFFFH (58X2). This pin also receives the 12.75V programming supply voltage ( $\text{V}_{\text{PP}}$ ) during EPROM programming. If security level 1 is programmed, $\overline{\text{EA}}$ will be internally latched on Reset.
XTAL1	19	21	15	I	<b>Crystal 1:</b> Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	<b>Crystal 2:</b> Output from the inverting oscillator amplifier

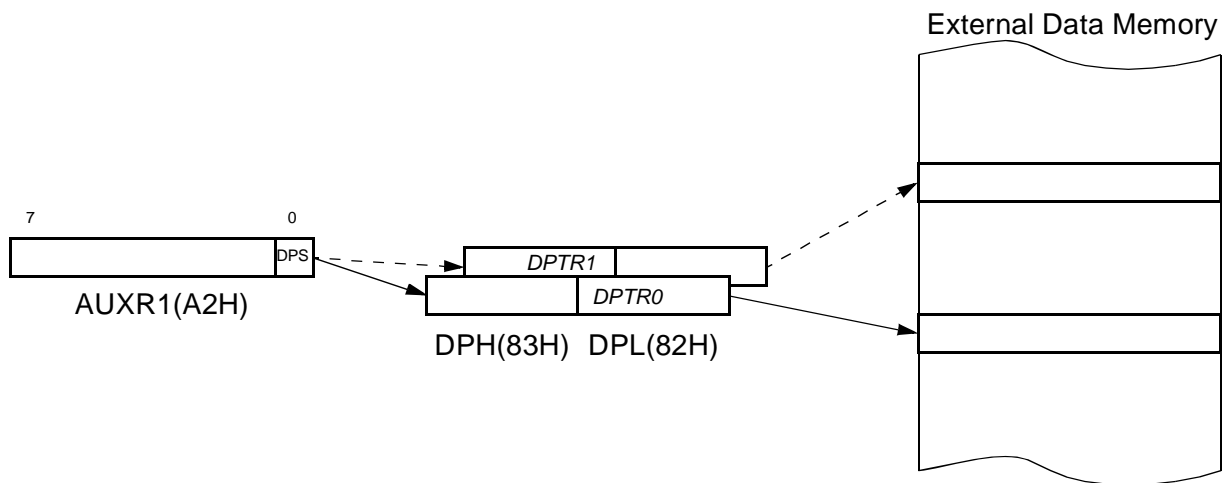
## 7. Dual Data Pointer Register Ddptr

The additional data pointer can be used to speed up code execution and reduce code size in a number of ways.

The dual DPTR structure is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called

DPS = AUXR1/bit0 (See Table 7-1.) that allows the program code to switch between them (Refer to Figure 7-1).

**Figure 7-1.** Use of Dual Pointer



**Table 7-1.** AUXR1: Auxiliary Register 1

7	6	5	4	3	2	1	0
-	-	-	-	GF3	0	-	DPS

Bit Number	Bit Mnemonic	Description
7	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
4	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
3	GF3	This bit is a general purpose user flag
2	0	<b>Reserved</b> Always stuck at 0.
1	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
0	DPS	<b>Data Pointer Selection</b> Clear to select DPTR0. Set to select DPTR1.

Reset Value = XXXX 00X0

Not bit addressable

User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new feature. In that case, the reset value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

## 9. TS80C54/58X2 Serial I/O Port

The serial I/O port in the TS80C54/58X2 is compatible with the serial I/O port in the 80C52. It provides both synchronous and asynchronous communication modes. It operates as an Universal Asynchronous Receiver and Transmitter (UART) in three full-duplex modes (Modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates

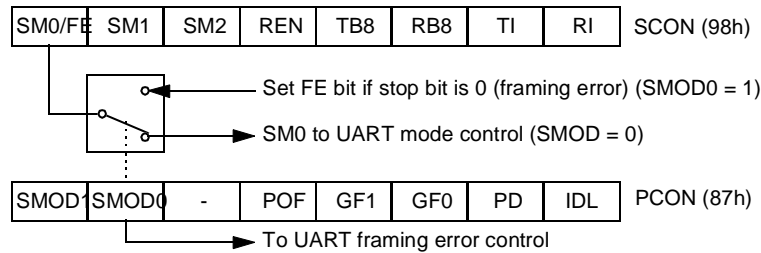
Serial I/O port includes the following enhancements:

- Framing error detection
- Automatic address recognition

### 9.1 Framing Error Detection

Framing bit error detection is provided for the three asynchronous modes (modes 1, 2 and 3). To enable the framing bit error detection feature, set SMOD0 bit in PCON register (See Figure 9-1).

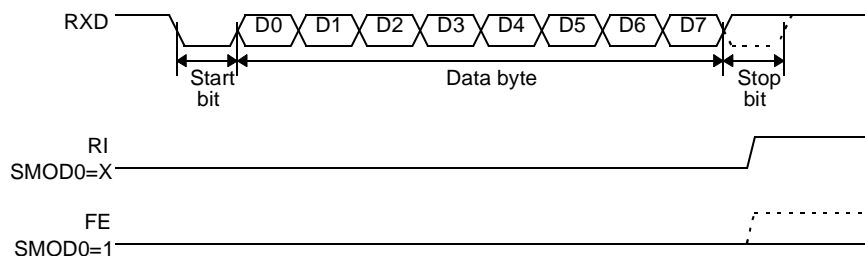
**Figure 9-1.** Framing Error Block Diagram



When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two CPUs. If a valid stop bit is not found, the Framing Error bit (FE) in SCON register (See Table 9-3.) bit is set.

Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset can clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 9-2. and Figure 9-3.).

**Figure 9-2.** UART Timings in Mode 1





**Table 9-3.** SCON Register  
SCON - Serial Control Register (98h)

7	6	5	4	3	2	1	0
FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Bit Number	Bit Mnemonic	Description																				
7	FE	<b>Framing Error bit (SMOD0=1)</b> Clear to reset the error state, not cleared by a valid stop bit. Set by hardware when an invalid stop bit is detected. SMOD0 must be set to enable access to the FE bit																				
	SM0	<b>Serial port Mode bit 0</b> Refer to SM1 for serial port mode selection. SMOD0 must be cleared to enable access to the SM0 bit																				
6	SM1	<b>Serial port Mode bit 1</b> <table><tr><th>SM0</th><th>SM1Mode</th><th>Description</th><th>Baud Rate</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Shift RegisterF<sub>XTAL</sub>/12 (/6 in X2 mode)</td></tr><tr><td>0</td><td>1</td><td>1</td><td>8-bit UARTVariable</td></tr><tr><td>1</td><td>0</td><td>2</td><td>9-bit UARTF<sub>XTAL</sub>/64 or F<sub>XTAL</sub>/32 (/32, /16 in X2 mode)</td></tr><tr><td>1</td><td>1</td><td>3</td><td>9-bit UARTVariable</td></tr></table>	SM0	SM1Mode	Description	Baud Rate	0	0	0	Shift RegisterF <sub>XTAL</sub> /12 (/6 in X2 mode)	0	1	1	8-bit UARTVariable	1	0	2	9-bit UARTF <sub>XTAL</sub> /64 or F <sub>XTAL</sub> /32 (/32, /16 in X2 mode)	1	1	3	9-bit UARTVariable
SM0	SM1Mode	Description	Baud Rate																			
0	0	0	Shift RegisterF <sub>XTAL</sub> /12 (/6 in X2 mode)																			
0	1	1	8-bit UARTVariable																			
1	0	2	9-bit UARTF <sub>XTAL</sub> /64 or F <sub>XTAL</sub> /32 (/32, /16 in X2 mode)																			
1	1	3	9-bit UARTVariable																			
5	SM2	<b>Serial port Mode 2 bit / Multiprocessor Communication Enable bit</b> Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0.																				
4	REN	<b>Reception Enable bit</b> Clear to disable serial reception. Set to enable serial reception.																				
3	TB8	Transmitter Bit 8 / Ninth bit to transmit in modes 2 and 3. Clear to transmit a logic 0 in the 9th bit. Set to transmit a logic 1 in the 9th bit.																				
2	RB8	<b>Receiver Bit 8 / Ninth bit received in modes 2 and 3</b> Cleared by hardware if 9th bit received is a logic 0. Set by hardware if 9th bit received is a logic 1. In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used.																				
1	TI	<b>Transmit Interrupt flag</b> Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes.																				
0	RI	<b>Receive Interrupt flag</b> Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0, see Figure 9-2. and Figure 9-3. in the other modes.																				

Reset Value = 0000 0000b

Bit addressable

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

**Table 10-2.** IE Register  
IE - Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	-	ET2	ES	ET1	EX1	ET0	EX0

Bit Number	Bit Mnemonic	Description
7	EA	Enable All interrupt bit Clear to disable all interrupts. Set to enable all interrupts. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its own interrupt enable bit.
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
5	ET2	Timer 2 overflow interrupt Enable bit Clear to disable timer 2 overflow interrupt. Set to enable timer 2 overflow interrupt.
4	ES	Serial port Enable bit Clear to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	Timer 1 overflow interrupt Enable bit Clear to disable timer 1 overflow interrupt. Set to enable timer 1 overflow interrupt.
2	EX1	External interrupt 1 Enable bit Clear to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	Timer 0 overflow interrupt Enable bit Clear to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.
0	EX0	External interrupt 0 Enable bit Clear to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0X00 0000b

Bit addressable

## 11. Idle mode

An instruction that sets PCON.0 causes that to be the last instruction executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer, and Serial Port functions. The CPU status is preserved in its entirety : the Stack Pointer, Program Counter, Program Status Word, Accumulator and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels.

There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bits GF0 and GF1 can be used to give an indication if an interrupt occurred during normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

### 11.1 Power-Down Mode

To save maximum power, a power-down mode can be invoked by software (Refer to Table 9-4., PCON register).

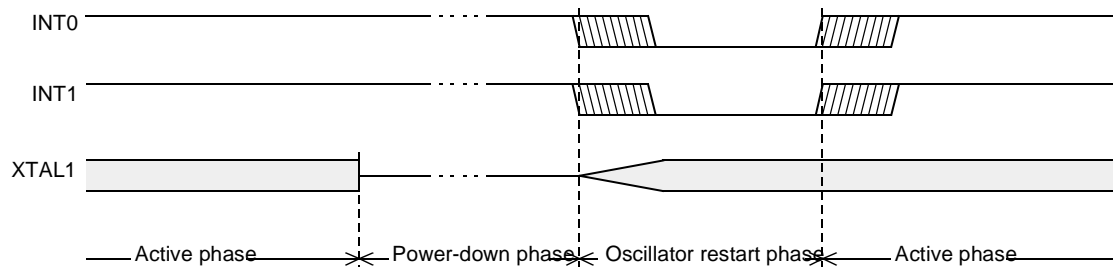
In power-down mode, the oscillator is stopped and the instruction that invoked power-down mode is the last instruction executed. The internal RAM and SFRs retain their value until the power-down mode is terminated.  $V_{CC}$  can be lowered to save further power. Either a hardware reset or an external interrupt can cause an exit from power-down. To properly terminate power-down, the reset or external interrupt should not be executed before  $V_{CC}$  is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.

Only external interrupts  $\overline{INT0}$  and  $\overline{INT1}$  are useful to exit from power-down. For that, interrupt must be enabled and configured as level or edge sensitive interrupt input.

Holding the pin low restarts the oscillator but bringing the pin high completes the exit as detailed in Figure 11-1. When both interrupts are enabled, the oscillator restarts as soon as one of the two inputs is held low and power down exit will be completed when the first input will be released. In this case the higher priority interrupt service routine is executed.

Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put TS80C54/58X2 into power-down mode.

**Figure 11-1.** Power-Down Exit Waveform



Exit from power-down by reset redefines all the SFRs, exit from power-down by external interrupt does not affect the SFRs.

Exit from power-down by either reset or external interrupt does not affect the internal RAM content.

*NOTE: If idle mode is activated with power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.*

**Table 11-1.** The state of ports during idle and power-down modes

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data*	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data*	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

\* Port 0 can force a "zero" level. A "one" Level will leave port floating.

## 12. Hardware Watchdog Timer

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upset. The WDT consists of a 14-bit counter and the WatchDog Timer ReSeT (WDTRST) SFR. The WDT is by default disabled from exiting reset. To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, it will increment every machine cycle while the oscillator is running and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST-pin.

### 12.1 Using the WDT

To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, the user needs to service it by writing to 01EH and 0E1H to WDTRST to avoid WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH) and this will reset the device. When WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycle. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST-pin. The RESET pulse duration is  $96 \times T_{OSC}$ , where  $T_{OSC} = 1/F_{OSC}$ . To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

To have a more powerful WDT, a  $2^7$  counter has been added to extend the Time-out capability, ranking from 16ms to 2s @  $F_{OSC} = 12\text{MHz}$ . To manage this feature, refer to WDTPRG register description, Table 12-2. (SFR0A7h).

**Table 12-1.** WDTRST Register  
WDTRST Address (0A6h)

	7	6	5	4	3	2	1
Reset value	X	X	X	X	X	X	X

Write only, this SFR is used to reset/enable the WDT by writing 01EH then 0E1H in sequence.

### 17.2.3 Signature bytes

The TS87C54/58X2 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in section 8.3.

## 17.3 EPROM Programming

### 17.3.1 Set-up modes

In order to program and verify the EPROM or to read the signature bytes, the TS87C54/58X2 is placed in specific set-up modes (See Figure 17-1.).

Control and program signals must be held at the levels indicated in Table 17-2.

### 17.3.2 Definition of terms








**Address Lines:** P1.0-P1.7, P2.0-P2.5, P3.4 respectively for A0-A14 (P2.5 (A13) for TS87C54X2, P3.4 (A14) for TS87C58X2).

**Data Lines:** P0.0-P0.7 for D0-D7

**Control Signals:** RST,  $\overline{\text{PSEN}}$ , P2.6, P2.7, P3.3, P3.6, P3.7.

**Program Signals:** ALE/ $\overline{\text{PROG}}$ ,  $\overline{\text{EA}}$ /VPP.

**Table 17-2.** EPROM Set-Up Modes

Mode	RST	PSEN	ALE/ $\overline{\text{PROG}}$	$\overline{\text{EA}}$ /VPP	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code data	1	0		12.75	0	1	1	1	1
Verify Code data	1	0	1	1	0		0	1	1
Program Encryption Array Address 0-3Fh	1	0		12.75	0	1	1	0	1
Read Signature Bytes	1	0	1	1	0		0	0	0
Program Lock bit 1	1	0		12.75	1	1	1	1	1
Program Lock bit 2	1	0		12.75	1	1	1	0	0
Program Lock bit 3	1	0		12.75	1	0	1	1	0

## 19.4 DC Parameters for Low Voltage

$T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ;  $V_{SS} = 0\text{ V}$ ;  $V_{CC} = 2.7\text{ V}$  to  $5.5\text{ V} \pm 10\%$ ;  $F = 0$  to  $30\text{ MHz}$ .

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ;  $V_{SS} = 0\text{ V}$ ;  $V_{CC} = 2.7\text{ V}$  to  $5.5\text{ V} \pm 10\%$ ;  $F = 0$  to  $30\text{ MHz}$ .

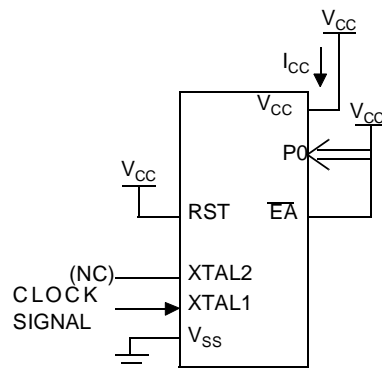
**Table 19-2.** DC Parameters for Low Voltage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$V_{IL}$	Input Low Voltage	-0.5		$0.2 V_{CC} - 0.1$	V	
$V_{IH}$	Input High Voltage except XTAL1, RST	$0.2 V_{CC} + 0.9$		$V_{CC} + 0.5$	V	
$V_{IH1}$	Input High Voltage, XTAL1, RST	$0.7 V_{CC}$		$V_{CC} + 0.5$	V	
$V_{OL}$	Output Low Voltage, ports 1, 2, 3 <sup>(6)</sup>			0.45	V	$I_{OL} = 0.8\text{ mA}^{(4)}$
$V_{OL1}$	Output Low Voltage, port 0, ALE, $\overline{\text{PSEN}}$ <sup>(6)</sup>			0.45	V	$I_{OL} = 1.6\text{ mA}^{(4)}$
$V_{OH}$	Output High Voltage, ports 1, 2, 3	$0.9 V_{CC}$			V	$I_{OH} = -10\text{ }\mu\text{A}$
$V_{OH1}$	Output High Voltage, port 0, ALE, $\overline{\text{PSEN}}$	$0.9 V_{CC}$			V	$I_{OH} = -40\text{ }\mu\text{A}$
$I_{IL}$	Logical 0 Input Current ports 1, 2 and 3			-50	$\mu\text{A}$	$V_{in} = 0.45\text{ V}$
$I_{LI}$	Input Leakage Current			$\pm 10$	$\mu\text{A}$	$0.45\text{ V} < V_{in} < V_{CC}$
$I_{TL}$	Logical 1 to 0 Transition Current, ports 1, 2, 3			-650	$\mu\text{A}$	$V_{in} = 2.0\text{ V}$
$R_{RST}$	RST Pulldown Resistor	50	90 <sup>(5)</sup>	200	k $\Omega$	
CIO	Capacitance of I/O Buffer			10	pF	$F_c = 1\text{ MHz}$ $T_A = 25^\circ\text{C}$
$I_{PD}$	Power Down Current		20 <sup>(5)</sup> 10 <sup>(5)</sup>	50 30	$\mu\text{A}$	$V_{CC} = 2.0\text{ V}$ to $5.5\text{ V}^{(3)}$ $V_{CC} = 2.0\text{ V}$ to $3.3\text{ V}^{(3)}$
$I_{CC}$ under RESET	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			1 + 0.2 Freq (MHz) @12MHz 3.4 @16MHz 4.2	mA	$V_{CC} = 3.3\text{ V}^{(1)}$
$I_{CC}$ operating	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			1 + 0.3 Freq (MHz) @12MHz 4.6 @16MHz 5.8	mA	$V_{CC} = 3.3\text{ V}^{(8)}$
$I_{CC}$ idle	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			0.15 Freq (MHz) + 0.2 @12MHz 2 @16MHz 2.6	mA	$V_{CC} = 3.3\text{ V}^{(2)}$

- $I_{CC}$  under reset is measured with all output pins disconnected; XTAL1 driven with  $T_{CLCH}$ ,  $T_{CHCL} = 5\text{ ns}$  (see Figure 19-5.),  $V_{IL} = V_{SS} + 0.5\text{ V}$ ,  $V_{IH} = V_{CC} - 0.5\text{ V}$ ; XTAL2 N.C.;  $\overline{\text{EA}} = \text{RST} = \text{Port 0} = V_{CC}$ .  $I_{CC}$  would be slightly higher if a crystal oscillator used..
- Idle  $I_{CC}$  is measured with all output pins disconnected; XTAL1 driven with  $T_{CLCH}$ ,  $T_{CHCL} = 5\text{ ns}$ ,  $V_{IL} = V_{SS} + 0.5\text{ V}$ ,  $V_{IH} = V_{CC} - 0.5\text{ V}$ ; XTAL2 N.C.; Port 0 =  $V_{CC}$ ;  $\overline{\text{EA}} = \text{RST} = V_{SS}$  (see Figure 19-3.).
- Power Down  $I_{CC}$  is measured with all output pins disconnected;  $\overline{\text{EA}} = V_{SS}$ , PORT 0 =  $V_{CC}$ ; XTAL2 NC.; RST =  $V_{SS}$  (see Figure 19-4.).
- Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the  $V_{OL}$ s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100pF), the noise pulse on the ALE line may exceed 0.45V with maxi  $V_{OL}$  peak 0.6V. A Schmitt Trigger use is not necessary.

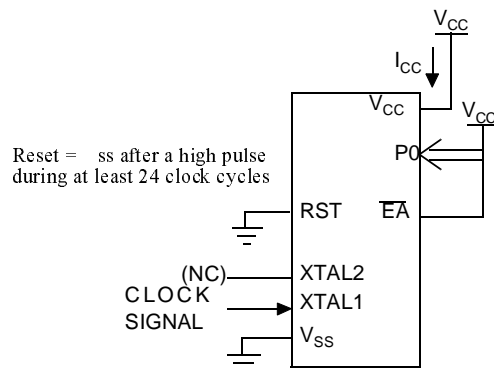
5. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
6. Under steady state (non-transient) conditions,  $I_{OL}$  must be externally limited as follows:  
 Maximum  $I_{OL}$  per port pin: 10 mA  
 Maximum  $I_{OL}$  per 8-bit port:  
 Port 0: 26 mA  
 Ports 1, 2 and 3: 15 mA  
 Maximum total  $I_{OL}$  for all output pins: 71 mA  
 If  $I_{OL}$  exceeds the test condition,  $V_{OL}$  may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
7. For other values, please contact your sales office.
8. Operating  $I_{CC}$  is measured with all output pins disconnected; XTAL1 driven with  $T_{CLCH}$ ,  $T_{CHCL} = 5$  ns (see Figure 19-5.),  $V_{IL} = V_{SS} + 0.5$  V,  
 $V_{IH} = V_{CC} - 0.5$  V; XTAL2 N.C.;  $\overline{EA} = \text{Port 0} = V_{CC}$ ; RST =  $V_{SS}$ . The internal ROM runs the code 80 FE (label: SJMP label).  $I_{CC}$  would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.

**Figure 19-1.**  $I_{CC}$  Test Condition, under reset



All other pins are disconnected.

**Figure 19-2.** Operating  $I_{CC}$  Test Condition



All other pins are disconnected.



## 19.5.4 External Data Memory Characteristics

**Table 19-8.** Symbol Description

Symbol	Parameter
$T_{RLRH}$	$\overline{RD}$ Pulse Width
$T_{WLWH}$	$\overline{WR}$ Pulse Width
$T_{RLDV}$	$\overline{RD}$ to Valid Data In
$T_{RHDx}$	Data Hold After $\overline{RD}$
$T_{RHDZ}$	Data Float After $\overline{RD}$
$T_{LLDV}$	ALE to Valid Data In
$T_{AVDV}$	Address to Valid Data In
$T_{LLWL}$	ALE to $\overline{WR}$ or $\overline{RD}$
$T_{AVWL}$	Address to $\overline{WR}$ or $\overline{RD}$
$T_{QVWX}$	Data Valid to $\overline{WR}$ Transition
$T_{QVWH}$	Data set-up to $\overline{WR}$ High
$T_{WHQX}$	Data Hold After $\overline{WR}$
$T_{RLAZ}$	$\overline{RD}$ Low to Address Float
$T_{WHLH}$	$\overline{RD}$ or $\overline{WR}$ High to ALE high

**Table 19-9.** AC Parameters for a Fix Clock

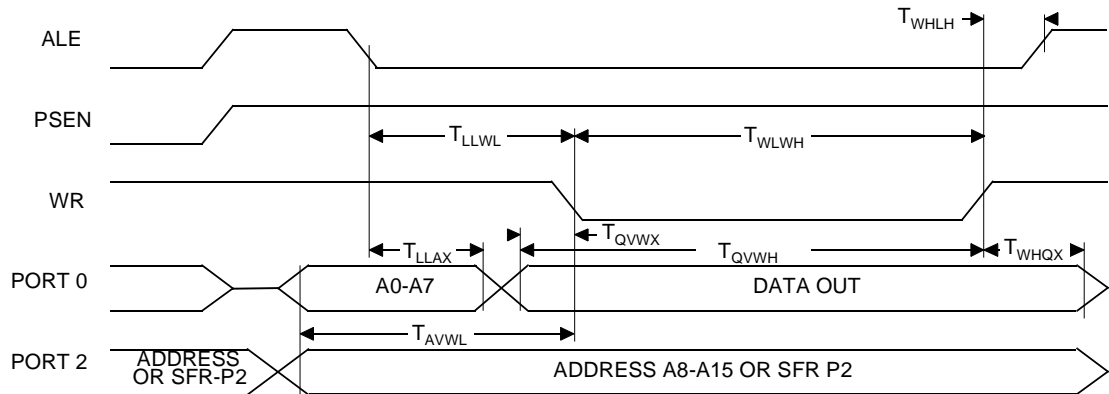
Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$T_{RLRH}$	130		85		135		125		175		ns
$T_{WLWH}$	130		85		135		125		175		ns
$T_{RLDV}$		100		60		102		95		137	ns
$T_{RHDx}$	0		0		0		0		0		ns
$T_{RHDZ}$		30		18		35		25		42	ns
$T_{LLDV}$		160		98		165		155		222	ns
$T_{AVDV}$		165		100		175		160		235	ns
$T_{LLWL}$	50	100	30	70	55	95	45	105	70	130	ns
$T_{AVWL}$	75		47		80		70		103		ns
$T_{QVWX}$	10		7		15		5		13		ns
$T_{QVWH}$	160		107		165		155		213		ns
$T_{WHQX}$	15		9		17		10		18		ns
$T_{RLAZ}$		0		0		0		0		0	ns
$T_{WHLH}$	10	40	7	27	15	35	5	45	13	53	ns

**Table 19-10.** AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
$T_{RLRH}$	Min	6 T - x	3 T - x	20	15	25	ns
$T_{WLWH}$	Min	6 T - x	3 T - x	20	15	25	ns
$T_{RLDV}$	Max	5 T - x	2.5 T - x	25	23	30	ns
$T_{RHDZ}$	Min	x	x	0	0	0	ns
$T_{RHDZ}$	Max	2 T - x	T - x	20	15	25	ns
$T_{LLDV}$	Max	8 T - x	4 T - x	40	35	45	ns
$T_{AVDV}$	Max	9 T - x	4.5 T - x	60	50	65	ns
$T_{LLWL}$	Min	3 T - x	1.5 T - x	25	20	30	ns
$T_{LLWL}$	Max	3 T + x	1.5 T + x	25	20	30	ns
$T_{AVWL}$	Min	4 T - x	2 T - x	25	20	30	ns
$T_{QVWX}$	Min	T - x	0.5 T - x	15	10	20	ns
$T_{QVWH}$	Min	7 T - x	3.5 T - x	15	10	20	ns
$T_{WHQX}$	Min	T - x	0.5 T - x	10	8	15	ns
$T_{RLAZ}$	Max	x	x	0	0	0	ns
$T_{WHLH}$	Min	T - x	0.5 T - x	15	10	20	ns
$T_{WHLH}$	Max	T + x	0.5 T + x	15	10	20	ns

### 19.5.5 External Data Memory Write Cycle

**Figure 19-7.** External Data Memory Write Cycle



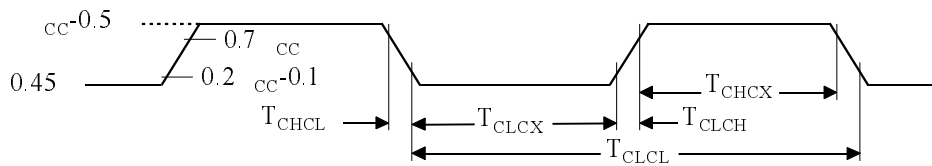
### 19.5.11 External Clock Drive Characteristics (XTAL1)

Table 19-15. AC Parameters

Symbol	Parameter	Min	Max	Units
$T_{CLCL}$	Oscillator Period	25		ns
$T_{CHCX}$	High Time	5		ns
$T_{CLCX}$	Low Time	5		ns
$T_{CLCH}$	Rise Time		5	ns
$T_{CHCL}$	Fall Time		5	ns
$T_{CHCX}/T_{CLCX}$	Cyclic ratio in X2 mode	40	60	%

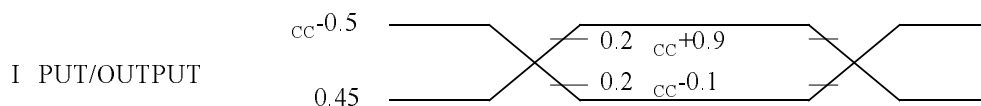
### 19.5.12 External Clock Drive Waveforms

Figure 19-11. External Clock Drive Waveforms



### 19.5.13 AC Testing Input/Output Waveforms

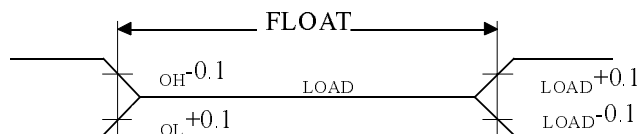
**Figure 19-12. AC Testing Input/Output Waveforms**



AC inputs during testing are driven at  $V_{CC} - 0.5$  for a logic "1" and 0.45V for a logic "0". Timing measurement are made at  $V_{IH}$  min for a logic "1" and  $V_{IL}$  max for a logic "0".

### 19.5.14 Float Waveforms

**Figure 19-13. Float Waveforms**



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded  $V_{OH}/V_{OL}$  level occurs.  $I_{OL}/I_{OH} \geq \pm 20\text{mA}$ .

### 19.5.15 Clock Waveforms

Valid in normal clock mode. In X2 mode XTAL2 signal must be changed to XTAL2 divided by two.

Part Number	Supply Voltage	Temperature Range	Package	Packing
TS87C54X2-MCC	5V ±10%	Commercial	PQFP44	Tray
TS87C54X2-MCE	5V ±10%	Commercial	VQFP44	Tray
TS87C54X2-VCA	5V ±10%	Commercial	PDIL40	Stick
TS87C54X2-VCB	5V ±10%	Commercial	PLCC44	Stick
TS87C54X2-VCC	5V ±10%	Commercial	PQFP44	Tray
TS87C54X2-VCE	5V ±10%	Commercial	VQFP44	Tray
TS87C54X2-LCA	2.7 to 5.5V	Commercial	PDIL40	Stick
TS87C54X2-LCB	2.7 to 5.5V	Commercial	PLCC44	Stick
TS87C54X2-LCC	2.7 to 5.5V	Commercial	PQFP44	Tray
TS87C54X2-LCE	2.7 to 5.5V	Commercial	VQFP44	Tray
TS87C54X2-MIA	5V ±10%	Industrial	PDIL40	Stick
TS87C54X2-MIB	5V ±10%	Industrial	PLCC44	Stick
TS87C54X2-MIC	5V ±10%	Industrial	PQFP44	Tray
TS87C54X2-MIE	5V ±10%	Industrial	VQFP44	Tray
TS87C54X2-VIA	5V ±10%	Industrial	PDIL40	Stick
TS87C54X2-VIB	5V ±10%	Industrial	PLCC44	Stick
TS87C54X2-VIC	5V ±10%	Industrial	PQFP44	Tray
TS87C54X2-VIE	5V ±10%	Industrial	VQFP44	Tray
TS87C54X2-LIA	2.7 to 5.5V	Industrial	PDIL40	Stick
TS87C54X2-LIB	2.7 to 5.5V	Industrial	PLCC44	Stick
TS87C54X2-LIC	2.7 to 5.5V	Industrial	PQFP44	Tray
TS87C54X2-LIE	2.7 to 5.5V	Industrial	VQFP44	Tray
AT87C54X2-3CSUM	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C54X2-SLSUM	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C54X2-RLTUM	5V ±10%	Industrial & Green	VQFP44	Tray
AT87C54X2-3CSUL	2.7 to 5.5V	Industrial & Green	PDIL40	Stick
AT87C54X2-SLSUL	2.7 to 5.5V	Industrial & Green	PLCC44	Stick
AT87C54X2-RLTUL	2.7 to 5.5V	Industrial & Green	VQFP44	Tray
AT87C54X2-3CSUV	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C54X2-SLSUV	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C54X2-RLTUV	5V ±10%	Industrial & Green	VQFP44	Tray