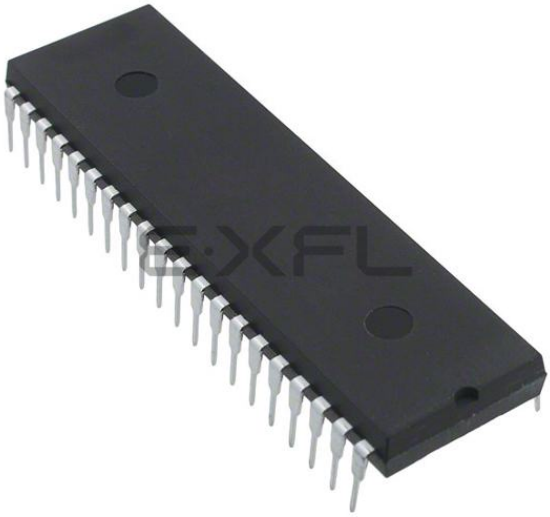

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	30/20MHz
Connectivity	UART/USART
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIL
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts87c58x2-lia

4. SFR Mapping

The Special Function Registers (SFRs) of the TS80C54/58X2 fall into the following categories:

- C51 core registers: ACC, B, DPH, DPL, PSW, SP, AUXR1
- I/O port registers: P0, P1, P2, P3
- Timer registers: T2CON, T2MOD, TCON, TH0, TH1, TH2, TMOD, TL0, TL1, TL2, RCAP2L, RCAP2H
- Serial I/O port registers: SADDR, SADEN, SBUF, SCON
- Power and clock control registers: PCON
- HDW Watchdog Timer Reset: WDTRST, WDTPRG
- Interrupt system registers: IE, IP, IPH
- Others: AUXR, CKCON

Table 4-1. All SFRs with their address and their reset value

	Bit address-able	**Non Bit addressable**							
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h									FFh
F0h	B 0000 0000								F7h
E8h									EFh
E0h	ACC 0000 0000								E7h
D8h									DFh
D0h	PSW 0000 0000								D7h
C8h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			CFh
C0h									C7h
B8h	IP XX00 0000	SADEN 0000 0000							BFh
B0h	P3 1111 1111							IPH XX00 0000	B7h
A8h	IE 0X00 0000	SADDR 0000 0000							AFh
A0h	P2 1111 1111		AUXR1 XXXX 0XX0				WDTRST XXXX XXXX	WDTPRG XXXX X000	A7h
98h	SCON 0000 0000	SBUF XXXX XXXX							9Fh
90h	P1 1111 1111								97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XXXX XXX0	CKCON XXXX XXX0	8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00X1 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

reserved

Table 5-1. Pin Description for 40/44 pin packages

MNEMONIC	PIN NUMBER			TYPE	Name And Function
	DIL	LCC	VQFP 1.4		
V_{SS}	20	22	16	I	**Ground:** 0V reference
Vss1		1	39	I	Optional Ground: **Contact the Sales Office for ground connection.**
V_{CC}	40	44	38	I	**Power Supply:** This is the power supply voltage for normal, idle and power-down operation
P0.0-P0.7	39-32	43-36	37-30	I/O	**Port 0**: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. Port 0 pins must be polarized to Vcc or Vss in order to prevent any parasitic current consumption. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-up when emitting 1s. Port 0 also inputs the code bytes during EPROM programming. External pull-ups are required during program verification during which P0 outputs the code bytes.
P1.0-P1.7	1-8	2-9	40-44 1-3	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups. Port 1 also receives the low-order address byte during memory programming and verification. Alternate functions for Port 1 include:
	1	2	40	I/O	**T2 (P1.0):** Timer/Counter 2 external count input/Clockout
	2	3	41	I	**T2EX (P1.1):** Timer/Counter 2 Reload/Capture/Direction Control
P2.0-P2.7	21-28	24-31	18-25	I/O	**Port 2**: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR).In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 emits the contents of the P2 SFR. Some Port 2 pins receive the high order address bits during EPROM programming and verification: P2.0 to P2.5 for A8 to A13
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Some Port 3 pin P3.4 receive the high order address bits during EPROM programming and verification for TS8xC58X2 devices. Port 3 also serves the special features of the 80C51 family, as listed below.
	10	11	5	I	**RXD (P3.0):** Serial input port
	11	13	7	O	**TXD (P3.1):** Serial output port
	12	14	8	I	**$\overline{\text{INT0}}$ (P3.2):** External interrupt 0
	13	15	9	I	**$\overline{\text{INT1}}$ (P3.3):** External interrupt 1
	14	16	10	I	**T0 (P3.4):** Timer 0 external input
	15	17	11	I	**T1 (P3.5):** Timer 1 external input
	16	18	12	O	**$\overline{\text{WR}}$ (P3.6):** External data memory write strobe
	17	19	13	O	**$\overline{\text{RD}}$ (P3.7):** External data memory read strobe P3.4 also receives A14 during TS87C58X2 EPROM Programming.
Reset	9	10	4	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC}.

6. TS80C54/58X2 Enhanced Features

In comparison to the original 80C52, the TS80C54/58X2 implements some new features, which are:

- The X2 option.
- The Dual Data Pointer.
- The Watchdog.
- The 4 level interrupt priority system.
- The power-off flag.
- The ONCE mode.
- The ALE disabling.
- Some enhanced features are also located in the UART and the timer 2.

6.1 X2 Feature

The TS80C54/58X2 core needs only 6 clock periods per machine cycle. This feature called ”X2” provides the following advantages:

- Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power.
- Save power consumption while keeping same CPU power (oscillator power saving).
- Save power consumption by dividing dynamically operating frequency by 2 in operating and idle modes.
- Increase CPU power by 2 while keeping same crystal frequency.

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

6.1.1 Description

The clock for the whole circuit and peripheral is first divided by two before being used by the CPU core and peripherals. This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%. Figure 6-2. shows the clock generation block diagram. X2 bit is validated on XTAL1÷2 rising edge to avoid glitches when switching from X2 to STD mode. Figure 6-2. shows the mode switching waveforms.

Figure 6-1. Clock Generation Diagram

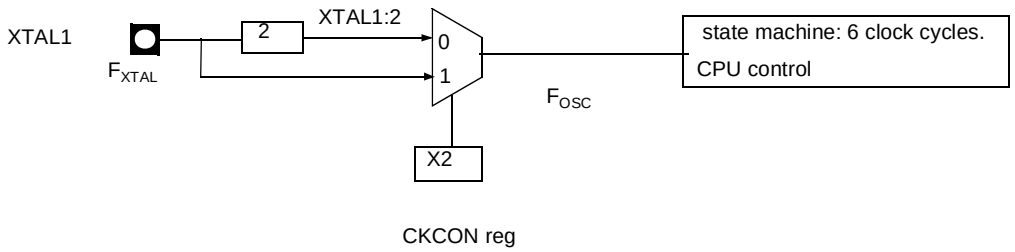


Table 7-1. AUXR1: Auxiliary Register 1

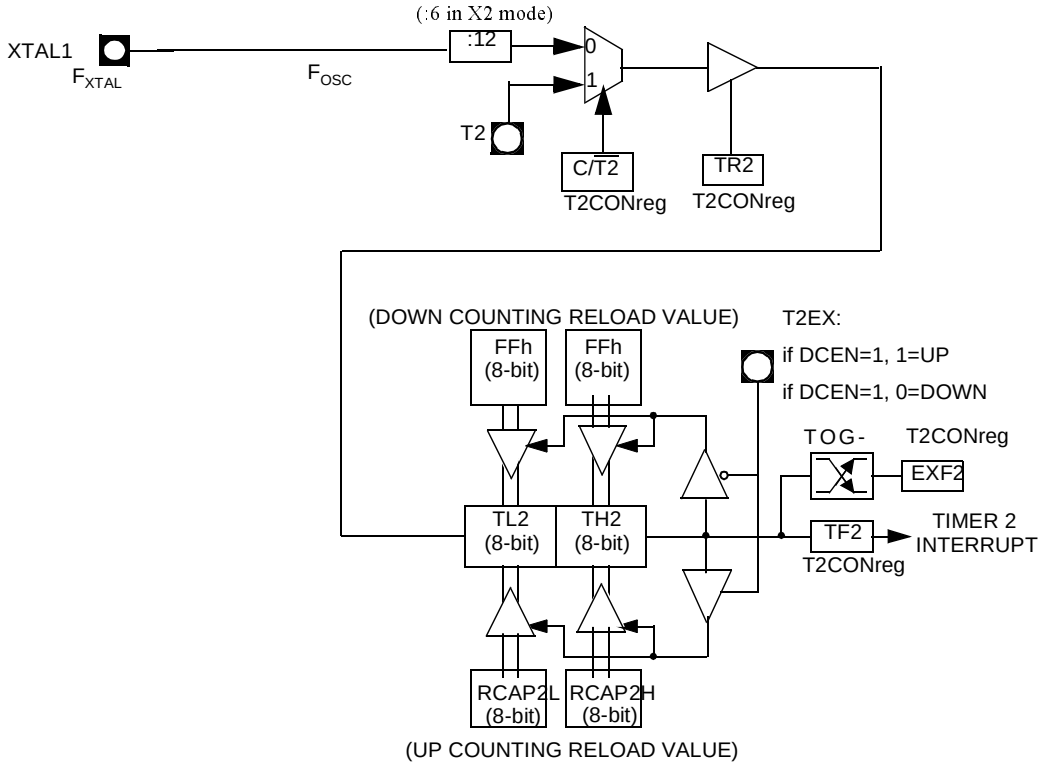
7	6	5	4	3	2	1	0
-	-	-	-	GF3	0	-	DPS

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	GF3	This bit is a general purpose user flag
2	0	**Reserved** Always stuck at 0.
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	DPS	**Data Pointer Selection** Clear to select DPTR0. Set to select DPTR1.

Reset Value = XXXX 00X0
Not bit addressable

User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new feature. In that case, the reset value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

Figure 8-1. Auto-Reload Mode Up/Down Counter (DCEN = 1)



8.1.1 Programmable Clock-Output

In the clock-out mode, timer 2 operates as a 50%-duty-cycle, programmable clock generator (See Figure 8-2) . The input clock increments TL2 at frequency $F_{OSC}/2$. The timer repeatedly counts to overflow from a loaded value. At overflow, the contents of RCAP2H and RCAP2L registers are loaded into TH2 and TL2. In this mode, timer 2 overflows do not generate interrupts. The formula gives the clock-out frequency as a function of the system oscillator frequency and the value in the RCAP2H and RCAP2L registers :

$$Clock-OutFrequency = \frac{F_{osc}}{4 \times (65536 - RCAP2H/RCAP2L)}$$

For a 16 MHz system clock, timer 2 has a programmable frequency range of 61 Hz ($F_{OSC}/2^{16)}$ to 4 MHz ($F_{OSC}/4$). The generated clock signal is brought out to T2 pin (P1.0).

Timer 2 is programmed for the clock-out mode as follows:

- Set T2OE bit in T2MOD register.
- Clear C/$\overline{T2}$ bit in T2CON register.
- Determine the 16-bit reload value from the formula and enter it in RCAP2H/RCAP2L registers.

Table 8-2. T2MOD Register

T2MOD - Timer 2 Mode Control Register (C9h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	T2OE	DCEN

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	T2OE	**Timer 2 Output Enable bit** Clear to program P1.0/T2 as clock input or I/O port. Set to program P1.0/T2 as clock output.
0	DCEN	**Down Counter Enable bit** Clear to disable timer 2 as up/down counter. Set to enable timer 2 as up/down counter.

Reset Value = XXXX XX00b

Not bit addressable

Table 9-4. PCON Register

Table 9-5. PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	**SMOD0**	**-**	**POF**	**GF1**	**GF0**	**PD**	**IDL**

Bit Number	Bit Mnemonic	Description
7	SMOD1	**Serial port Mode bit 1** Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	**Serial port Mode bit 0** Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	POF	**Power-Off Flag** Clear to recognize next reset type. Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	**Power-Down mode bit** Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	**Idle mode bit** Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b
Not bit addressable

Power-off flag reset value will be 1 only after a power on (cold reset). A warm reset doesn't affect the value of this bit.

12. Hardware Watchdog Timer

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upset. The WDT consists of a 14-bit counter and the WatchDog Timer ReSeT (WDTRST) SFR. The WDT is by default disabled from exiting reset. To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, it will increment every machine cycle while the oscillator is running and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST-pin.

12.1 Using the WDT

To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, the user needs to service it by writing to 01EH and 0E1H to WDTRST to avoid WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH) and this will reset the device. When WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycle. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST-pin. The RESET pulse duration is 96 x T_{OSC} , where T_{OSC} = $1/F_{OSC}$. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

To have a more powerful WDT, a 2^7 counter has been added to extend the Time-out capability, ranking from 16ms to 2s @ F_{OSC} = 12MHz. To manage this feature, refer to WDTPRG register description, Table 12-2. (SFR0A7h).

Table 12-1. WDTRST Register
WDTRST Address (0A6h)

	7	6	5	4	3	2	1
Reset value	X	X	X	X	X	X	X

Write only, this SFR is used to reset/enable the WDT by writing 01EH then 0E1H in sequence.

Table 12-2. WDTPRG Register
WDTPRG Address (0A7h)

7	6	5	4	3	2	1	0
T4	T3	T2	T1	T0	S2	S1	S0

Bit Number	Bit Mnemonic	Description
7	T4	**Reserved** Do not try to set or clear this bit.
6	T3	
5	T2	
4	T1	
3	T0	
2	S2	WDT Time-out select bit 2
1	S1	WDT Time-out select bit 1
0	S0	WDT Time-out select bit 0
		S2S1 S0 Selected Time-out 0 0 0 (2^{14} - 1) machine cycles, 16.3 ms @ 12 MHz 0 0 1 (2^{15} - 1) machine cycles, 32.7 ms @ 12 MHz 0 1 0 (2^{16} - 1) machine cycles, 65.5 ms @ 12 MHz 0 1 1 (2^{17} - 1) machine cycles, 131 ms @ 12 MHz 1 0 0 (2^{18} - 1) machine cycles, 262 ms @ 12 MHz 1 0 1 (2^{19} - 1) machine cycles, 542 ms @ 12 MHz 1 1 0 (2^{20} - 1) machine cycles, 1.05 s @ 12 MHz 1 1 1 (2^{21} - 1) machine cycles, 2.09 s @ 12 MHz

Reset value XXXX X000

12.1.1 WDT during Power Down and Idle

In Power Down mode the oscillator stops, which means the WDT also stops. While in Power Down mode the user does not need to service the WDT. There are 2 methods of exiting Power Down mode: by a hardware reset or via a level activated external interrupt which is enabled prior to entering Power Down mode. When Power Down is exited with hardware reset, servicing the WDT should occur as it normally should whenever the TS80C54/58X2 is reset. Exiting Power Down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service routine.

To ensure that the WDT does not overflow within a few states of exiting of powerdown, it is best to reset the WDT just before entering powerdown.

In the Idle mode, the oscillator continues to run. To prevent the WDT from resetting the TS80C54/58X2 while in Idle mode, the user should always set up a timer that will periodically exit Idle, service the WDT, and re-enter Idle mode.

13. ONCE™ Mode (ON Chip Emulation)

The ONCE mode facilitates testing and debugging of systems using TS80C54/58X2 without removing the circuit from the board. The ONCE mode is invoked by driving certain pins of the TS80C54/58X2; the following sequence must be exercised:

- Pull ALE low while the device is in reset (RST high) and $\overline{\text{PSEN}}$ is high.
- Hold ALE low as RST is deactivated.

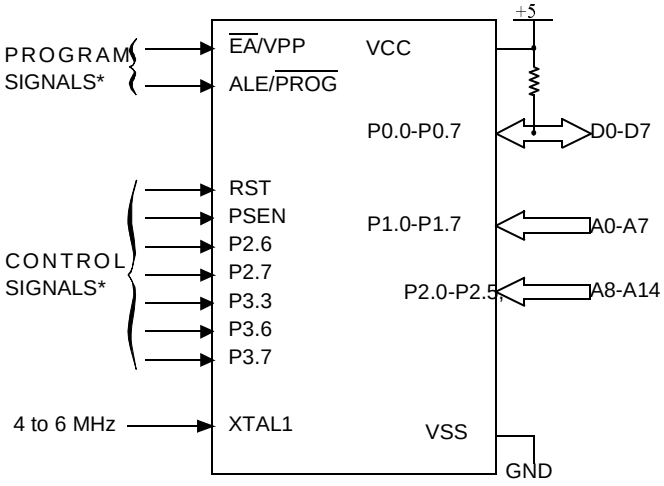
While the TS80C54/58X2 is in ONCE mode, an emulator or test CPU can be used to drive the circuit Table 13-1 shows the status of the port pins during ONCE mode.

Normal operation is restored when normal reset is applied.

Table 13-1. External Pin Status during ONCE Mode

ALE	PSEN	Port 0	Port 1	Port 2	Port 3	XTAL1/2
Weak pull-up	Weak pull-up	Float	Weak pull-up	Weak pull-up	Weak pull-up	Active

Figure 17-1. Set-Up Modes Configuration



* See Table 31. for proper value on these inputs

17.3.3 Programming Algorithm

The Improved Quick Pulse algorithm is based on the Quick Pulse algorithm and decreases the number of pulses applied during byte programming from 25 to 1.

To program the TS80C54/58X2 the following sequence must be exercised:

- Step 1: Activate the combination of control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Input the appropriate data on the data lines.
- Step 4: Raise $\overline{EA}$/VPP from VCC to VPP (typical 12.75V).
- Step 5: Pulse ALE/$\overline{PROG}$ once.
- Step 6: Lower $\overline{EA}$/VPP from VPP to VCC

Repeat step 2 through 6 changing the address and data for the entire array or until the end of the object file is reached (See Figure 17-2.).

17.3.4 Verify algorithm

Code array verify must be done after each byte or block of bytes is programmed. In either case, a complete verify of the programmed array will ensure reliable programming of the TS87C54/58X2.

P 2.7 is used to enable data output.

To verify the TS87C54/58X2 code the following sequence must be exercised:

- Step 1: Activate the combination of program and control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Read data on the data lines.

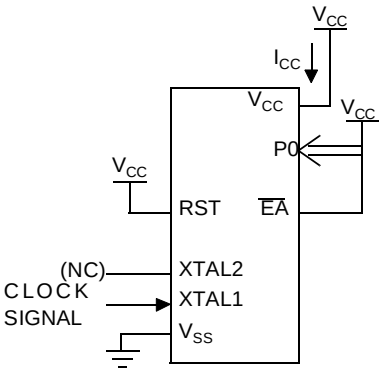
Repeat step 2 through 3 changing the address for the entire array verification (See Figure 17-2.)

Table 18-1. Signature Bytes Content

Location	Contents	Comment
30h	58h	Manufacturer Code: Atmel Wireless & Microcontrollers
31h	57h	Family Code: C51 X2
60h	37h	Product name: TS80C58X2
60h	B7h	Product name: TS87C58X2
60h	3Bh	Product name: TS80C54X2
60h	BBh	Product name: TS87C54X2
61h	FFh	Product revision number

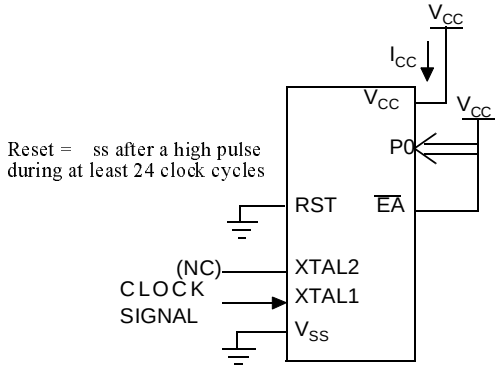
5. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
6. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:
   Port 0: 26 mA
   Ports 1, 2 and 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
7. For other values, please contact your sales office.
8. Operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH}, T_{CHCL} = 5 ns (see Figure 19-5.), $V_{IL} = V_{SS} + 0.5$ V,
   $V_{IH} = V_{CC} - 0.5$V; XTAL2 N.C.; $\overline{EA}$ = Port 0 = V_{CC}; RST = V_{SS}. The internal ROM runs the code 80 FE (label: SJMP label). I_{CC} would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.

Figure 19-1. I_{CC} Test Condition, under reset



All other pins are disconnected.

Figure 19-2. Operating I_{CC} Test Condition



All other pins are disconnected.

19.5 AC Parameters

19.5.1 Explanation of the AC Symbols

Each timing symbol has 5 characters. The first character is always a “T” (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example:T_{AVLL} = Time for Address Valid to ALE Low.
T_{LLPL} = Time for ALE Low to $\overline{PSEN}$ Low.

T_A = 0 to +70°C (commercial temperature range); V_{SS} = 0 V; V_{CC} = 5 V ± 10%; -M and -V ranges.
T_A = -40°C to +85°C (industrial temperature range); V_{SS} = 0 V; V_{CC} = 5 V ± 10%; -M and -V ranges.
T_A = 0 to +70°C (commercial temperature range); V_{SS} = 0 V; 2.7 V < V_{CC} < 5.5 V; -L range.
T_A = -40°C to +85°C (industrial temperature range); V_{SS} = 0 V; 2.7 V < V_{CC} < 5.5 V; -L range.

Table 19-3. gives the maximum applicable load capacitance for Port 0, Port 1, 2 and 3, and ALE and $\overline{PSEN}$ signals. Timings will be guaranteed if these capacitances are respected. Higher capacitance values can be used, but timings will then be degraded.

Table 19-3. Load Capacitance versus speed range, in pF

	-M	-V	-L
Port 0	100	50	100
Port 1, 2, 3	80	50	80
ALE / $\overline{PSEN}$	100	30	100

Table 19-5., Table 19-8. and Table 19-11. give the description of each AC symbols.

Table 19-6., Table 19-9. and Table 19-12. give for each range the AC parameter.

Table 19-7., Table 19-10. and Table 19-13. give the frequency derating formula of the AC parameter. To calculate each AC symbols, take the x value corresponding to the speed grade you need (-M, -V or -L) and replace this value in the formula. Values of the frequency must be limited to the corresponding speed grade:

Table 19-4. Max frequency for derating formula regarding the speed grade

	-M X1 mode	-M X2 mode	-V X1 mode	-V X2 mode	-L X1 mode	-L X2 mode
Freq (MHz)	40	20	40	30	30	20
T (ns)	25	50	25	33.3	33.3	50

Example:

T_{LLIV} in X2 mode for a -V part at 20 MHz (T = $1/20^{E6}$ = 50 ns):

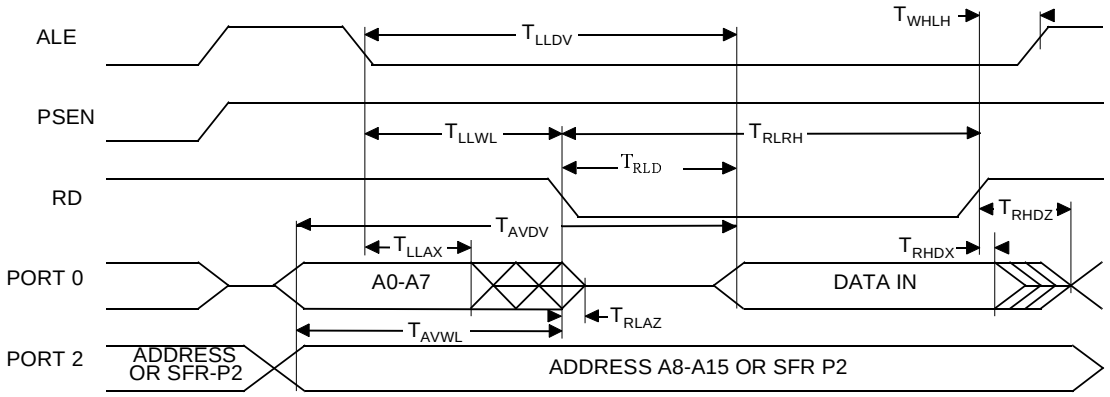
x= 22 (Table 19-7.)

T= 50ns

T_{LLIV}= 2T - x = 2 x 50 - 22 = 78ns

19.5.6 External Data Memory Read Cycle

Figure 19-8. External Data Memory Read Cycle



19.5.7 Serial Port Timing - Shift Register Mode

Table 19-11. Symbol Description

Symbol	Parameter
T_{XLXL}	Serial port clock cycle time
T_{QVHX}	Output data set-up to clock rising edge
T_{XHQX}	Output data hold after clock rising edge
T_{XHDX}	Input data hold after clock rising edge
T_{XHDV}	Clock rising edge to input data valid

Table 19-12. AC Parameters for a Fix Clock

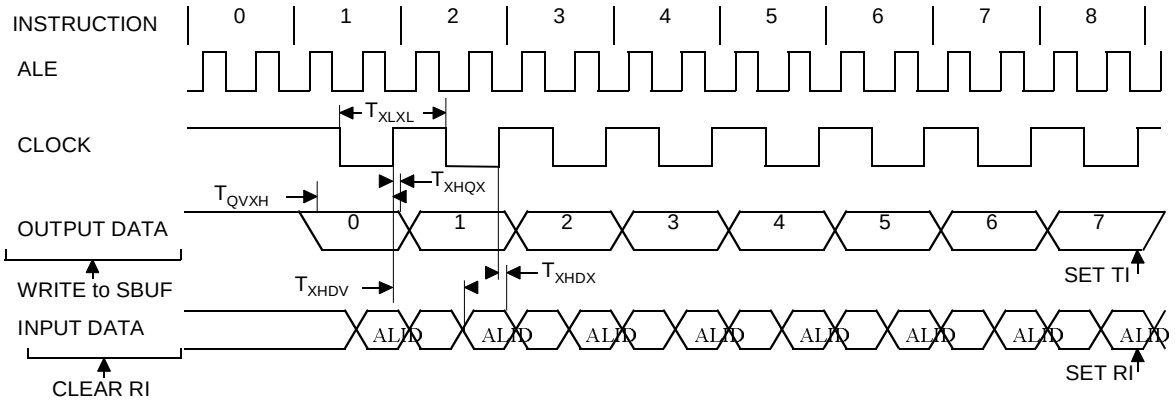
Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
Symbol	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
T_{XLXL}	300		200		300		300		400		ns
T_{QVHX}	200		117		200		200		283		ns
T_{XHQX}	30		13		30		30		47		ns
T_{XHDX}	0		0		0		0		0		ns
T_{XHDV}		117		34		117		117		200	ns

Table 19-13. AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
T_{XLXL}	Min	12 T	6 T				ns
T_{QVHX}	Min	10 T - x	5 T - x	50	50	50	ns
T_{XHQX}	Min	2 T - x	T - x	20	20	20	ns
T_{XHDX}	Min	x	x	0	0	0	ns
T_{XHDV}	Max	10 T - x	5 T- x	133	133	133	ns

19.5.8 Shift Register Timing Waveforms

Figure 19-9. Shift Register Timing Waveforms



Part Number	Supply Voltage	Temperature Range	Package	Packing
TS80C58X2xxx-MCA	-5 to +/-10%	Commercial	PDIL40	Stick
TS80C58X2xxx-MCB	-5 to +/-10%	Commercial	PLCC44	Stick
TS80C58X2xxx-MCC	-5 to +/-10%	Commercial	PQFP44	Tray
TS80C58X2xxx-MCE	-5 to +/-10%	Commercial	VQFP44	Tray
TS80C58X2xxx-VCA	-5 to +/-10%	Commercial	PDIL40	Stick
TS80C58X2xxx-VCB	-5 to +/-10%	Commercial	PLCC44	Stick
TS80C58X2xxx-VCC	-5 to +/-10%	Commercial	PQFP44	Tray
TS80C58X2xxx-VCE	-5 to +/-10%	Commercial	VQFP44	Tray
TS80C58X2xxx-LCA	-5 to +/-10%	Commercial	PDIL40	Stick
TS80C58X2xxx-LCB	-5 to +/-10%	Commercial	PLCC44	Stick
TS80C58X2xxx-LCC	-5 to +/-10%	Commercial	PQFP44	Tray
TS80C58X2xxx-LCE	-5 to +/-10%	Commercial	VQFP44	Tray
TS80C58X2xxx-MIA	-5 to +/-10%	Industrial	PDIL40	Stick
TS80C58X2xxx-MIB	-5 to +/-10%	Industrial	PLCC44	Stick
TS80C58X2xxx-MIC	-5 to +/-10%	Industrial	PQFP44	Tray
TS80C58X2xxx-MIE	-5 to +/-10%	Industrial	VQFP44	Tray
TS80C58X2xxx-VIA	-5 to +/-10%	Industrial	PDIL40	Stick
TS80C58X2xxx-VIB	-5 to +/-10%	Industrial	PLCC44	Stick
TS80C58X2xxx-VIC	-5 to +/-10%	Industrial	PQFP44	Tray
TS80C58X2xxx-VIE	-5 to +/-10%	Industrial	VQFP44	Tray
TS80C58X2xxx-LIA	-5 to +/-10%	Industrial	PDIL40	Stick
TS80C58X2xxx-LIB	-5 to +/-10%	Industrial	PLCC44	Stick
TS80C58X2xxx-LIC	-5 to +/-10%	Industrial	PQFP44	Tray
TS80C58X2xxx-LIE	-5 to +/-10%	Industrial	VQFP44	Tray
AT80C58X2zzz-3CSUM	-5 to +/-10%	Industrial & Green	PDIL40	Stick
AT80C58X2zzz-SLSUM	-5 to +/-10%	Industrial & Green	PLCC44	Stick
AT80C58X2zzz-RLTUM	-5 to +/-10%	Industrial & Green	VQFP44	Tray
AT80C58X2zzz-3CSUL	-5 to +/-10%	Industrial & Green	PDIL40	Stick
AT80C58X2zzz-SLSUL	-5 to +/-10%	Industrial & Green	PLCC44	Stick
AT80C58X2zzz-RLTUL	-5 to +/-10%	Industrial & Green	VQFP44	Tray
AT80C58X2zzz-3CSUV	-5 to +/-10%	Industrial & Green	PDIL40	Stick
AT80C58X2zzz-SLSUV	-5 to +/-10%	Industrial & Green	PLCC44	Stick
AT80C58X2zzz-RLTUV	-5 to +/-10%	Industrial & Green	VQFP44	Tray
TS87C58X2-MCA	5V ±10%	Commercial	PDIL40	Stick
TS87C58X2-MCB	5V ±10%	Commercial	PLCC44	Stick
TS87C58X2-MCC	5V ±10%	Commercial	PQFP44	Tray

Part Number	Supply Voltage	Temperature Range	Package	Packing
TS87C58X2-MCE	5V ±10%	Commercial	VQFP44	Tray
TS87C58X2-VCA	5V ±10%	Commercial	PDIL40	Stick
TS87C58X2-VCB	5V ±10%	Commercial	PLCC44	Stick
TS87C58X2-VCC	5V ±10%	Commercial	PQFP44	Tray
TS87C58X2-VCE	5V ±10%	Commercial	VQFP44	Tray
TS87C58X2-LCA	2.7 to 5.5V	Commercial	PDIL40	Stick
TS87C58X2-LCB	2.7 to 5.5V	Commercial	PLCC44	Stick
TS87C58X2-LCC	2.7 to 5.5V	Commercial	PQFP44	Tray
TS87C58X2-LCE	2.7 to 5.5V	Commercial	VQFP44	Tray
TS87C58X2-MIA	5V ±10%	Industrial	PDIL40	Stick
TS87C58X2-MIB	5V ±10%	Industrial	PLCC44	Stick
TS87C58X2-MIC	5V ±10%	Industrial	PQFP44	Tray
TS87C58X2-MIE	5V ±10%	Industrial	VQFP44	Tray
TS87C58X2-VIA	5V ±10%	Industrial	PDIL40	Stick
TS87C58X2-VIB	5V ±10%	Industrial	PLCC44	Stick
TS87C58X2-VIC	5V ±10%	Industrial	PQFP44	Tray
TS87C58X2-VIE	5V ±10%	Industrial	VQFP44	Tray
TS87C58X2-LIA	2.7 to 5.5V	Industrial	PDIL40	Stick
TS87C58X2-LIB	2.7 to 5.5V	Industrial	PLCC44	Stick
TS87C58X2-LIC	2.7 to 5.5V	Industrial	PQFP44	Tray
TS87C58X2-LIE	2.7 to 5.5V	Industrial	VQFP44	Tray
AT87C58X2-3CSUM	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUM	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUM	5V ±10%	Industrial & Green	VQFP44	Tray
AT87C58X2-3CSUL	2.7 to 5.5V	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUL	2.7 to 5.5V	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUL	2.7 to 5.5V	Industrial & Green	VQFP44	Tray
AT87C58X2-3CSUV	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUV	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUV	5V ±10%	Industrial & Green	VQFP44	Tray

21. Datasheet Revision History

21.1 Changes from Rev. C 01/01 to Rev. D 11/05

1. Added green product Ordering Information.

21.2 Changes from Rev. D 11/05 to Rev. E 04/06

1. Changed value of AUXR register.

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