



Welcome to E-XFL.COM

#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40/20MHz
Connectivity	UART/USART
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts87c58x2-mib

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



The TS80C54/58X2 has 2 software-selectable modes of reduced activity for further reduction in power consumption. In the idle mode the CPU is frozen while the timers, the serial port and the interrupt system are still operating. In the power-down mode the RAM is saved and all other functions are inoperative.

PDIL40 PLCC44 PQFP44 F1 VQFP44 1.4	ROM (bytes)	EPROM (bytes)
TS80C54X2	16k	0
TS80C58X2	32k	0
TS87C54X2	0	16k
TS87C58X2	0	32k

## 2. Block Diagram



		PIN NU	MBER	TYPE			
MNEMONIC	DIL	LCC	VQFP 1.4	TTPE	Name And Function		
MNEMONIC		PIN NU	MBER	TYPE	NAME AND FUNCTION		
ALE/PROG	30	33	27	O (I)	Address Latch Enable/Program Pulse: Output pulse for latching the low byte of address during an access to external memory. In normal operation, ALE is emitted constant rate of 1/6 (1/3 in X2 mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each acce external data memory. This pin is also the program pulse input (PROG) during EP programming. ALE can be disabled by setting SFR's AUXR.0 bit. With this bit set will be inactive during internal fetches.		
PSEN	29	32	26	0	Program Store ENable: The read strobe to external program memory. When executing code from the external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory. PSEN is not activated during fetches from internal program memory.		
ĒĀ/V <sub>PP</sub>	31	35	29	I	<b>External Access Enable/Programming Supply Voltage:</b> $\overline{EA}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H and 3FFFH (54X2) or 7FFFH (58X2). If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 3FFFH (54X2) or 7FFFH (58X2). This pin also receives the 12.75V programming supply voltage (V <sub>PP</sub> ) during EPROM programming. If security level 1 is programmed, $\overline{EA}$ will be internally latched on Reset.		
XTAL1	19	21	15	I	<b>Crystal 1:</b> Input to the inverting oscillator amplifier and input to the internal clock generator circuits.		
XTAL2	18	20	14	0	Crystal 2: Output from the inverting oscillator amplifier		

### **Table 5-1.**Pin Description for 40/44 pin packages





## 6. TS80C54/58X2 Enhanced Features

In comparison to the original 80C52, the TS80C54/58X2 implements some new features, which are:

- The X2 option.
- The Dual Data Pointer.
- The Watchdog.
- The 4 level interrupt priority system.
- The power-off flag.
- The ONCE mode.
- The ALE disabling.
- Some enhanced features are also located in the UART and the timer 2.

### 6.1 X2 Feature

The TS80C54/58X2 core needs only 6 clock periods per machine cycle. This feature called "X2" provides the following advantages:

- Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power.
- Save power consumption while keeping same CPU power (oscillator power saving).
- Save power consumption by dividing dynamically operating frequency by 2 in operating and idle modes.
- Increase CPU power by 2 while keeping same crystal frequency.

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

### 6.1.1 Description

The clock for the whole circuit and peripheral is first divided by two before being used by the CPU core and peripherals. This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%. Figure 6-2. shows the clock generation block diagram. X2 bit is validated on XTAL1÷2 rising edge to avoid glitches when switching from X2 to STD mode. Figure 6-2. shows the mode switching waveforms.

### Figure 6-1. Clock Generation Diagram



## 8 AT/TS8xC54/8X2



Figure 6-2. Mode Switching Waveforms

The X2 bit in the CKCON register (See Table 6-1.) allows to switch from 12 clock cycles per instruction to 6 clock cycles and vice versa. At reset, the standard speed is activated (STD mode). Setting this bit activates the X2 feature (X2 mode).

### CAUTION

In order to prevent any incorrect operation while operating in X2 mode, user must be aware that all peripherals using clock frequency as time reference (UART, timers) will have their time reference divided by two. For example a free running timer generating an interrupt every 20 ms will then generate an interrupt every 10 ms. UART with 4800 baud rate will have 9600 baud rate.





### **Table 7-1.**AUXR1: Auxiliary Register 1

7	6	5	4	3	2	1	0
-	-	-	-	GF3	0	-	DPS

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
4	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
3	GF3	This bit is a general purpose user flag
2	0	Reserved Always stuck at 0.
1	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
0	DPS	Data Pointer Selection Clear to select DPTR0. Set to select DPTR1.

Reset Value = XXXX 00X0 Not bit addressable

User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new feature. In that case, the reset value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.





### 8.1.1 Programmable Clock-Output

In the clock-out mode, timer 2 operates as a 50%-duty-cycle, programmable clock generator (See Figure 8-2) . The input clock increments TL2 at frequency  $F_{OSC}/2$ . The timer repeatedly counts to overflow from a loaded value. At overflow, the contents of RCAP2H and RCAP2L registers are loaded into TH2 and TL2. In this mode, timer 2 overflows do not generate interrupts. The formula gives the clock-out frequency as a function of the system oscillator frequency and the value in the RCAP2H and RCAP2L registers :

$$Clock - OutFrequency = \frac{F_{osc}}{4 \times (65536 - RCAP2H/RCAP2L)}$$

For a 16 MHz system clock, timer 2 has a programmable frequency range of 61 Hz  $(F_{OSC}/2^{16})$  to 4 MHz  $(F_{OSC}/4)$ . The generated clock signal is brought out to T2 pin (P1.0).

Timer 2 is programmed for the clock-out mode as follows:

- Set T2OE bit in T2MOD register.
- Clear C/T2 bit in T2CON register.
- Determine the 16-bit reload value from the formula and enter it in RCAP2H/RCAP2L registers.







#### Figure 9-3. UART Timings in Modes 2 and 3

### 9.1.1 Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit. To support automatic address recognition, a device is identified by a given address and a broadcast address.

NOTE: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).

#### 9.1.2 Given Address

Each device has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don't-care bits (defined by zeros) to form the device's given address. The don't-care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed.

To address a device by its individual address, the SADEN mask byte must be 1111 1111b. For example:

SADDR	0101 0110b
SADEN	<u>1111 1100b</u>
Given	0101 01XXb

The following is an example of how to use given addresses to address different slaves:

Slave A:	SADDR <u>SADEN</u> Given	1111 0001b <u>1111 1010b</u> 1111 0X0Xb
Slave B:	SADDR <u>SADEN</u> Given	1111 0011b <u>1111 1001b</u> 1111 0XX1b
Slave C:	SADDR <u>SADEN</u> Given	1111 0010b <u>1111 1101b</u> 1111 00X1b

The SADEN byte is selected so that each slave may be addressed separately.

For slave A, bit 0 (the LSB) is a don't-care bit; for slaves B and C, bit 0 is a 1. To communicate with slave A only, the master must send an address where bit 0 is clear (e.g. 1111 0000b). For slave A, bit 1 is a 1; for slaves B and C, bit 1 is a don't care bit. To communicate with slaves B and C, but not slave A, the master must send an address with bits 0 and 1 both set (e.g. 1111

0011b).

To communicate with slaves A, B and C, the master must send an address with bit 0 set, bit 1 clear, and bit 2 clear (e.g. 1111 0001b).

### 9.1.3 Broadcast Address

A broadcast address is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't-care bits, e.g.:

SADDR	0101 0110b	
SADEN	1111 1100b	
Broadcast =SADDR OR SADEN	1111 111Xb	

The use of don't-care bits provides flexibility in defining the broadcast address, however in most applications, a broadcast address is FFh. The following is an example of using broadcast addresses:

Slave A:	SADDR <u>SADEN</u> Broadcast	1111 0001b <u>1111 1010b</u> 1111 1X11b,
Slave B:	SADDR <u>SADEN</u> Broadcast	1111 0011b <u>1111 1001b</u> 1111 1X11B,
Slave C:	SADDR= <u>SADEN</u> Broadcast	1111 0010b <u>1111 1101b</u> 1111 1111b

For slaves A and B, bit 2 is a don't care bit; for slave C, bit 2 is set. To communicate with all of the slaves, the master must send an address FFh. To communicate with slaves A and B, but not slave C, the master can send and address FBh.

### 9.1.4 Reset Addresses

On reset, the SADDR and SADEN registers are initialized to 00h, i.e. the given and broadcast addresses are XXXX XXXb (all don't-care bits). This ensures that the serial port will reply to any address, and so, that it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition.



## AT/TS8xC54/8X2

### Table 9-3.

SCON Register SCON - Serial Control Register (98h)

7	6		5	4	3	2	1	0		
FE/SM0	SM1		SM2	REN	TB8	RB8	TI	RI		
Bit Number	Bit Mnemonic		Description							
7	FE	Fran Clea Set SMC	Framing Error bit (SMOD0=1) Clear to reset the error state, not cleared by a valid stop bit. Set by hardware when an invalid stop bit is detected. SMOD0 must be set to enable access to the FE bit							
	SM0	Seria Refe SMC	al port Mode er to SM1 for s DD0 must be c	bit 0 serial port mod cleared to enab	e selection. le access to the	e SM0 bit				
6	SM1	<b>Seri</b> SMC 0 1 1	ierial port Mode bit 1         SM0       SM1Mode       Description       Baud Rate         0       0       0       Shift RegisterF <sub>XTAL</sub> /12 (/6 in X2 mode)         0       1       1       8-bit UARTVariable         0       2       9-bit UARTF <sub>XTAL</sub> /64 or F <sub>XTAL</sub> /32 (/32, /16 in X2 mode)         1       3       9-bit UARTVariable							
5	SM2	Serial port Mode 2 bit / Multiprocessor Communication Enable bit Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0.								
4	REN	Rece Clea Set 1	eption Enable ar to disable so to enable seri	e bit erial reception. al reception.						
3	TB8	Tran Clea Set	Transmitter Bit 8 / Ninth bit to transmit in modes 2 and 3. Clear to transmit a logic 0 in the 9th bit. Set to transmit a logic 1 in the 9th bit.							
2	RB8	Rece Clea Set I In m	Receiver Bit 8 / Ninth bit received in modes 2 and 3 Cleared by hardware if 9th bit received is a logic 0. Set by hardware if 9th bit received is a logic 1. In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used.							
1	TI	Tran Clea Set I the c	Transmit Interrupt flag         Clear to acknowledge interrupt.         Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other         modes.							
0	RI	Rece Clea Set the c	eive Interrupt ar to acknowle by hardware a other modes.	t flag edge interrupt. at the end of th	e 8th bit time in	mode 0, see F	igure 9-2. and	Figure 9-3. in		

Reset Value = 0000 0000b Bit addressable





If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

	IE - Interrupt Enable Register (A8h)									
7	6	5	4	3	2	1	0			
EA	-	ET2	ES	ET1	EX1	ET0	EX0			
Bit Number	Bit Mnemonic			Descrip	otion					
7	EA	Enable All interru Clear to disable a Set to enable all i If EA=1, each inte own interrupt ena	able All interrupt bit ear to disable all interrupts. at to enable all interrupts. EA=1, each interrupt source is individually enabled or disabled by setting or clearing its n interrupt enable bit.							
6	-	<b>Reserved</b> The value read fr	om this bit is in	determinate. Do	o not set this bi	t.				
5	ET2	Timer 2 overflow i Clear to disable to Set to enable time	imer 2 overflow interrupt Enable bit Clear to disable timer 2 overflow interrupt. Set to enable timer 2 overflow interrupt.							
4	ES	Serial port Enable Clear to disable s Set to enable ser	Serial port Enable bit Clear to disable serial port interrupt. Set to enable serial port interrupt.							
3	ET1	Timer 1 overflow i Clear to disable ti Set to enable time	imer 1 overflow interrupt Enable bit Clear to disable timer 1 overflow interrupt. Set to enable timer 1 overflow interrupt.							
2	EX1	External interrupt Clear to disable e Set to enable ext	xternal interrupt 1 Enable bit Clear to disable external interrupt 1. Set to enable external interrupt 1.							
1	ET0	Timer 0 overflow i Clear to disable ti Set to enable time	imer 0 overflow interrupt Enable bit Clear to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.							
0	EX0	External interrupt Clear to disable e Set to enable ext	0 Enable bit external interrup ernal interrupt (	ot 0. ).						

Table 10-2. IE Register

Reset Value = 0X00 0000b Bit addressable



### Figure 11-1. Power-Down Exit Waveform



Exit from power-down by reset redefines all the SFRs, exit from power-down by external interrupt does no affect the SFRs.

Exit from power-down by either reset or external interrupt does not affect the internal RAM content.

NOTE: If idle mode is activated with power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data*	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data*	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

 Table 11-1.
 The state of ports during idle and power-down modes

\* Port 0 can force a "zero" level A "one" Level will leave port floating.

# AT/TS8xC54/8X2

Table 18-1.	Signature B	ytes Content
-------------	-------------	--------------

	-)	
Location	Contents	Comment
30h	58h	Manufacturer Code: Atmel Wireless & Microcontrollers
31h	57h	Family Code: C51 X2
60h	37h	Product name: TS80C58X2
60h	B7h	Product name: TS87C58X2
60h	3Bh	Product name: TS80C54X2
60h	BBh	Product name: TS87C54X2
61h	FFh	Product revision number



## AT/TS8xC54/8X2

Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
V <sub>OL1</sub>	Output Low Voltage, port 0 <sup>(6)</sup>			0.3 0.45 1.0	V V V	$\begin{split} I_{OL} &= 200 \ \mu A^{(4)} \\ I_{OL} &= 3.2 \ m A^{(4)} \\ I_{OL} &= 7.0 \ m A^{(4)} \end{split}$
V <sub>OL2</sub>	Output Low Voltage, ALE, PSEN			0.3 0.45 1.0	V V V	$\begin{split} I_{OL} &= 100 \; \mu A^{(4)} \\ I_{OL} &= 1.6 \; m A^{(4)} \\ I_{OL} &= 3.5 \; m A^{(4)} \end{split}$
V <sub>OH</sub>	Output High Voltage, ports 1, 2, 3	V <sub>CC</sub> - 0.3 V <sub>CC</sub> - 0.7 V <sub>CC</sub> - 1.5			> > >	I <sub>OH</sub> = -10 μA I <sub>OH</sub> = -30 μA I <sub>OH</sub> = -60 μA V <sub>CC</sub> = 5 V ± 10%
V <sub>OH1</sub>	Output High Voltage, port 0	V <sub>CC</sub> - 0.3 V <sub>CC</sub> - 0.7 V <sub>CC</sub> - 1.5			V V V	$I_{OH} = -200 \ \mu A$ $I_{OH} = -3.2 \ m A$ $I_{OH} = -7.0 \ m A$ $V_{CC} = 5 \ V \pm 10\%$
V <sub>OH2</sub>	Output High Voltage,ALE, PSEN	V <sub>CC</sub> - 0.3 V <sub>CC</sub> - 0.7 V <sub>CC</sub> - 1.5			V V V	$I_{OH} = -100 \ \mu A$ $I_{OH} = -1.6 \ m A$ $I_{OH} = -3.5 \ m A$ $V_{CC} = 5 \ V \pm 10\%$
R <sub>RST</sub>	RST Pulldown Resistor	50	90 (5)	200	kΩ	
IIL	Logical 0 Input Current ports 1, 2 and 3			-50	μΑ	Vin = 0.45 V
I <sub>LI</sub>	Input Leakage Current			±10	μA	0.45 V < Vin < $V_{CC}$
I <sub>TL</sub>	Logical 1 to 0 Transition Current, ports 1, 2, 3			-650	μA	Vin = 2.0 V
C <sub>IO</sub>	Capacitance of I/O Buffer			10	pF	Fc = 1 MHz T <sub>A</sub> = 25°C
I <sub>PD</sub>	Power Down Current		20 (5)	50	μΑ	$2.0 \text{ V} < \text{V}_{\text{CC}} < 5.5 \text{ V}^{(3)}$
I <sub>CC</sub> under RESET	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			1 + 0.4 Freq (MHz) @12MHz 5.8 @16MHz 7.4	mA	$V_{CC} = 5.5 V^{(1)}$
I <sub>cc</sub> operating	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			3 + 0.6 Freq (MHz) @12MHz 10.2 @16MHz 12.6	mA	V <sub>CC</sub> = 5.5 V <sup>(8)</sup>
l <sub>cc</sub> idle	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			0.25+0.3 Freq (MHz) @12MHz 3.9 @16MHz 5.1	mA	$V_{\rm CC} = 5.5 \ V^{(2)}$



### 19.5 AC Parameters

### 19.5.1 Explanation of the AC Symbols

Each timing symbol has 5 characters. The first character is always a "T" (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example:  $T_{AVLL}$  = Time for Address Valid to ALE Low.  $T_{ILPL}$  = Time for ALE Low to PSEN Low.

TA = 0 to +70°C (commercial temperature range);  $V_{SS} = 0 \text{ V}$ ;  $V_{CC} = 5 \text{ V} \pm 10\%$ ; -M and -V ranges. TA = -40°C to +85°C (industrial temperature range);  $V_{SS} = 0 \text{ V}$ ;  $V_{CC} = 5 \text{ V} \pm 10\%$ ; -M and -V ranges.

TA = 0 to +70°C (commercial temperature range);  $V_{SS} = 0$  V; 2.7 V <  $V_{CC}$  < 5.5 V; -L range. TA = -40°C to +85°C (industrial temperature range);  $V_{SS} = 0$  V; 2.7 V <  $V_{CC}$  < 5.5 V; -L range.

Table 19-3. gives the maximum applicable load capacitance for Port 0, Port 1, 2 and 3, and ALE and  $\overrightarrow{\text{PSEN}}$  signals. Timings will be guaranteed if these capacitances are respected. Higher capacitance values can be used, but timings will then be degraded.

	-М	-V	-L
Port 0	100	50	100
Port 1, 2, 3	80	50	80
ALE / PSEN	100	30	100

Table 19-3. Load Capacitance versus speed range, in pF

Table 19-5., Table 19-8. and Table 19-11. give the description of each AC symbols.

Table 19-6., Table 19-9. and Table 19-12. give for each range the AC parameter.

Table 19-7., Table 19-10. and Table 19-13. give the frequency derating formula of the AC parameter. To calculate each AC symbols, take the x value corresponding to the speed grade you need (-M, -V or -L) and replace this value in the formula. Values of the frequency must be limited to the corresponding speed grade:

 Table 19-4.
 Max frequency for derating formula regarding the speed grade

	-M X1 mode	-M X2 mode	-V X1 mode	-V X2 mode	-L X1 mode	-L X2 mode
Freq (MHz)	40	20	40	30	30	20
T (ns)	25	50	25	33.3	33.3	50

Example:

 $T_{111V}$  in X2 mode for a -V part at 20 MHz (T = 1/20^{E6} = 50 ns):

x= 22 (Table 19-7.)

T= 50ns

 $T_{LLIV} = 2T - x = 2 \times 50 - 22 = 78$ ns





### 19.5.6 External Data Memory Read Cycle





### 19.5.7 Serial Port Timing - Shift Register Mode Table 19-11. Symbol Description

Symbol	Parameter
T <sub>XLXL</sub>	Serial port clock cycle time
T <sub>QVHX</sub>	Output data set-up to clock rising edge
T <sub>XHQX</sub>	Output data hold after clock rising edge
T <sub>XHDX</sub>	Input data hold after clock rising edge
T <sub>XHDV</sub>	Clock rising edge to input data valid

Table 19-12. AC Parameters for a Fix Clock

Speed	-I 40 I	M MHz	- X2 n 30 l 60 MHz	V node MHz z equiv.	۔ standard M	V mode 40 Hz	- X2 n 20 I 40 MHz	L node MHz z equiv.	- standar 30 I	L d mode MHz	Units
Symbol	Min	Max	Min	Max	Min	Мах	Min	Max	Min	Max	
T <sub>XLXL</sub>	300		200		300		300		400		ns
T <sub>QVHX</sub>	200		117		200		200		283		ns
T <sub>XHQX</sub>	30		13		30		30		47		ns
T <sub>XHDX</sub>	0		0		0		0		0		ns
T <sub>XHDV</sub>		117		34		117		117		200	ns

Symbol	Туре	Standard Clock	X2 Clock	-М	-V	-L	Units
T <sub>XLXL</sub>	Min	12 T	6 T				ns
T <sub>QVHX</sub>	Min	10 T - x	5 T - x	50	50	50	ns
T <sub>XHQX</sub>	Min	2 T - x	T - x	20	20	20	ns
T <sub>XHDX</sub>	Min	х	х	0	0	0	ns
T <sub>XHDV</sub>	Max	10 T - x	5 T- x	133	133	133	ns

Table 19-13. AC Parameters for a Variable Clock: derating formula

### 19.5.8 Shift Register Timing Waveforms

Figure 19-9. Shift Register Timing Waveforms







### 19.5.9 EPROM Programming and Verification Characteristics

 $T_A$  = 21°C to 27°C;  $V_{SS}$  = 0V;  $V_{CC}$  = 5V  $\pm$  10% while programming.  $V_{CC}$  = operating range while verifying.

Symbol	Parameter	Min	Мах	Units
V <sub>PP</sub>	Programming Supply Voltage	12.5	13	V
I <sub>PP</sub>	Programming Supply Current		75	mA
1/T <sub>CLCL</sub>	Oscillator Frquency	4	6	MHz
T <sub>AVGL</sub>	Address Setup to PROG Low	48 T <sub>CLCL</sub>		
T <sub>GHAX</sub>	Adress Hold after PROG	48 T <sub>CLCL</sub>		
T <sub>DVGL</sub>	Data Setup to PROG Low	48 T <sub>CLCL</sub>		
T <sub>GHDX</sub>	Data Hold after PROG	48 T <sub>CLCL</sub>		
T <sub>EHSH</sub>	(Enable) High to V <sub>PP</sub>	48 T <sub>CLCL</sub>		
T <sub>SHGL</sub>	V <sub>PP</sub> Setup to PROG Low	10		μs
T <sub>GHSL</sub>	V <sub>PP</sub> Hold after PROG	10		μs
T <sub>GLGH</sub>	PROG Width	90	110	μs
T <sub>AVQV</sub>	Address to Valid Data		48 T <sub>CLCL</sub>	
T <sub>ELQV</sub>	ENABLE Low to Data Valid		48 T <sub>CLCL</sub>	
T <sub>EHQZ</sub>	Data Float after ENABLE	0	48 T <sub>CLCL</sub>	

Table 19-14. EPROM Programming Parameters

### 19.5.10 EPROM Programming and Verification Waveforms





\* 8KB: up to P2.4, 16KB: up to P2.5, 32KB: up to P3.4, 64KB: up to P3.5



### 19.5.13 AC Testing Input/Output Waveforms

### Figure 19-12. AC Testing Input/Output Waveforms



AC inputs during testing are driven at V<sub>CC</sub> - 0.5 for a logic "1" and 0.45V for a logic "0". Timing measurement are made at V<sub>IH</sub> min for a logic "1" and V<sub>IL</sub> max for a logic "0".

### 19.5.14 Float Waveforms

### Figure 19-13. Float Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded  $V_{OH}/V_{OL}$  level occurs.  $I_{OL}/I_{OH} \ge \pm 20$ mA.

#### 19.5.15 Clock Waveforms

Valid in normal clock mode. In X2 mode XTAL2 signal must be changed to XTAL2 divided by two.



## 20. Ordering Information

Table 20-1.	
-------------	--

Possible Ordering Entries

Part Number	Supply Voltage	Temperature Range	Package	Packing
TS80C54X2xxx-MCA	-5 to +/-10%	Commercial	PDIL40	Stick
TS80C54X2xxx-MCB	-5 to +/-10%	Commercial	PLCC44	Stick
TS80C54X2xxx-MCC	-5 to +/-10%	Commercial	PQFP44	Tray
TS80C54X2xxx-MCE	-5 to +/-10%	Commercial	VQFP44	Tray
TS80C54X2xxx-VCA	-5 to +/-10%	Commercial	PDIL40	Stick
TS80C54X2xxx-VCB	-5 to +/-10%	Commercial	PLCC44	Stick
TS80C54X2xxx-VCC	-5 to +/-10%	Commercial	PQFP44	Tray
TS80C54X2xxx-VCE	-5 to +/-10%	Commercial	VQFP44	Tray
TS80C54X2xxx-LCA	-5 to +/-10%	Commercial	PDIL40	Stick
TS80C54X2xxx-LCB	-5 to +/-10%	Commercial	PLCC44	Stick
TS80C54X2xxx-LCC	-5 to +/-10%	Commercial	PQFP44	Tray
TS80C54X2xxx-LCE	-5 to +/-10%	Commercial	VQFP44	Tray
TS80C54X2xxx-MIA	-5 to +/-10%	Industrial	PDIL40	Stick
TS80C54X2xxx-MIB	-5 to +/-10%	Industrial	PLCC44	Stick
TS80C54X2xxx-MIC	-5 to +/-10%	Industrial	PQFP44	Tray
TS80C54X2xxx-MIE	-5 to +/-10%	Industrial	VQFP44	Tray
TS80C54X2xxx-VIA	-5 to +/-10%	Industrial	PDIL40	Stick
TS80C54X2xxx-VIB	-5 to +/-10%	Industrial	PLCC44	Stick
TS80C54X2xxx-VIC	-5 to +/-10%	Industrial	PQFP44	Tray
TS80C54X2xxx-VIE	-5 to +/-10%	Industrial	VQFP44	Tray
TS80C54X2xxx-LIA	-5 to +/-10%	Industrial	PDIL40	Stick
TS80C54X2xxx-LIB	-5 to +/-10%	Industrial	PLCC44	Stick
TS80C54X2xxx-LIC	-5 to +/-10%	Industrial	PQFP44	Tray
TS80C54X2xxx-LIE	-5 to +/-10%	Industrial	VQFP44	Tray
		·		
AT80C54X2zzz-3CSUM	-5 to +/-10%	Industrial & Green	PDIL40	Stick
AT80C54X2zzz-SLSUM	-5 to +/-10%	Industrial & Green	PLCC44	Stick
AT80C54X2zzz-RLTUM	-5 to +/-10%	Industrial & Green	VQFP44	Tray
AT80C54X2zzz-3CSUL	-5 to +/-10%	Industrial & Green	PDIL40	Stick
AT80C54X2zzz-SLSUL	-5 to +/-10%	Industrial & Green	PLCC44	Stick
AT80C54X2zzz-RLTUL	-5 to +/-10%	Industrial & Green	VQFP44	Tray
AT80C54X2zzz-3CSUV	-5 to +/-10%	Industrial & Green	PDIL40	Stick
AT80C54X2zzz-SLSUV	-5 to +/-10%	Industrial & Green	PLCC44	Stick
AT80C54X2zzz-RLTUV	-5 to +/-10%	Industrial & Green	VQFP44	Tray
TS87C54X2-MCA	5V ±10%	Commercial	PDIL40	Stick
TS87C54X2-MCB	5V ±10%	Commercial	PLCC44	Stick

# 8 AT/TS8xC54/8X2

# AT/TS8xC54/8X2

Part Number	Supply Voltage	Temperature Range	Package	Packing
TS87C54X2-MCC	5V ±10%	Commercial	PQFP44	Tray
TS87C54X2-MCE	5V ±10%	Commercial	VQFP44	Tray
TS87C54X2-VCA	5V ±10%	Commercial	PDIL40	Stick
TS87C54X2-VCB	5V ±10%	Commercial	PLCC44	Stick
TS87C54X2-VCC	5V ±10%	Commercial	PQFP44	Tray
TS87C54X2-VCE	5V ±10%	Commercial	VQFP44	Tray
TS87C54X2-LCA	2.7 to 5.5V	Commercial	PDIL40	Stick
TS87C54X2-LCB	2.7 to 5.5V	Commercial	PLCC44	Stick
TS87C54X2-LCC	2.7 to 5.5V	Commercial	PQFP44	Tray
TS87C54X2-LCE	2.7 to 5.5V	Commercial	VQFP44	Tray
TS87C54X2-MIA	5V ±10%	Industrial	PDIL40	Stick
TS87C54X2-MIB	5V ±10%	Industrial	PLCC44	Stick
TS87C54X2-MIC	5V ±10%	Industrial	PQFP44	Tray
TS87C54X2-MIE	5V ±10%	Industrial	VQFP44	Tray
TS87C54X2-VIA	5V ±10%	Industrial	PDIL40	Stick
TS87C54X2-VIB	5V ±10%	Industrial	PLCC44	Stick
TS87C54X2-VIC	5V ±10%	Industrial	PQFP44	Tray
TS87C54X2-VIE	5V ±10%	Industrial	VQFP44	Tray
TS87C54X2-LIA	2.7 to 5.5V	Industrial	PDIL40	Stick
TS87C54X2-LIB	2.7 to 5.5V	Industrial	PLCC44	Stick
TS87C54X2-LIC	2.7 to 5.5V	Industrial	PQFP44	Tray
TS87C54X2-LIE	2.7 to 5.5V	Industrial	VQFP44	Tray
AT87C54X2-3CSUM	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C54X2-SLSUM	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C54X2-RLTUM	5V ±10%	Industrial & Green	VQFP44	Tray
AT87C54X2-3CSUL	2.7 to 5.5V	Industrial & Green	PDIL40	Stick
AT87C54X2-SLSUL	2.7 to 5.5V	Industrial & Green	PLCC44	Stick
AT87C54X2-RLTUL	2.7 to 5.5V	Industrial & Green	VQFP44	Tray
AT87C54X2-3CSUV	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C54X2-SLSUV	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C54X2-RLTUV	5V ±10%	Industrial & Green	VQFP44	Tray

