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Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40/20MHz
Connectivity	UART/USART
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-VQFP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts87c58x2-mie

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The TS80C54/58X2 has 2 software-selectable modes of reduced activity for further reduction in power consumption. In the idle mode the CPU is frozen while the timers, the serial port and the interrupt system are still operating. In the power-down mode the RAM is saved and all other functions are inoperative.

PDIL40 PLCC44 PQFP44 F1 VQFP44 1.4	ROM (bytes)	EPROM (bytes)
TS80C54X2	16k	0
TS80C58X2	32k	0
TS87C54X2	0	16k
TS87C58X2	0	32k

2. Block Diagram





Table 4-1.	All SFRs with their address and their reset valu	e
		-

	Bit address- able		Non Bit addressable									
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F				
F8h									FFh			
F0h	B 0000 0000								F7h			
E8h									EFh			
E0h	ACC 0000 0000								E7h			
D8h									DFh			
D0h	PSW 0000 0000								D7h			
C8h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			CFh			
C0h									C7h			
B8h	IP XX00 0000	SADEN 0000 0000							BFh			
B0h	P3 1111 1111							IPH XX00 0000	B7h			
A8h	IE 0X00 0000	SADDR 0000 0000							AFh			
A0h	P2 1111 1111		AUXR1 XXXX 0XX0				WDTRST XXXX XXXX	WDTPRG XXXX X000	A7h			
98h	SCON 0000 0000	SBUF XXXX XXXX							9Fh			
90h	P1 1111 1111								97h			
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XXXX XXX0	CKCON XXXX XXX0	8Fh			
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00X1 0000	87h			
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	<u> </u>			

reserved



Table 7-1.AUXR1: Auxiliary Register 1

7	6	5	4	3	2	1	0
-	-	-	-	GF3	0	-	DPS

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
3	GF3	This bit is a general purpose user flag
2	0	Reserved Always stuck at 0.
1	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
0	DPS	Data Pointer Selection Clear to select DPTR0. Set to select DPTR1.

Reset Value = XXXX 00X0 Not bit addressable

User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new feature. In that case, the reset value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.



8. Timer 2

The timer 2 in the TS80C54/58X2 is compatible with the timer 2 in the 80C52.

It is a 16-bit timer/counter: the count is maintained by two eight-bit timer registers, TH2 and TL2, connected in cascade. It is controlled by T2CON register (See Table 8-1) and T2MOD register (See Table 8-2). Timer 2 operation is similar to Timer 0 and Timer 1. C/T2 selects $F_{OSC}/12$ (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows TL2 to be incremented by the selected input.

Timer 2 has 3 operating modes: capture, autoreload and Baud Rate Generator. These modes are selected by the combination of RCLK, TCLK and CP/RL2 (T2CON), as described in the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description.

Refer to the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description for the description of Capture and Baud Rate Generator Modes.

In TS80C54/58X2 Timer 2 includes the following enhancements:

- Auto-reload mode with up or down counter
- Programmable clock-output

8.1 Auto-Reload Mode

The auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. If DCEN bit in T2MOD is cleared, timer 2 behaves as in 80C52 (refer to the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description). If DCEN bit is set, timer 2 acts as an Up/down timer/counter as shown in Figure 8-1. In this mode the T2EX pin controls the direction of count.

When T2EX is high, timer 2 counts up. Timer overflow occurs at FFFFh which sets the TF2 flag and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L registers to be loaded into the timer registers TH2 and TL2.

When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers TH2 and TL2 equals the value stored in RCAP2H and RCAP2L registers. The underflow sets TF2 flag and reloads FFFFh into the timer registers.

The EXF2 bit toggles when timer 2 overflows or underflows according to the the direction of the count. EXF2 does not generate any interrupt. This bit can be used to provide 17-bit resolution

- **AIMEL**
- Enter a 16-bit initial value in timer registers TH2/TL2. It can be the same as the reload value or a different one depending on the application.
- To start the timer, set TR2 run control bit in T2CON register.

It is possible to use timer 2 as a baud rate generator and a clock generator simultaneously. For this configuration, the baud rates and clock frequencies are not independent since both functions use the values in the RCAP2H and RCAP2L registers.



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Table 9-4. PCON Register

Table 3-J.	FUUN		ioi ivegistei	(0711)				
7	6	5	4	3	2	1	0	
SMOD1	SMOD1 SMOD0		POF	GF1	GF0	PD	IDL	
Bit	Bit							
Number	Mnemonic			Descrip	tion			
7	SMOD1	Serial port Mode Set to select dou	e bit 1 uble baud rate in	n mode 1, 2 or 3	3.			
6	SMOD0	Serial port Mode Clear to select S Set to to select F	Serial port Mode bit 0 Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.					
5	-	Reserved The value read fi	om this bit is in	determinate. Do	o not set this bi	t.		
4	POF	Power-Off Flag Clear to recogniz Set by hardware	e next reset typ when VCC rise	e. s from 0 to its n	ominal voltage	. Can also be s	et by software.	
3	GF1	General purpose Cleared by user Set by user for g	e Flag for general purp eneral purpose	oose usage. usage.				
2	GF0	General purpose Cleared by user Set by user for g	ieneral purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.					
1	PD	Power-Down mo Cleared by hardw Set to enter powe	ower-Down mode bit leared by hardware when reset occurs. iet to enter power-down mode.					
0	IDL	Idle mode bit Clear by hardwar Set to enter idle	re when interrup mode.	ot or reset occu	rS.			

Table 9-5. PCON - Power Control Register (87h)

Reset Value = 00X1 0000b Not bit addressable

Power-off flag reset value will be 1 only after a power on (cold reset). A warm reset doesn't affect the value of this bit.

11. Idle mode

An instruction that sets PCON.0 causes that to be the last instruction executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer, and Serial Port functions. The CPU status is preserved in its entirely : the Stack Pointer, Program Counter, Program Status Word, Accumulator and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels.

There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bits GF0 and GF1 can be used to give an indication if an interrupt occured during normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

11.1 Power-Down Mode

To save maximum power, a power-down mode can be invoked by software (Refer to Table 9-4., PCON register).

In power-down mode, the oscillator is stopped and the instruction that invoked power-down mode is the last instruction executed. The internal RAM and SFRs retain their value until the power-down mode is terminated. V_{CC} can be lowered to save further power. Either a hardware reset or an external interrupt can cause an exit from power-down. To properly terminate power-down, the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.

Only external interrupts INT0 and INT1 are useful to exit from power-down. For that, interrupt must be enabled and configured as level or edge sensitive interrupt input.

Holding the pin low restarts the oscillator but bringing the pin high completes the exit as detailed in Figure 11-1. When both interrupts are enabled, the oscillator restarts as soon as one of the two inputs is held low and power down exit will be completed when the first input will be released. In this case the higher priority interrupt service routine is executed.

Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put TS80C54/58X2 into power-down mode.





Figure 11-1. Power-Down Exit Waveform



Exit from power-down by reset redefines all the SFRs, exit from power-down by external interrupt does no affect the SFRs.

Exit from power-down by either reset or external interrupt does not affect the internal RAM content.

NOTE: If idle mode is activated with power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data*	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data*	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

 Table 11-1.
 The state of ports during idle and power-down modes

* Port 0 can force a "zero" level A "one" Level will leave port floating.

13. ONCE[™] Mode (ON Chip Emulation)

The ONCE mode facilitates testing and debugging of systems using TS80C54/58X2 without removing the circuit from the board. The ONCE mode is invoked by driving certain pins of the TS80C54/58X2; the following sequence must be exercised:

- Pull ALE low while the device is in reset (RST high) and PSEN is high.
- Hold ALE low as RST is deactivated.

While the TS80C54/58X2 is in ONCE mode, an emulator or test CPU can be used to drive the circuit Table 13-1 shows the status of the port pins during ONCE mode.

Normal operation is restored when normal reset is applied.

Table 13-1. External Pin Status during ONCE Mode

ALE PSEN		Port 0	Port 1	Port 2	Port 3	XTAL1/2
Weak pull-up	Weak pull-up	Float	Weak pull-up	Weak pull-up	Weak pull-up	Active



17. TS87C54/58X2 EPROM

17.1 EPROM Structure

The TS87C54/58X2 EPROM is divided in two different arrays:

- the code array:16/32 Kbytes.
- the encryption array:64 bytes.
- In addition a third non programmable array is implemented:
- the signature array: 4 bytes.

17.2 EPROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

17.2.1 Encryption Array

Within the EPROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

17.2.2 Program Lock Bits

The three lock bits, when programmed according to Table 17-1., will provide different level of protection for the on-chip code and data.

F	Program Lo	ock Bits		
Security level	LB1	LB2	LB3	Protection Description
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data.
2	Р	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, \overline{EA} is sampled and latched on reset, and further programming of the EPROM is disabled.
3	U	Р	U	Same as 2, also verify is disabled.
4	U	U	Р	Same as 3, also external execution is disabled.

Table 17-1.Program Lock bits

U: unprogrammed,

P: programmed

WARNING: Security level 2 and 3 should only be programmed after EPROM and Core verification.







* See Table 31. for proper value on these inputs

17.3.3 Programming Algorithm

The Improved Quick Pulse algorithm is based on the Quick Pulse algorithm and decreases the number of pulses applied during byte programming from 25 to 1.

To program the TS80C54/58X2 the following sequence must be exercised:

- Step 1: Activate the combination of control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Input the appropriate data on the data lines.
- Step 4: Raise EA/VPP from VCC to VPP (typical 12.75V).
- Step 5: Pulse ALE/PROG once.
- Step 6: Lower EA/VPP from VPP to VCC

Repeat step 2 through 6 changing the address and data for the entire array or until the end of the object file is reached (See Figure 17-2.).

17.3.4 Verify algorithm

Code array verify must be done after each byte or block of bytes is programmed. In either case, a complete verify of the programmed array will ensure reliable programming of the TS87C54/58X2.

P 2.7 is used to enable data output.

To verify the TS87C54/58X2 code the following sequence must be exercised:

- Step 1: Activate the combination of program and control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Read data on the data lines.

Repeat step 2 through 3 changing the address for the entire array verification (See Figure 17-2.)





The encryption array cannot be directly verified. Verification of the encryption array is done by observing that the code array is well encrypted.





17.4 EPROM Erasure (Windowed Packages Only)

Erasing the EPROM erases the code array, the encryption array and the lock bits returning the parts to full functionality.

Erasure leaves all the EPROM cells in a 1's state (FF).

17.4.1 Erasure Characteristics

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Å) to an integrated dose at least 15 W-sec/cm². Exposing the EPROM to an ultraviolet lamp of 12,000 μ W/cm² rating for 30 minutes, at a distance of about 25 mm, should be sufficient. An exposure of 1 hour is recommended with most of standard erasers.

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Å. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

18. Signature Bytes

The TS87C54/58X2 has four signature bytes in location 30h, 31h, 60h and 61h. To read these bytes follow the procedure for EPROM verify but activate the control lines provided in Table 31. for Read Signature Bytes. Table 18-1. shows the content of the signature byte for the TS80C54/58X2.

AT/TS8xC54/8X2

Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
V _{OL1}	Output Low Voltage, port 0 ⁽⁶⁾			0.3 0.45 1.0	V V V	$\begin{split} I_{OL} &= 200 \ \mu A^{(4)} \\ I_{OL} &= 3.2 \ m A^{(4)} \\ I_{OL} &= 7.0 \ m A^{(4)} \end{split}$
V _{OL2}	Output Low Voltage, ALE, PSEN			0.3 0.45 1.0	V V V	$\begin{split} I_{OL} &= 100 \; \mu A^{(4)} \\ I_{OL} &= 1.6 \; m A^{(4)} \\ I_{OL} &= 3.5 \; m A^{(4)} \end{split}$
V _{OH}	Output High Voltage, ports 1, 2, 3	V _{CC} - 0.3 V _{CC} - 0.7 V _{CC} - 1.5			> > >	I _{OH} = -10 μA I _{OH} = -30 μA I _{OH} = -60 μA V _{CC} = 5 V ± 10%
V _{OH1}	Output High Voltage, port 0	V _{CC} - 0.3 V _{CC} - 0.7 V _{CC} - 1.5			V V V	$I_{OH} = -200 \ \mu A$ $I_{OH} = -3.2 \ m A$ $I_{OH} = -7.0 \ m A$ $V_{CC} = 5 \ V \pm 10\%$
V _{OH2}	Output High Voltage,ALE, PSEN	V _{CC} - 0.3 V _{CC} - 0.7 V _{CC} - 1.5			V V V	$I_{OH} = -100 \ \mu A$ $I_{OH} = -1.6 \ m A$ $I_{OH} = -3.5 \ m A$ $V_{CC} = 5 \ V \pm 10\%$
R _{RST}	RST Pulldown Resistor	50	90 (5)	200	kΩ	
IIL	Logical 0 Input Current ports 1, 2 and 3			-50	μA	Vin = 0.45 V
I _{LI}	Input Leakage Current			±10	μA	0.45 V < Vin < V_{CC}
I _{TL}	Logical 1 to 0 Transition Current, ports 1, 2, 3			-650	μA	Vin = 2.0 V
C _{IO}	Capacitance of I/O Buffer			10	pF	Fc = 1 MHz T _A = 25°C
I _{PD}	Power Down Current		20 (5)	50	μΑ	$2.0 \text{ V} < \text{V}_{\text{CC}} < 5.5 \text{ V}^{(3)}$
I _{CC} under RESET	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			1 + 0.4 Freq (MHz) @12MHz 5.8 @16MHz 7.4	mA	$V_{CC} = 5.5 V^{(1)}$
I _{cc} operating	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			3 + 0.6 Freq (MHz) @12MHz 10.2 @16MHz 12.6	mA	V _{CC} = 5.5 V ⁽⁸⁾
l _{cc} idle	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			0.25+0.3 Freq (MHz) @12MHz 3.9 @16MHz 5.1	mA	$V_{\rm CC} = 5.5 \ V^{(2)}$



- 5. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
- Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows: Maximum I_{OL} per port pin: 10 mA Maximum I_{OL} per 8-bit port: Port 0: 26 mA Ports 1, 2 and 3: 15 mA Maximum total I_{OL} for all output pins: 71 mA If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- 7. For other values, please contact your sales office.
- Operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH}, T_{CHCL} = 5 ns (see Figure 19-5.), V_{IL} = V_{SS} + 0.5 V,

 $V_{IH} = V_{CC} - 0.5V$; XTAL2 N.C.; $\overline{EA} = Port 0 = V_{CC}$; RST = V_{SS} . The internal ROM runs the code 80 FE (label: SJMP label). I_{CC} would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.





All other pins are disconnected.





All other pins are disconnected.



Symbol	Туре	Standard Clock	X2 Clock	-М	-V	-L	Units
T _{LHLL}	Min	2 T - x	T - x	10	8	15	ns
T _{AVLL}	Min	T - x	0.5 T - x	15	13	20	ns
T _{LLAX}	Min	T - x	0.5 T - x	15	13	20	ns
T _{LLIV}	Max	4 T - x	2 T - x	30	22	35	ns
T _{LLPL}	Min	T - x	0.5 T - x	10	8	15	ns
T _{PLPH}	Min	3 T - x	1.5 T - x	20	15	25	ns
T _{PLIV}	Max	3 T - x	1.5 T - x	40	25	45	ns
T _{PXIX}	Min	x	х	0	0	0	ns
T _{PXIZ}	Max	T - x	0.5 T - x	7	5	15	ns
T _{AVIV}	Max	5 T - x	2.5 T - x	40	30	45	ns
T _{PLAZ}	Max	х	х	10	10	10	ns

Table 19-7. AC Parameters for a Variable Clock: derating formula

19.5.3 External Program Memory Read Cycle









19.5.4 External Data Memory Characteristics

 Table 19-8.
 Symbol Description

Symbol	Parameter
T _{RLRH}	RD Pulse Width
T _{WLWH}	WR Pulse Width
T _{RLDV}	RD to Valid Data In
T _{RHDX}	Data Hold After RD
T _{RHDZ}	Data Float After RD
T_{LLDV}	ALE to Valid Data In
T _{AVDV}	Address to Valid Data In
T _{LLWL}	ALE to WR or RD
T _{AVWL}	Address to WR or RD
T _{QVWX}	Data Valid to WR Transition
T _{QVWH}	Data set-up to WR High
T _{WHQX}	Data Hold After WR
T _{RLAZ}	RD Low to Address Float
T _{WHLH}	RD or WR High to ALE high

Table 19-9. AC Parameters for a Fix Clock

Speed	-	M MH7	- X2 n 30 l 60 MH:	V node MHz z equiv	۔ standard M	V mode 40 Hz	- X2 n 20 I 40 MH:	L node MHz z equiv	۔ standar 30 ا	L d mode MHz	Units
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
T _{RLRH}	130		85		135		125		175		ns
T _{WLWH}	130		85		135		125		175		ns
T _{RLDV}		100		60		102		95		137	ns
T _{RHDX}	0		0		0		0		0		ns
T _{RHDZ}		30		18		35		25		42	ns
T _{LLDV}		160		98		165		155		222	ns
T _{AVDV}		165		100		175		160		235	ns
T _{LLWL}	50	100	30	70	55	95	45	105	70	130	ns
T _{AVWL}	75		47		80		70		103		ns
T _{QVWX}	10		7		15		5		13		ns
T _{QVWH}	160		107		165		155		213		ns
T _{WHQX}	15		9		17		10		18		ns
T _{RLAZ}		0		0		0		0		0	ns
T _{WHLH}	10	40	7	27	15	35	5	45	13	53	ns

19.5.11 External Clock Drive Characteristics (XTAL1)

Table 19-15.AC Parameters

Symbol	Parameter	Min	Мах	Units
T _{CLCL}	Oscillator Period	25		ns
T _{CHCX}	High Time	5		ns
T _{CLCX}	Low Time	5		ns
T _{CLCH}	Rise Time		5	ns
T _{CHCL}	Fall Time		5	ns
T _{CHCX} /T _{CLCX}	Cyclic ratio in X2 mode	40	60	%

19.5.12 External Clock Drive Waveforms

Figure 19-11. External Clock Drive Waveforms







19.5.13 AC Testing Input/Output Waveforms

Figure 19-12. AC Testing Input/Output Waveforms



AC inputs during testing are driven at V_{CC} - 0.5 for a logic "1" and 0.45V for a logic "0". Timing measurement are made at V_{IH} min for a logic "1" and V_{IL} max for a logic "0".

19.5.14 Float Waveforms

Figure 19-13. Float Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \ge \pm 20$ mA.

19.5.15 Clock Waveforms

Valid in normal clock mode. In X2 mode XTAL2 signal must be changed to XTAL2 divided by two.

AT/TS8xC54/8X2

Part Number	Supply Voltage	Temperature Range	Package	Packing
TS87C54X2-MCC	5V ±10%	Commercial	PQFP44	Tray
TS87C54X2-MCE	5V ±10%	Commercial	VQFP44	Tray
TS87C54X2-VCA	5V ±10%	Commercial	PDIL40	Stick
TS87C54X2-VCB	5V ±10%	Commercial	PLCC44	Stick
TS87C54X2-VCC	5V ±10%	Commercial	PQFP44	Tray
TS87C54X2-VCE	5V ±10%	Commercial	VQFP44	Tray
TS87C54X2-LCA	2.7 to 5.5V	Commercial	PDIL40	Stick
TS87C54X2-LCB	2.7 to 5.5V	Commercial	PLCC44	Stick
TS87C54X2-LCC	2.7 to 5.5V	Commercial	PQFP44	Tray
TS87C54X2-LCE	2.7 to 5.5V	Commercial	VQFP44	Tray
TS87C54X2-MIA	5V ±10%	Industrial	PDIL40	Stick
TS87C54X2-MIB	5V ±10%	Industrial	PLCC44	Stick
TS87C54X2-MIC	5V ±10%	Industrial	PQFP44	Tray
TS87C54X2-MIE	5V ±10%	Industrial	VQFP44	Tray
TS87C54X2-VIA	5V ±10%	Industrial	PDIL40	Stick
TS87C54X2-VIB	5V ±10%	Industrial	PLCC44	Stick
TS87C54X2-VIC	5V ±10%	Industrial	PQFP44	Tray
TS87C54X2-VIE	5V ±10%	Industrial	VQFP44	Tray
TS87C54X2-LIA	2.7 to 5.5V	Industrial	PDIL40	Stick
TS87C54X2-LIB	2.7 to 5.5V	Industrial	PLCC44	Stick
TS87C54X2-LIC	2.7 to 5.5V	Industrial	PQFP44	Tray
TS87C54X2-LIE	2.7 to 5.5V	Industrial	VQFP44	Tray
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AT87C54X2-3CSUM	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C54X2-SLSUM	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C54X2-RLTUM	5V ±10%	Industrial & Green	VQFP44	Tray
AT87C54X2-3CSUL	2.7 to 5.5V	Industrial & Green	PDIL40	Stick
AT87C54X2-SLSUL	2.7 to 5.5V	Industrial & Green	PLCC44	Stick
AT87C54X2-RLTUL	2.7 to 5.5V	Industrial & Green	VQFP44	Tray
AT87C54X2-3CSUV	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C54X2-SLSUV	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C54X2-RLTUV	5V ±10%	Industrial & Green	VQFP44	Tray



AT/TS8xC54/8X2

Part Number	Supply Voltage	Temperature Range	Package	Packing
TS87C58X2-MCE	5V ±10%	Commercial	VQFP44	Tray
TS87C58X2-VCA	5V ±10%	Commercial	PDIL40	Stick
TS87C58X2-VCB	5V ±10%	Commercial	PLCC44	Stick
TS87C58X2-VCC	5V ±10%	Commercial	PQFP44	Tray
TS87C58X2-VCE	5V ±10%	Commercial	VQFP44	Tray
TS87C58X2-LCA	2.7 to 5.5V	Commercial	PDIL40	Stick
TS87C58X2-LCB	2.7 to 5.5V	Commercial	PLCC44	Stick
TS87C58X2-LCC	2.7 to 5.5V	Commercial	PQFP44	Tray
TS87C58X2-LCE	2.7 to 5.5V	Commercial	VQFP44	Tray
TS87C58X2-MIA	5V ±10%	Industrial	PDIL40	Stick
TS87C58X2-MIB	5V ±10%	Industrial	PLCC44	Stick
TS87C58X2-MIC	5V ±10%	Industrial	PQFP44	Tray
TS87C58X2-MIE	5V ±10%	Industrial	VQFP44	Tray
TS87C58X2-VIA	5V ±10%	Industrial	PDIL40	Stick
TS87C58X2-VIB	5V ±10%	Industrial	PLCC44	Stick
TS87C58X2-VIC	5V ±10%	Industrial	PQFP44	Tray
TS87C58X2-VIE	5V ±10%	Industrial	VQFP44	Tray
TS87C58X2-LIA	2.7 to 5.5V	Industrial	PDIL40	Stick
TS87C58X2-LIB	2.7 to 5.5V	Industrial	PLCC44	Stick
TS87C58X2-LIC	2.7 to 5.5V	Industrial	PQFP44	Tray
TS87C58X2-LIE	2.7 to 5.5V	Industrial	VQFP44	Tray
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AT87C58X2-3CSUM	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUM	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUM	5V ±10%	Industrial & Green	VQFP44	Tray
AT87C58X2-3CSUL	2.7 to 5.5V	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUL	2.7 to 5.5V	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUL	2.7 to 5.5V	Industrial & Green	VQFP44	Tray
AT87C58X2-3CSUV	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUV	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUV	5V ±10%	Industrial & Green	VQFP44	Tray

21. Datasheet Revision History

21.1 Changes from Rev. C 01/01 to Rev. D 11/05

1. Added green product Ordering Information.

21.2 Changes from Rev. D 11/05 to Rev. E 04/06

1. Changed value of AUXR register.

