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Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40/30MHz
Connectivity	UART/USART
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts87c58x2-vcb

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The TS80C54/58X2 has 2 software-selectable modes of reduced activity for further reduction in power consumption. In the idle mode the CPU is frozen while the timers, the serial port and the interrupt system are still operating. In the power-down mode the RAM is saved and all other functions are inoperative.

PDIL40 PLCC44 PQFP44 F1 VQFP44 1.4	ROM (bytes)	EPROM (bytes)
TS80C54X2	16k	0
TS80C58X2	32k	0
TS87C54X2	0	16k
TS87C58X2	0	32k

2. Block Diagram



4. SFR Mapping

The Special Function Registers (SFRs) of the TS80C54/58X2 fall into the following categories:

- C51 core registers: ACC, B, DPH, DPL, PSW, SP, AUXR1
- I/O port registers: P0, P1, P2, P3
- Timer registers: T2CON, T2MOD, TCON, TH0, TH1, TH2, TMOD, TL0, TL1, TL2, RCAP2L, RCAP2H
- Serial I/O port registers: SADDR, SADEN, SBUF, SCON
- Power and clock control registers: PCON
- HDW Watchdog Timer Reset: WDTRST, WDTPRG
- Interrupt system registers: IE, IP, IPH
- Others: AUXR, CKCON





Table 4-1.	All SFRs with their address and their reset valu	e
		-

	Bit address- able		Non Bit addressable								
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F			
F8h									FFh		
F0h	B 0000 0000								F7h		
E8h									EFh		
E0h	ACC 0000 0000								E7h		
D8h									DFh		
D0h	PSW 0000 0000								D7h		
C8h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			CFh		
C0h									C7h		
B8h	IP XX00 0000	SADEN 0000 0000							BFh		
B0h	P3 1111 1111							IPH XX00 0000	B7h		
A8h	IE 0X00 0000	SADDR 0000 0000							AFh		
A0h	P2 1111 1111		AUXR1 XXXX 0XX0				WDTRST XXXX XXXX	WDTPRG XXXX X000	A7h		
98h	SCON 0000 0000	SBUF XXXX XXXX							9Fh		
90h	P1 1111 1111								97h		
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XXXX XXX0	CKCON XXXX XXX0	8Fh		
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00X1 0000	87h		
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	<u> </u>		

reserved



Table 5-1. Pin Description for 40/44 pin packages

		PIN NU	MBER	TYPE		
MNEMONIC	DIL	LCC	VQFP 1.4	ITPE	Name And Function	
V _{SS}	20	22	16	I	Ground: 0V reference	
Vss1		1	39	I	Optional Ground: Contact the Sales Office for ground connection.	
V _{cc}	40	44	38	I	Power Supply: This is the power supply voltage for normal, idle and power-down operation	
P0.0-P0.7	39-32	43-36	37-30	I/O	Port 0: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to	
					them float and can be used as high impedance inputs. Port 0 pins must be polarized to Vcc or Vss in order to prevent any parasitic current consumption. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-up when emitting 1s. Port 0 also inputs the code bytes during EPROM programming. External pull-ups are required during program verification during which P0 outputs the code bytes.	
P1.0-P1.7	1-8	2-9	40-44 1-3	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current becaus of the internal pull-ups. Port 1 also receives the low-order address byte during memor programming and verification. Alternate functions for Port 1 include:	
	1	2	40	I/O	T2 (P1.0): Timer/Counter 2 external count input/Clockout	
	2	3	41	I	T2EX (P1.1): Timer/Counter 2 Reload/Capture/Direction Control	
P2.0-P2.7	21-28	24-31	18-25	I/O	Port 2 : Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as	
					Inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16- bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ Ri), port 2 emits the contents of the P2 SFR. Some Port 2 pins receive the high order address bits during EPROM programming and verification: P2.0 to P2.5 for A8 to A13	
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Some Port 3 pin P3.4 receive the high order address bits during EPROM programming and verification for TS8xC58X2 devices.	
	10	11	5	1	RXD (P3 0): Serial input port	
	11	13	7	0	TXD (P3.1): Serial output port	
	12	14	8		INTO (P3.2): External interrupt 0	
	13	15	9		INT1 (P3.3): External interrupt 1	
	14	16	10	1	T0 (P3.4): Timer 0 external input	
	15	17	11	I	T1 (P3.5): Timer 1 external input	
	16	18	12	0	WR (P3.6): External data memory write strobe	
	17	19	13	0	RD (P3.7): External data memory read strobe P3.4 also receives A14 during TS87C58X2 EPROM Programming.	
Reset	9	10	4	I	Reset: A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC} .	



Figure 6-2. Mode Switching Waveforms

The X2 bit in the CKCON register (See Table 6-1.) allows to switch from 12 clock cycles per instruction to 6 clock cycles and vice versa. At reset, the standard speed is activated (STD mode). Setting this bit activates the X2 feature (X2 mode).

CAUTION

In order to prevent any incorrect operation while operating in X2 mode, user must be aware that all peripherals using clock frequency as time reference (UART, timers) will have their time reference divided by two. For example a free running timer generating an interrupt every 20 ms will then generate an interrupt every 10 ms. UART with 4800 baud rate will have 9600 baud rate.





Table 7-1.AUXR1: Auxiliary Register 1

7	6	5	4	3	2	1	0
-	-	-	-	GF3	0	-	DPS

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
3	GF3	This bit is a general purpose user flag
2	0	Reserved Always stuck at 0.
1	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
0	DPS	Data Pointer Selection Clear to select DPTR0. Set to select DPTR1.

Reset Value = XXXX 00X0 Not bit addressable

User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new feature. In that case, the reset value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

7.1 Application

Software can take advantage of the additional data pointers to both increase speed and reduce code size, for example, block operations (copy, compare, search ...) are well served by using one data pointer as a 'source' pointer and the other one as a "destination" pointer.

ASSEMBLY LANGUAGE

; Block move using ; Destroys DPTR0 ; note: DPS exits o	g dual data), DPTR1, A opposite of	pointers A and PSW entry state	
; unless an extra l	NC AUXR1	is added	
;			
00A2	AUXR	1 EQU 0A2H	
;			
0000 909000	MOV	DPTR,#SOURCE	; address of SOURCE
0003 05A2	INC	AUXR1	; switch data pointers
0005 90A000	MOV	DPTR,#DEST	; address of DEST
0008	LOOP		
0008 05A2	INC	AUXR1	; switch data pointers
000A E0	MOVX	A, @DPTR	; get a byte from SOURCE
000B A3	INC	DPTR	; increment SOURCE address
000C 05A2	INC	AUXR1	; switch data pointers
000E F0	MOVX	@DPTR,A	; write the byte to DEST
000F A3	INC	DPTR	; increment DEST address
0010 70F6	JNZ	LOOP	; check for 0 terminator
0012 05A2	INC	AUXR1	; (optional) restore DPS

INC is a short (2 bytes) and fast (12 clocks) way to manipulate the DPS bit in the AUXR1 SFR. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry. Observe that without the last instruction (INC AUXR1), the routine will exit with DPS in the opposite state.





8. Timer 2

The timer 2 in the TS80C54/58X2 is compatible with the timer 2 in the 80C52.

It is a 16-bit timer/counter: the count is maintained by two eight-bit timer registers, TH2 and TL2, connected in cascade. It is controlled by T2CON register (See Table 8-1) and T2MOD register (See Table 8-2). Timer 2 operation is similar to Timer 0 and Timer 1. C/T2 selects $F_{OSC}/12$ (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows TL2 to be incremented by the selected input.

Timer 2 has 3 operating modes: capture, autoreload and Baud Rate Generator. These modes are selected by the combination of RCLK, TCLK and CP/RL2 (T2CON), as described in the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description.

Refer to the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description for the description of Capture and Baud Rate Generator Modes.

In TS80C54/58X2 Timer 2 includes the following enhancements:

- Auto-reload mode with up or down counter
- Programmable clock-output

8.1 Auto-Reload Mode

The auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. If DCEN bit in T2MOD is cleared, timer 2 behaves as in 80C52 (refer to the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description). If DCEN bit is set, timer 2 acts as an Up/down timer/counter as shown in Figure 8-1. In this mode the T2EX pin controls the direction of count.

When T2EX is high, timer 2 counts up. Timer overflow occurs at FFFFh which sets the TF2 flag and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L registers to be loaded into the timer registers TH2 and TL2.

When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers TH2 and TL2 equals the value stored in RCAP2H and RCAP2L registers. The underflow sets TF2 flag and reloads FFFFh into the timer registers.

The EXF2 bit toggles when timer 2 overflows or underflows according to the the direction of the count. EXF2 does not generate any interrupt. This bit can be used to provide 17-bit resolution





8.1.1 Programmable Clock-Output

In the clock-out mode, timer 2 operates as a 50%-duty-cycle, programmable clock generator (See Figure 8-2) . The input clock increments TL2 at frequency $F_{OSC}/2$. The timer repeatedly counts to overflow from a loaded value. At overflow, the contents of RCAP2H and RCAP2L registers are loaded into TH2 and TL2. In this mode, timer 2 overflows do not generate interrupts. The formula gives the clock-out frequency as a function of the system oscillator frequency and the value in the RCAP2H and RCAP2L registers :

$$Clock - OutFrequency = \frac{F_{osc}}{4 \times (65536 - RCAP2H/RCAP2L)}$$

For a 16 MHz system clock, timer 2 has a programmable frequency range of 61 Hz $(F_{OSC}/2^{16})$ to 4 MHz $(F_{OSC}/4)$. The generated clock signal is brought out to T2 pin (P1.0).

Timer 2 is programmed for the clock-out mode as follows:

- Set T2OE bit in T2MOD register.
- Clear C/T2 bit in T2CON register.
- Determine the 16-bit reload value from the formula and enter it in RCAP2H/RCAP2L registers.



9. TS80C54/58X2 Serial I/O Port

The serial I/O port in the TS80C54/58X2 is compatible with the serial I/O port in the 80C52. It provides both synchronous and asynchronous communication modes. It operates as an Universal Asynchronous Receiver and Transmitter (UART) in three full-duplex modes (Modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates

Serial I/O port includes the following enhancements:

- Framing error detection
- Automatic address recognition

9.1 Framing Error Detection

Framing bit error detection is provided for the three asynchronous modes (modes 1, 2 and 3). To enable the framing bit error detection feature, set SMOD0 bit in PCON register (See Figure 9-1).



Figure 9-1. Framing Error Block Diagram

When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two CPUs. If a valid stop bit is not found, the Framing Error bit (FE) in SCON register (See Table 9-3.) bit is set.

Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset can clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 9-2. and Figure 9-3.).











Figure 9-3. UART Timings in Modes 2 and 3

9.1.1 Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit. To support automatic address recognition, a device is identified by a given address and a broadcast address.

NOTE: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).

9.1.2 Given Address

Each device has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don't-care bits (defined by zeros) to form the device's given address. The don't-care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed.

To address a device by its individual address, the SADEN mask byte must be 1111 1111b. For example:

SADDR	0101 0110b
SADEN	<u>1111 1100b</u>
Given	0101 01XXb



If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

	IE - Interrupt Enable Register (A8h)									
7	6	5	4	3	2	1	0			
EA	-	ET2	ES	ET1	EX1	ET0	EX0			
Bit Number	Bit Mnemonic			Descrip	otion					
7	EA	Enable All interru Clear to disable a Set to enable all i If EA=1, each inte own interrupt ena	able All interrupt bit ar to disable all interrupts. t to enable all interrupts. A=1, each interrupt source is individually enabled or disabled by setting or clearing its n interrupt enable bit.							
6	-	Reserved The value read fr	om this bit is in	determinate. Do	o not set this bi	t.				
5	ET2	Timer 2 overflow i Clear to disable to Set to enable time	imer 2 overflow interrupt Enable bit Clear to disable timer 2 overflow interrupt. Set to enable timer 2 overflow interrupt.							
4	ES	Serial port Enable Clear to disable s Set to enable ser	e bit erial port interr ial port interrup	upt. t.						
3	ET1	Timer 1 overflow i Clear to disable ti Set to enable time	Fimer 1 overflow interrupt Enable bit Clear to disable timer 1 overflow interrupt. Set to enable timer 1 overflow interrupt.							
2	EX1	External interrupt Clear to disable e Set to enable ext	xternal interrupt 1 Enable bit Zlear to disable external interrupt 1. Set to enable external interrupt 1.							
1	ET0	Timer 0 overflow i Clear to disable ti Set to enable time	imer 0 overflow interrupt Enable bit Clear to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.							
0	EX0	External interrupt Clear to disable e Set to enable ext	0 Enable bit external interrup ernal interrupt (ot 0.).						

Table 10-2. IE Register

Reset Value = 0X00 0000b Bit addressable

Table 10-3.	IP Register
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IP - Interrupt Priority Register (B8h)

7	6		5	4	3	2	1	0		
-	-		PT2	PS	PT1	PX1	PT0	PX0		
Bit Number	Bit Mnemonic		Description							
7	-	Reserve The valu	ed ue read fro	om this bit is in	determinate. Do	o not set this bit				
6	-	Reserve The valu	ed ue read fro	om this bit is in	determinate. Do	o not set this bit				
5	PT2	Timer 2 Refer to	fimer 2 overflow interrupt Priority bit Refer to PT2H for priority level.							
4	PS	Serial portion Refer to	Serial port Priority bit Refer to PSH for priority level.							
3	PT1	Timer 1 Refer to	imer 1 overflow interrupt Priority bit Refer to PT1H for priority level.							
2	PX1	Externa Refer to	xternal interrupt 1 Priority bit lefer to PX1H for priority level.							
1	PT0	Timer 0 Refer to	mer 0 overflow interrupt Priority bit efer to PT0H for priority level.							
0	PX0	Externa Refer to	I interrup PX0H for	t 0 Priority bit priority level.	:					

Reset Value = XX00 0000b Bit addressable





14. Power-Off Flag

The power-off flag allows the user to distinguish between a "cold start" reset and a "warm start" reset.

A cold start reset is the one induced by V_{CC} switch-on. A warm start reset occurs while V_{CC} is still applied to the device and could be generated for example by an exit from power-down.

The power-off flag (POF) is located in PCON register (See Table 14-1.). POF is set by hardware when V_{CC} rises from 0 to its nominal voltage. The POF can be set or cleared by software allowing the user to determine the type of reset.

The POF value is only relevant with a Vcc range from 4.5V to 5.5V. For lower Vcc value, reading POF bit will return indeterminate value.

	6	5	4	3	2	1	0
SMOD1	SMOD) -	POF	GF1	GF0	PD	IDL
Bit Number	Bit Mnemonic	Description					
7	SMOD1	Serial port M Set to select	Serial port Mode bit 1 Set to select double baud rate in mode 1, 2 or 3.				
6	SMOD0	Serial port M Clear to selec Set to to selec	Serial port Mode bit 0 Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.				
5	-	Reserved The value rea	Reserved The value read from this bit is indeterminate. Do not set this bit.				
4	POF	Power-Off Fla Clear to recog Set by hardwa	Power-Off Flag Clear to recognize next reset type. Set by hardware when V _{CC} rises from 0 to its nominal voltage. Can also be set by software.				
3	GF1	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.					
2	GF0	General purp Cleared by us Set by user fo	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.				
1	PD	Power-Down mode bit Cleared by hardware when reset occurs. Set to enter power-down mode.					
0	IDL	Idle mode bit Clear by hardware when interrupt or reset occurs. Set to enter idle mode.					

Table 14-1. PCON Register PCON - Power Control Register (87h)

Reset Value = 00X1 0000b Not bit addressable





* See Table 31. for proper value on these inputs

17.3.3 Programming Algorithm

The Improved Quick Pulse algorithm is based on the Quick Pulse algorithm and decreases the number of pulses applied during byte programming from 25 to 1.

To program the TS80C54/58X2 the following sequence must be exercised:

- Step 1: Activate the combination of control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Input the appropriate data on the data lines.
- Step 4: Raise EA/VPP from VCC to VPP (typical 12.75V).
- Step 5: Pulse ALE/PROG once.
- Step 6: Lower EA/VPP from VPP to VCC

Repeat step 2 through 6 changing the address and data for the entire array or until the end of the object file is reached (See Figure 17-2.).

17.3.4 Verify algorithm

Code array verify must be done after each byte or block of bytes is programmed. In either case, a complete verify of the programmed array will ensure reliable programming of the TS87C54/58X2.

P 2.7 is used to enable data output.

To verify the TS87C54/58X2 code the following sequence must be exercised:

- Step 1: Activate the combination of program and control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Read data on the data lines.

Repeat step 2 through 3 changing the address for the entire array verification (See Figure 17-2.)





19. Electrical Characteristics

19.1 Absolute Maximum Ratings ⁽¹⁾

Ambiant Temperature Under Bias: C = commercial0°C to 70°C I = industrial -40°C to 85°C Storage Temperature-65°C to + 150°C Voltage on V_{CC} to V_{SS}-0.5 V to + 7 V Voltage on V_{PP} to V_{SS}-0.5 V to + 13 V Voltage on Any Pin to V_{SS}-0.5 V to V_{CC} + 0.5 V Power Dissipation1 W⁽²⁾

- 1. Stresses at or above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.
- 2. This value is based on the maximum allowable die temperature and the thermal resistance of the package.

19.2 Power consumption measurement

Since the introduction of the first C51 devices, every manufacturer made operating lcc measurements under reset, which made sense for the designs were the CPU was running under reset. In Atmel new devices, the CPU is no more active during reset, so the power consumption is very low but is not really representative of what will happen in the customer system. That's why, while keeping measurements under Reset, Atmel presents a new way to measure the operating lcc:

Using an internal test ROM, the following code is executed:

Label:

SJMP Label (80 FE)

Ports 1, 2, 3 are disconnected, Port 0 is tied to FFh, EA = Vcc, RST = Vss, XTAL2 is not connected and XTAL1 is driven by the clock.

This is much more representative of the real operating Icc.

19.3 DC Parameters for Standard Voltage

 $\begin{array}{l} T_{A}=0^{\circ}C \ to \ +70^{\circ}C; \ V_{SS}=0 \ V; \ V_{CC}=5 \ V \pm 10\%; \ F=0 \ to \ 40 \ MHz. \\ T_{A}=-40^{\circ}C \ to \ +85^{\circ}C; \ V_{SS}=0 \ V; \ V_{CC}=5 \ V \pm 10\%; \ F=0 \ to \ 40 \ MHz. \end{array}$

Table 19-1.	DC Parameters in Standard Voltage
-------------	-----------------------------------

Symbol	Parameter	Min	Тур	Мах	Unit	Test Conditions
V _{IL}	Input Low Voltage	-0.5		0.2 V _{CC} - 0.1	V	
V _{IH}	Input High Voltage except XTAL1, RST	0.2 V _{CC} + 0.9		V _{CC} + 0.5	V	
V _{IH1}	Input High Voltage, XTAL1, RST	0.7 V _{CC}		V _{CC} + 0.5	V	
				0.3	V	$I_{OL} = 100 \ \mu A^{(4)}$
V _{OL}	Output Low Voltage, ports 1, 2, 3 ⁽⁶⁾			0.45	V	I _{OL} = 1.6 mA ⁽⁴⁾
				1.0	V	I _{OL} = 3.5 mA ⁽⁴⁾

19.5.11 External Clock Drive Characteristics (XTAL1)

Table 19-15.AC Parameters

Symbol	Parameter	Min	Мах	Units
T _{CLCL}	Oscillator Period	25		ns
T _{CHCX}	High Time	5		ns
T _{CLCX}	Low Time	5		ns
T _{CLCH}	Rise Time		5	ns
T _{CHCL}	Fall Time		5	ns
T _{CHCX} /T _{CLCX}	Cyclic ratio in X2 mode	40	60	%

19.5.12 External Clock Drive Waveforms

Figure 19-11. External Clock Drive Waveforms









This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though ($T_A=25^{\circ}C$ fully loaded) RD and WR propagation delays are approximately 50ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.





Part Number	Supply Voltage	Temperature Range	Package	Packing
TS80C58X2xxx-MCA	-5 to +/-10%	Commercial	PDIL40	Stick
TS80C58X2xxx-MCB	-5 to +/-10%	Commercial	PLCC44	Stick
TS80C58X2xxx-MCC	-5 to +/-10%	Commercial	PQFP44	Tray
TS80C58X2xxx-MCE	-5 to +/-10%	Commercial	VQFP44	Tray
TS80C58X2xxx-VCA	-5 to +/-10%	Commercial	PDIL40	Stick
TS80C58X2xxx-VCB	-5 to +/-10%	Commercial	PLCC44	Stick
TS80C58X2xxx-VCC	-5 to +/-10%	Commercial	PQFP44	Tray
TS80C58X2xxx-VCE	-5 to +/-10%	Commercial	VQFP44	Tray
TS80C58X2xxx-LCA	-5 to +/-10%	Commercial	PDIL40	Stick
TS80C58X2xxx-LCB	-5 to +/-10%	Commercial	PLCC44	Stick
TS80C58X2xxx-LCC	-5 to +/-10%	Commercial	PQFP44	Tray
TS80C58X2xxx-LCE	-5 to +/-10%	Commercial	VQFP44	Tray
TS80C58X2xxx-MIA	-5 to +/-10%	Industrial	PDIL40	Stick
TS80C58X2xxx-MIB	-5 to +/-10%	Industrial	PLCC44	Stick
TS80C58X2xxx-MIC	-5 to +/-10%	Industrial	PQFP44	Tray
TS80C58X2xxx-MIE	-5 to +/-10%	Industrial	VQFP44	Tray
TS80C58X2xxx-VIA	-5 to +/-10%	Industrial	PDIL40	Stick
TS80C58X2xxx-VIB	-5 to +/-10%	Industrial	PLCC44	Stick
TS80C58X2xxx-VIC	-5 to +/-10%	Industrial	PQFP44	Tray
TS80C58X2xxx-VIE	-5 to +/-10%	Industrial	VQFP44	Tray
TS80C58X2xxx-LIA	-5 to +/-10%	Industrial	PDIL40	Stick
TS80C58X2xxx-LIB	-5 to +/-10%	Industrial	PLCC44	Stick
TS80C58X2xxx-LIC	-5 to +/-10%	Industrial	PQFP44	Tray
TS80C58X2xxx-LIE	-5 to +/-10%	Industrial	VQFP44	Tray
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AT80C58X2zzz-3CSUM	-5 to +/-10%	Industrial & Green	PDIL40	Stick
AT80C58X2zzz-SLSUM	-5 to +/-10%	Industrial & Green	PLCC44	Stick
AT80C58X2zzz-RLTUM	-5 to +/-10%	Industrial & Green	VQFP44	Tray
AT80C58X2zzz-3CSUL	-5 to +/-10%	Industrial & Green	PDIL40	Stick
AT80C58X2zzz-SLSUL	-5 to +/-10%	Industrial & Green	PLCC44	Stick
AT80C58X2zzz-RLTUL	-5 to +/-10%	Industrial & Green	VQFP44	Tray
AT80C58X2zzz-3CSUV	-5 to +/-10%	Industrial & Green	PDIL40	Stick
AT80C58X2zzz-SLSUV	-5 to +/-10%	Industrial & Green	PLCC44	Stick
AT80C58X2zzz-RLTUV	-5 to +/-10%	Industrial & Green	VQFP44	Tray
TS87C58X2-MCA	5V ±10%	Commercial	PDIL40	Stick
TS87C58X2-MCB	5V ±10%	Commercial	PLCC44	Stick
TS87C58X2-MCC	5V ±10%	Commercial	PQFP44	Tray

AT/TS8xC54/8X2

Part Number	Supply Voltage	Temperature Range	Package	Packing
TS87C58X2-MCE	5V ±10%	Commercial	VQFP44	Tray
TS87C58X2-VCA	5V ±10%	Commercial	PDIL40	Stick
TS87C58X2-VCB	5V ±10%	Commercial	PLCC44	Stick
TS87C58X2-VCC	5V ±10%	Commercial	PQFP44	Tray
TS87C58X2-VCE	5V ±10%	Commercial	VQFP44	Tray
TS87C58X2-LCA	2.7 to 5.5V	Commercial	PDIL40	Stick
TS87C58X2-LCB	2.7 to 5.5V	Commercial	PLCC44	Stick
TS87C58X2-LCC	2.7 to 5.5V	Commercial	PQFP44	Tray
TS87C58X2-LCE	2.7 to 5.5V	Commercial	VQFP44	Tray
TS87C58X2-MIA	5V ±10%	Industrial	PDIL40	Stick
TS87C58X2-MIB	5V ±10%	Industrial	PLCC44	Stick
TS87C58X2-MIC	5V ±10%	Industrial	PQFP44	Tray
TS87C58X2-MIE	5V ±10%	Industrial	VQFP44	Tray
TS87C58X2-VIA	5V ±10%	Industrial	PDIL40	Stick
TS87C58X2-VIB	5V ±10%	Industrial	PLCC44	Stick
TS87C58X2-VIC	5V ±10%	Industrial	PQFP44	Tray
TS87C58X2-VIE	5V ±10%	Industrial	VQFP44	Tray
TS87C58X2-LIA	2.7 to 5.5V	Industrial	PDIL40	Stick
TS87C58X2-LIB	2.7 to 5.5V	Industrial	PLCC44	Stick
TS87C58X2-LIC	2.7 to 5.5V	Industrial	PQFP44	Tray
TS87C58X2-LIE	2.7 to 5.5V	Industrial	VQFP44	Tray
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AT87C58X2-3CSUM	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUM	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUM	5V ±10%	Industrial & Green	VQFP44	Tray
AT87C58X2-3CSUL	2.7 to 5.5V	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUL	2.7 to 5.5V	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUL	2.7 to 5.5V	Industrial & Green	VQFP44	Tray
AT87C58X2-3CSUV	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUV	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUV	5V ±10%	Industrial & Green	VQFP44	Tray

21. Datasheet Revision History

21.1 Changes from Rev. C 01/01 to Rev. D 11/05

1. Added green product Ordering Information.

21.2 Changes from Rev. D 11/05 to Rev. E 04/06

1. Changed value of AUXR register.

