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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

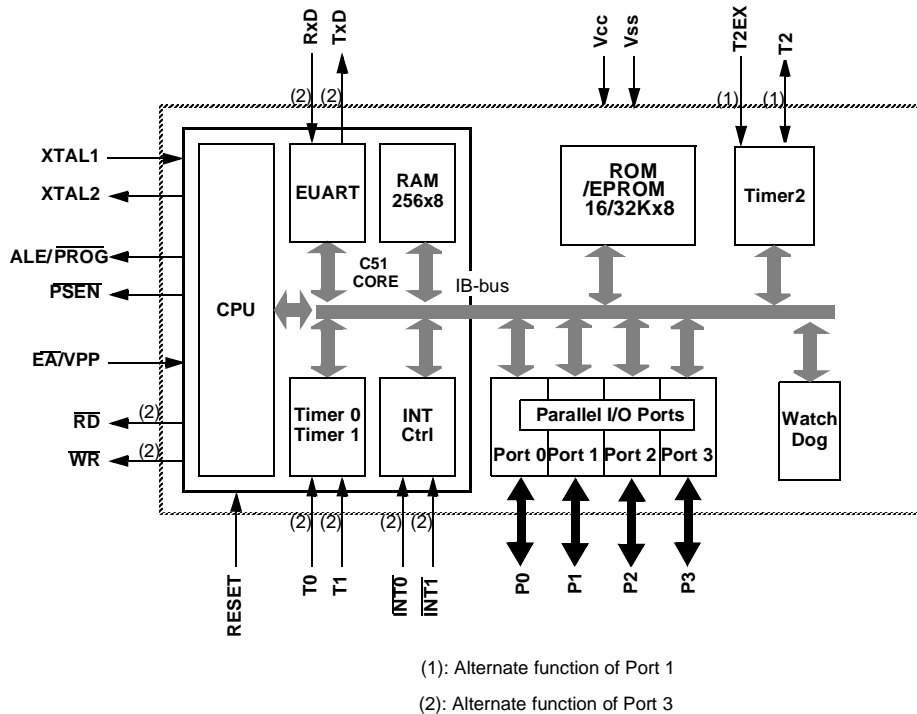
#### Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40/30MHz
Connectivity	UART/USART
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-PQFP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/ts87c58x2-vcc">https://www.e-xfl.com/product-detail/microchip-technology/ts87c58x2-vcc</a>

The TS80C54/58X2 has 2 software-selectable modes of reduced activity for further reduction in power consumption. In the idle mode the CPU is frozen while the timers, the serial port and the interrupt system are still operating. In the power-down mode the RAM is saved and all other functions are inoperative.

PDIL40 PLCC44 PQFP44 F1 VQFP44 1.4	ROM (bytes)	EPROM (bytes)
TS80C54X2	16k	0
TS80C58X2	32k	0
TS87C54X2	0	16k
TS87C58X2	0	32k

## 2. Block Diagram



**Table 5-1. Pin Description for 40/44 pin packages**

MNEMONIC	PIN NUMBER			TYPE	Name And Function
	DIL	LCC	VQFP 1.4		
V <sub>SS</sub>	20	22	16	I	<b>Ground:</b> 0V reference
V <sub>SS1</sub>		1	39	I	Optional Ground: <b>Contact the Sales Office for ground connection.</b>
V <sub>CC</sub>	40	44	38	I	<b>Power Supply:</b> This is the power supply voltage for normal, idle and power-down operation
P0.0-P0.7	39-32	43-36	37-30	I/O	<b>Port 0:</b> Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. Port 0 pins must be polarized to V <sub>CC</sub> or V <sub>SS</sub> in order to prevent any parasitic current consumption. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-up when emitting 1s. Port 0 also inputs the code bytes during EPROM programming. External pull-ups are required during program verification during which P0 outputs the code bytes.
P1.0-P1.7	1-8	2-9	40-44 1-3	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups. Port 1 also receives the low-order address byte during memory programming and verification. Alternate functions for Port 1 include:
	1	2	40	I/O	<b>T2 (P1.0):</b> Timer/Counter 2 external count input/Clockout
	2	3	41	I	<b>T2EX (P1.1):</b> Timer/Counter 2 Reload/Capture/Direction Control
P2.0-P2.7	21-28	24-31	18-25	I/O	<b>Port 2:</b> Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 emits the contents of the P2 SFR. Some Port 2 pins receive the high order address bits during EPROM programming and verification: P2.0 to P2.5 for A8 to A13
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	<b>Port 3:</b> Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Some Port 3 pin P3.4 receive the high order address bits during EPROM programming and verification for TS8xC58X2 devices. Port 3 also serves the special features of the 80C51 family, as listed below.
	10	11	5	I	<b>RXD (P3.0):</b> Serial input port
	11	13	7	O	<b>TXD (P3.1):</b> Serial output port
	12	14	8	I	<b>INT0 (P3.2):</b> External interrupt 0
	13	15	9	I	<b>INT1 (P3.3):</b> External interrupt 1
	14	16	10	I	<b>T0 (P3.4):</b> Timer 0 external input
	15	17	11	I	<b>T1 (P3.5):</b> Timer 1 external input
	16	18	12	O	<b>WR (P3.6):</b> External data memory write strobe
	17	19	13	O	<b>RD (P3.7):</b> External data memory read strobe P3.4 also receives A14 during TS87C58X2 EPROM Programming.
Reset	9	10	4	I	<b>Reset:</b> A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V <sub>SS</sub> permits a power-on reset using only an external capacitor to V <sub>CC</sub> .

**Table 7-1.** AUXR1: Auxiliary Register 1

7	6	5	4	3	2	1	0
-	-	-	-	GF3	0	-	DPS

Bit Number	Bit Mnemonic	Description
7	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
4	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
3	GF3	This bit is a general purpose user flag
2	0	<b>Reserved</b> Always stuck at 0.
1	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
0	DPS	<b>Data Pointer Selection</b> Clear to select DPTR0. Set to select DPTR1.

Reset Value = XXXX 00X0

Not bit addressable

User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new feature. In that case, the reset value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

## 7.1 Application

Software can take advantage of the additional data pointers to both increase speed and reduce code size, for example, block operations (copy, compare, search ...) are well served by using one data pointer as a 'source' pointer and the other one as a "destination" pointer.

### ASSEMBLY LANGUAGE

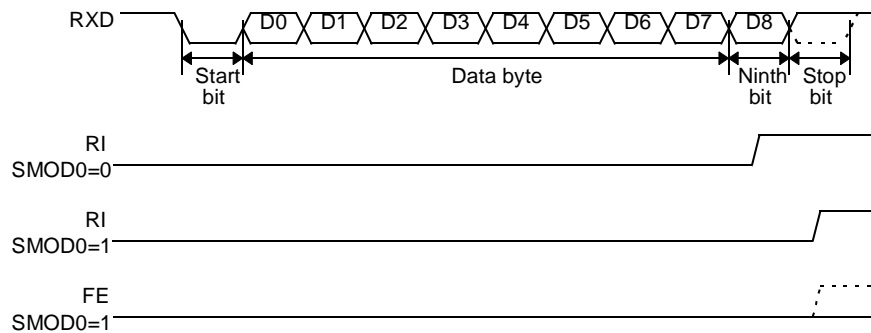
```

; Block move using dual data pointers
; Destroys DPTR0, DPTR1, A and PSW
; note: DPS exits opposite of entry state
; unless an extra INC AUXR1 is added
;
00A2          AUXR1 EQU 0A2H
;
0000 909000   MOV  DPTR,#SOURCE      ; address of SOURCE
0003 05A2     INC  AUXR1              ; switch data pointers
0005 90A000   MOV  DPTR,#DEST       ; address of DEST
0008          LOOP:
0008 05A2     INC  AUXR1              ; switch data pointers
000A E0       MOVX A,@DPTR          ; get a byte from SOURCE
000B A3       INC  DPTR              ; increment SOURCE address
000C 05A2     INC  AUXR1              ; switch data pointers
000E F0       MOVX @DPTR,A          ; write the byte to DEST
000F A3       INC  DPTR              ; increment DEST address
0010 70F6     JNZ  LOOP              ; check for 0 terminator
0012 05A2     INC  AUXR1              ; (optional) restore DPS

```

INC is a short (2 bytes) and fast (12 clocks) way to manipulate the DPS bit in the AUXR1 SFR. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry. Observe that without the last instruction (INC AUXR1), the routine will exit with DPS in the opposite state.

**Figure 9-3.** UART Timings in Modes 2 and 3



### 9.1.1 Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.

To support automatic address recognition, a device is identified by a given address and a broadcast address.

**NOTE:** The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).

### 9.1.2 Given Address

Each device has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don't-care bits (defined by zeros) to form the device's given address. The don't-care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed.

To address a device by its individual address, the SADEN mask byte must be 1111 1111b.

For example:

SADDR	0101 0110b
SADEN	1111 1100b
Given	0101 01XXb

**Table 9-3.** SCON Register  
SCON - Serial Control Register (98h)

7	6	5	4	3	2	1	0																				
FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI																				
Bit Number	Bit Mnemonic	Description																									
7	FE	<b>Framing Error bit (SMOD0=1)</b> Clear to reset the error state, not cleared by a valid stop bit. Set by hardware when an invalid stop bit is detected. SMOD0 must be set to enable access to the FE bit																									
	SM0	<b>Serial port Mode bit 0</b> Refer to SM1 for serial port mode selection. SMOD0 must be cleared to enable access to the SM0 bit																									
6	SM1	<b>Serial port Mode bit 1</b> <table border="1"> <thead> <tr> <th>SM0</th> <th>SM1Mode</th> <th>Description</th> <th>Baud Rate</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Shift Register <math>F_{XTAL}/12</math> (/6 in X2 mode)</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>8-bit UARTVariable</td> </tr> <tr> <td>1</td> <td>0</td> <td>2</td> <td>9-bit UART <math>F_{XTAL}/64</math> or <math>F_{XTAL}/32</math> (/32, /16 in X2 mode)</td> </tr> <tr> <td>1</td> <td>1</td> <td>3</td> <td>9-bit UARTVariable</td> </tr> </tbody> </table>						SM0	SM1Mode	Description	Baud Rate	0	0	0	Shift Register $F_{XTAL}/12$ (/6 in X2 mode)	0	1	1	8-bit UARTVariable	1	0	2	9-bit UART $F_{XTAL}/64$ or $F_{XTAL}/32$ (/32, /16 in X2 mode)	1	1	3	9-bit UARTVariable
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1	1	3	9-bit UARTVariable																								
5	SM2	<b>Serial port Mode 2 bit / Multiprocessor Communication Enable bit</b> Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0.																									
4	REN	<b>Reception Enable bit</b> Clear to disable serial reception. Set to enable serial reception.																									
3	TB8	Transmitter Bit 8 / Ninth bit to transmit in modes 2 and 3. Clear to transmit a logic 0 in the 9th bit. Set to transmit a logic 1 in the 9th bit.																									
2	RB8	<b>Receiver Bit 8 / Ninth bit received in modes 2 and 3</b> Cleared by hardware if 9th bit received is a logic 0. Set by hardware if 9th bit received is a logic 1. In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used.																									
1	TI	<b>Transmit Interrupt flag</b> Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes.																									
0	RI	<b>Receive Interrupt flag</b> Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0, see Figure 9-2. and Figure 9-3. in the other modes.																									

Reset Value = 0000 0000b

Bit addressable



If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

**Table 10-2.** IE Register  
IE - Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	-	ET2	ES	ET1	EX1	ET0	EX0

Bit Number	Bit Mnemonic	Description
7	EA	Enable All interrupt bit Clear to disable all interrupts. Set to enable all interrupts. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its own interrupt enable bit.
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
5	ET2	Timer 2 overflow interrupt Enable bit Clear to disable timer 2 overflow interrupt. Set to enable timer 2 overflow interrupt.
4	ES	Serial port Enable bit Clear to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	Timer 1 overflow interrupt Enable bit Clear to disable timer 1 overflow interrupt. Set to enable timer 1 overflow interrupt.
2	EX1	External interrupt 1 Enable bit Clear to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	Timer 0 overflow interrupt Enable bit Clear to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.
0	EX0	External interrupt 0 Enable bit Clear to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0X00 0000b

Bit addressable



**Table 10-4.** IPH Register  
IPH - Interrupt Priority High Register (B7h)

7	6	5	4	3	2	1	0															
-	-	PT2H	PSH	PT1H	PX1H	PT0H	PX0H															
Bit Number	Bit Mnemonic	Description																				
7	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.																				
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.																				
5	PT2H	Timer 2 overflow interrupt Priority High bit <table border="1"> <thead> <tr> <th>PT2H</th> <th>PT2</th> <th>Priority Level</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Lowest</td> </tr> <tr> <td>0</td> <td>1</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>Highest</td> </tr> </tbody> </table>						PT2H	PT2	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PT2H	PT2	Priority Level																				
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0	1																					
1	0																					
1	1	Highest																				
4	PSH	Serial port Priority High bit <table border="1"> <thead> <tr> <th>PSH</th> <th>PS</th> <th>Priority Level</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Lowest</td> </tr> <tr> <td>0</td> <td>1</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>Highest</td> </tr> </tbody> </table>						PSH	PS	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
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0	1																					
1	0																					
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3	PT1H	Timer 1 overflow interrupt Priority High bit <table border="1"> <thead> <tr> <th>PT1H</th> <th>PT1</th> <th>Priority Level</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Lowest</td> </tr> <tr> <td>0</td> <td>1</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>Highest</td> </tr> </tbody> </table>						PT1H	PT1	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PT1H	PT1	Priority Level																				
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0	1																					
1	0																					
1	1	Highest																				
2	PX1H	External interrupt 1 Priority High bit <table border="1"> <thead> <tr> <th>PX1H</th> <th>PX1</th> <th>Priority Level</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Lowest</td> </tr> <tr> <td>0</td> <td>1</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>Highest</td> </tr> </tbody> </table>						PX1H	PX1	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PX1H	PX1	Priority Level																				
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PT0H	PT0	Priority Level																				
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PX0H	PX0	Priority Level																				
0	0	Lowest																				
0	1																					
1	0																					
1	1	Highest																				

Reset Value = XX00 0000b

Not bit addressable

## 11. Idle mode

An instruction that sets PCON.0 causes that to be the last instruction executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer, and Serial Port functions. The CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels.

There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bits GF0 and GF1 can be used to give an indication if an interrupt occurred during normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

### 11.1 Power-Down Mode

To save maximum power, a power-down mode can be invoked by software (Refer to Table 9-4., PCON register).

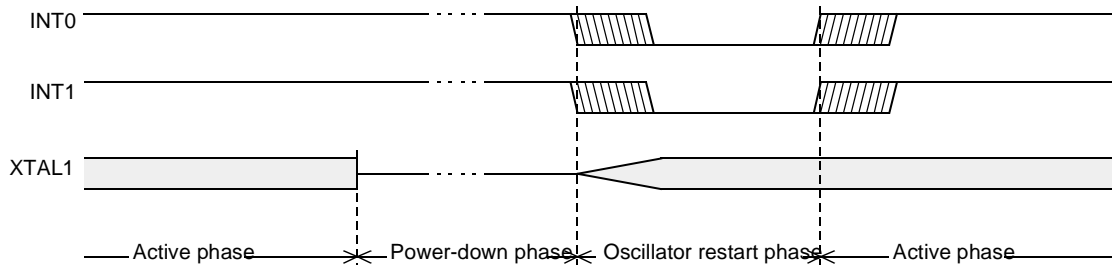
In power-down mode, the oscillator is stopped and the instruction that invoked power-down mode is the last instruction executed. The internal RAM and SFRs retain their value until the power-down mode is terminated.  $V_{CC}$  can be lowered to save further power. Either a hardware reset or an external interrupt can cause an exit from power-down. To properly terminate power-down, the reset or external interrupt should not be executed before  $V_{CC}$  is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.

Only external interrupts  $\overline{INT0}$  and  $\overline{INT1}$  are useful to exit from power-down. For that, interrupt must be enabled and configured as level or edge sensitive interrupt input.

Holding the pin low restarts the oscillator but bringing the pin high completes the exit as detailed in Figure 11-1. When both interrupts are enabled, the oscillator restarts as soon as one of the two inputs is held low and power down exit will be completed when the first input will be released. In this case the higher priority interrupt service routine is executed.

Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put TS80C54/58X2 into power-down mode.

**Figure 11-1.** Power-Down Exit Waveform



Exit from power-down by reset redefines all the SFRs, exit from power-down by external interrupt does not affect the SFRs.

Exit from power-down by either reset or external interrupt does not affect the internal RAM content.

*NOTE: If idle mode is activated with power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.*

**Table 11-1.** The state of ports during idle and power-down modes

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data*	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data*	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

\* Port 0 can force a "zero" level. A "one" Level will leave port floating.

## 12. Hardware Watchdog Timer

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upset. The WDT consists of a 14-bit counter and the WatchDog Timer ReSeT (WDTRST) SFR. The WDT is by default disabled from exiting reset. To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, it will increment every machine cycle while the oscillator is running and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST-pin.

### 12.1 Using the WDT

To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, the user needs to service it by writing to 01EH and 0E1H to WDTRST to avoid WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH) and this will reset the device. When WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycle. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST-pin. The RESET pulse duration is  $96 \times T_{OSC}$ , where  $T_{OSC} = 1/F_{OSC}$ . To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

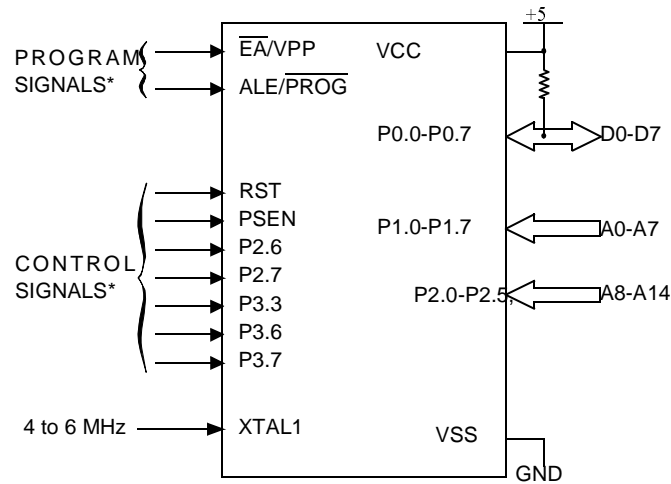
To have a more powerful WDT, a  $2^7$  counter has been added to extend the Time-out capability, ranking from 16ms to 2s @  $F_{OSC} = 12\text{MHz}$ . To manage this feature, refer to WDTPRG register description, Table 12-2. (SFR0A7h).

**Table 12-1.** WDTRST Register  
WDTRST Address (0A6h)

	7	6	5	4	3	2	1
Reset value	X	X	X	X	X	X	X

Write only, this SFR is used to reset/enable the WDT by writing 01EH then 0E1H in sequence.

Figure 17-1. Set-Up Modes Configuration



\* See Table 31. for proper value on these inputs

### 17.3.3 Programming Algorithm

The Improved Quick Pulse algorithm is based on the Quick Pulse algorithm and decreases the number of pulses applied during byte programming from 25 to 1.

To program the TS80C54/58X2 the following sequence must be exercised:

- Step 1: Activate the combination of control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Input the appropriate data on the data lines.
- Step 4: Raise  $\overline{EA}/VPP$  from VCC to VPP (typical 12.75V).
- Step 5: Pulse  $\overline{ALE}/\overline{PROG}$  once.
- Step 6: Lower  $\overline{EA}/VPP$  from VPP to VCC

Repeat step 2 through 6 changing the address and data for the entire array or until the end of the object file is reached (See Figure 17-2.).

### 17.3.4 Verify algorithm

Code array verify must be done after each byte or block of bytes is programmed. In either case, a complete verify of the programmed array will ensure reliable programming of the TS87C54/58X2.

P 2.7 is used to enable data output.

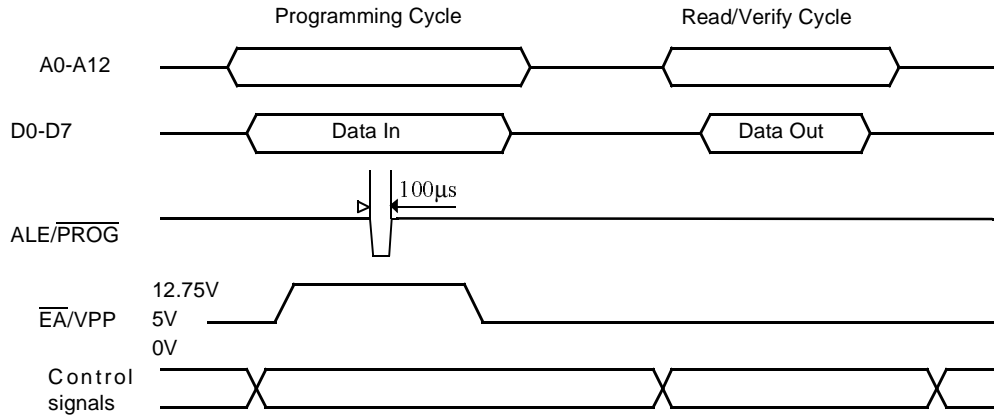
To verify the TS87C54/58X2 code the following sequence must be exercised:

- Step 1: Activate the combination of program and control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Read data on the data lines.

Repeat step 2 through 3 changing the address for the entire array verification (See Figure 17-2.)

The encryption array cannot be directly verified. Verification of the encryption array is done by observing that the code array is well encrypted.

**Figure 17-2.** Programming and Verification Signal's Waveform



## 17.4 EPROM Erasure (Windowed Packages Only)

Erasing the EPROM erases the code array, the encryption array and the lock bits returning the parts to full functionality.

Erasure leaves all the EPROM cells in a 1's state (FF).

### 17.4.1 Erasure Characteristics

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Å) to an integrated dose at least 15 W-sec/cm<sup>2</sup>. Exposing the EPROM to an ultraviolet lamp of 12,000 µW/cm<sup>2</sup> rating for 30 minutes, at a distance of about 25 mm, should be sufficient. An exposure of 1 hour is recommended with most of standard erasers.

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Å. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

## 18. Signature Bytes

The TS87C54/58X2 has four signature bytes in location 30h, 31h, 60h and 61h. To read these bytes follow the procedure for EPROM verify but activate the control lines provided in Table 31. for Read Signature Bytes. Table 18-1. shows the content of the signature byte for the TS80C54/58X2.

## 19.4 DC Parameters for Low Voltage

$T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ;  $V_{SS} = 0\text{ V}$ ;  $V_{CC} = 2.7\text{ V}$  to  $5.5\text{ V} \pm 10\%$ ;  $F = 0$  to  $30\text{ MHz}$ .

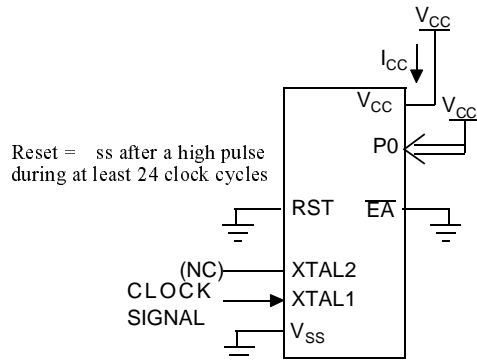
$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ;  $V_{SS} = 0\text{ V}$ ;  $V_{CC} = 2.7\text{ V}$  to  $5.5\text{ V} \pm 10\%$ ;  $F = 0$  to  $30\text{ MHz}$ .

**Table 19-2.** DC Parameters for Low Voltage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$V_{IL}$	Input Low Voltage	-0.5		$0.2 V_{CC} - 0.1$	V	
$V_{IH}$	Input High Voltage except XTAL1, RST	$0.2 V_{CC} + 0.9$		$V_{CC} + 0.5$	V	
$V_{IH1}$	Input High Voltage, XTAL1, RST	$0.7 V_{CC}$		$V_{CC} + 0.5$	V	
$V_{OL}$	Output Low Voltage, ports 1, 2, 3 <sup>(6)</sup>			0.45	V	$I_{OL} = 0.8\text{ mA}^{(4)}$
$V_{OL1}$	Output Low Voltage, port 0, ALE, $\overline{\text{PSEN}}$ <sup>(6)</sup>			0.45	V	$I_{OL} = 1.6\text{ mA}^{(4)}$
$V_{OH}$	Output High Voltage, ports 1, 2, 3	$0.9 V_{CC}$			V	$I_{OH} = -10\text{ }\mu\text{A}$
$V_{OH1}$	Output High Voltage, port 0, ALE, $\overline{\text{PSEN}}$	$0.9 V_{CC}$			V	$I_{OH} = -40\text{ }\mu\text{A}$
$I_{IL}$	Logical 0 Input Current ports 1, 2 and 3			-50	$\mu\text{A}$	$V_{in} = 0.45\text{ V}$
$I_{LI}$	Input Leakage Current			$\pm 10$	$\mu\text{A}$	$0.45\text{ V} < V_{in} < V_{CC}$
$I_{TL}$	Logical 1 to 0 Transition Current, ports 1, 2, 3			-650	$\mu\text{A}$	$V_{in} = 2.0\text{ V}$
$R_{RST}$	RST Pulldown Resistor	50	$90^{(5)}$	200	$\text{k}\Omega$	
$C_{IO}$	Capacitance of I/O Buffer			10	pF	$F_c = 1\text{ MHz}$ $T_A = 25^\circ\text{C}$
$I_{PD}$	Power Down Current		$20^{(5)}$ $10^{(5)}$	50 30	$\mu\text{A}$	$V_{CC} = 2.0\text{ V}$ to $5.5\text{ V}^{(3)}$ $V_{CC} = 2.0\text{ V}$ to $3.3\text{ V}^{(3)}$
$I_{CC}$ under RESET	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			1 + 0.2 Freq (MHz) @12MHz 3.4 @16MHz 4.2	mA	$V_{CC} = 3.3\text{ V}^{(1)}$
$I_{CC}$ operating	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			1 + 0.3 Freq (MHz) @12MHz 4.6 @16MHz 5.8	mA	$V_{CC} = 3.3\text{ V}^{(8)}$
$I_{CC}$ idle	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			0.15 Freq (MHz) + 0.2 @12MHz 2 @16MHz 2.6	mA	$V_{CC} = 3.3\text{ V}^{(2)}$

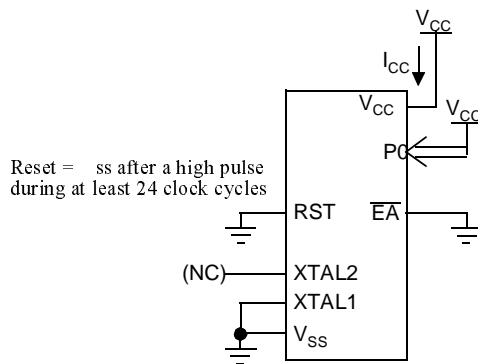
- $I_{CC}$  under reset is measured with all output pins disconnected; XTAL1 driven with  $T_{CLCH}$ ,  $T_{CHCL} = 5\text{ ns}$  (see Figure 19-5.),  $V_{IL} = V_{SS} + 0.5\text{ V}$ ,  $V_{IH} = V_{CC} - 0.5\text{ V}$ ; XTAL2 N.C.;  $\overline{\text{EA}} = \text{RST} = \text{Port } 0 = V_{CC}$ .  $I_{CC}$  would be slightly higher if a crystal oscillator used..
- Idle  $I_{CC}$  is measured with all output pins disconnected; XTAL1 driven with  $T_{CLCH}$ ,  $T_{CHCL} = 5\text{ ns}$ ,  $V_{IL} = V_{SS} + 0.5\text{ V}$ ,  $V_{IH} = V_{CC} - 0.5\text{ V}$ ; XTAL2 N.C; Port 0 =  $V_{CC}$ ;  $\overline{\text{EA}} = \text{RST} = V_{SS}$  (see Figure 19-3.).
- Power Down  $I_{CC}$  is measured with all output pins disconnected;  $\overline{\text{EA}} = V_{SS}$ , PORT 0 =  $V_{CC}$ ; XTAL2 NC.; RST =  $V_{SS}$  (see Figure 19-4.).
- Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the  $V_{OL}$ s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100pF), the noise pulse on the ALE line may exceed 0.45V with maxi  $V_{OL}$  peak 0.6V. A Schmitt Trigger use is not necessary.

**Figure 19-3.**  $I_{CC}$  Test Condition, Idle Mode



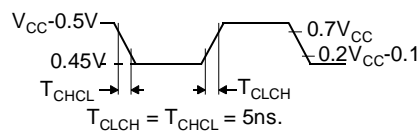
All other pins are disconnected.

**Figure 19-4.**  $I_{CC}$  Test Condition, Power-Down Mode



All other pins are disconnected.

**Figure 19-5.** Clock Signal Waveform for  $I_{CC}$  Tests in Active and Idle Modes



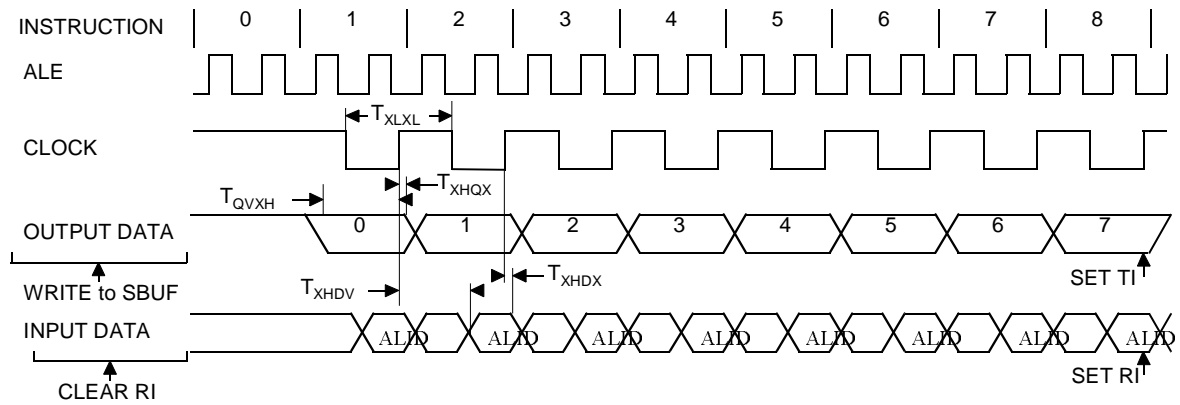


**Table 19-13.** AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
$T_{XLXL}$	Min	12 T	6 T				ns
$T_{QVXH}$	Min	10 T - x	5 T - x	50	50	50	ns
$T_{XHGX}$	Min	2 T - x	T - x	20	20	20	ns
$T_{XHDX}$	Min	x	x	0	0	0	ns
$T_{XHDV}$	Max	10 T - x	5 T - x	133	133	133	ns

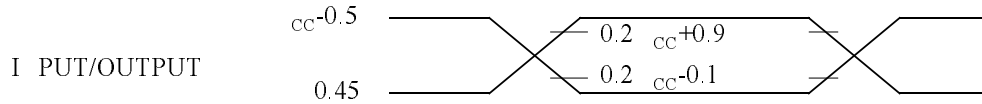
**19.5.8 Shift Register Timing Waveforms**

**Figure 19-9.** Shift Register Timing Waveforms



### 19.5.13 AC Testing Input/Output Waveforms

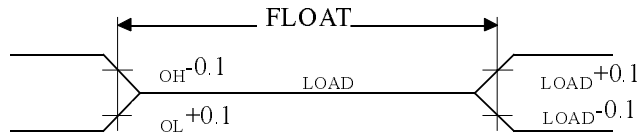
Figure 19-12. AC Testing Input/Output Waveforms



AC inputs during testing are driven at  $V_{CC} - 0.5$  for a logic "1" and  $0.45V$  for a logic "0". Timing measurement are made at  $V_{IH}$  min for a logic "1" and  $V_{IL}$  max for a logic "0".

### 19.5.14 Float Waveforms

Figure 19-13. Float Waveforms



For timing purposes a port pin is no longer floating when a  $100$  mV change from load voltage occurs and begins to float when a  $100$  mV change from the loaded  $V_{OH}/V_{OL}$  level occurs.  $I_{OL}/I_{OH} \geq \pm 20mA$ .

### 19.5.15 Clock Waveforms

Valid in normal clock mode. In X2 mode XTAL2 signal must be changed to XTAL2 divided by two.



## 20. Ordering Information

Table 20-1. Possible Ordering Entries

Part Number	Supply Voltage	Temperature Range	Package	Packing
TS80C54X2xxx-MCA	-5 to +/-10%	Commercial	PDIL40	Stick
TS80C54X2xxx-MCB	-5 to +/-10%	Commercial	PLCC44	Stick
TS80C54X2xxx-MCC	-5 to +/-10%	Commercial	PQFP44	Tray
TS80C54X2xxx-MCE	-5 to +/-10%	Commercial	VQFP44	Tray
TS80C54X2xxx-VCA	-5 to +/-10%	Commercial	PDIL40	Stick
TS80C54X2xxx-VCB	-5 to +/-10%	Commercial	PLCC44	Stick
TS80C54X2xxx-VCC	-5 to +/-10%	Commercial	PQFP44	Tray
TS80C54X2xxx-VCE	-5 to +/-10%	Commercial	VQFP44	Tray
TS80C54X2xxx-LCA	-5 to +/-10%	Commercial	PDIL40	Stick
TS80C54X2xxx-LCB	-5 to +/-10%	Commercial	PLCC44	Stick
TS80C54X2xxx-LCC	-5 to +/-10%	Commercial	PQFP44	Tray
TS80C54X2xxx-LCE	-5 to +/-10%	Commercial	VQFP44	Tray
TS80C54X2xxx-MIA	-5 to +/-10%	Industrial	PDIL40	Stick
TS80C54X2xxx-MIB	-5 to +/-10%	Industrial	PLCC44	Stick
TS80C54X2xxx-MIC	-5 to +/-10%	Industrial	PQFP44	Tray
TS80C54X2xxx-MIE	-5 to +/-10%	Industrial	VQFP44	Tray
TS80C54X2xxx-VIA	-5 to +/-10%	Industrial	PDIL40	Stick
TS80C54X2xxx-VIB	-5 to +/-10%	Industrial	PLCC44	Stick
TS80C54X2xxx-VIC	-5 to +/-10%	Industrial	PQFP44	Tray
TS80C54X2xxx-VIE	-5 to +/-10%	Industrial	VQFP44	Tray
TS80C54X2xxx-LIA	-5 to +/-10%	Industrial	PDIL40	Stick
TS80C54X2xxx-LIB	-5 to +/-10%	Industrial	PLCC44	Stick
TS80C54X2xxx-LIC	-5 to +/-10%	Industrial	PQFP44	Tray
TS80C54X2xxx-LIE	-5 to +/-10%	Industrial	VQFP44	Tray
AT80C54X2zzz-3CSUM	-5 to +/-10%	Industrial & Green	PDIL40	Stick
AT80C54X2zzz-SLSUM	-5 to +/-10%	Industrial & Green	PLCC44	Stick
AT80C54X2zzz-RLTUM	-5 to +/-10%	Industrial & Green	VQFP44	Tray
AT80C54X2zzz-3CSUL	-5 to +/-10%	Industrial & Green	PDIL40	Stick
AT80C54X2zzz-SLSUL	-5 to +/-10%	Industrial & Green	PLCC44	Stick
AT80C54X2zzz-RLTUL	-5 to +/-10%	Industrial & Green	VQFP44	Tray
AT80C54X2zzz-3CSUV	-5 to +/-10%	Industrial & Green	PDIL40	Stick
AT80C54X2zzz-SLSUV	-5 to +/-10%	Industrial & Green	PLCC44	Stick
AT80C54X2zzz-RLTUV	-5 to +/-10%	Industrial & Green	VQFP44	Tray
TS87C54X2-MCA	5V ±10%	Commercial	PDIL40	Stick
TS87C54X2-MCB	5V ±10%	Commercial	PLCC44	Stick

Part Number	Supply Voltage	Temperature Range	Package	Packing
TS80C58X2xxx-MCA	-5 to +/-10%	Commercial	PDIL40	Stick
TS80C58X2xxx-MCB	-5 to +/-10%	Commercial	PLCC44	Stick
TS80C58X2xxx-MCC	-5 to +/-10%	Commercial	PQFP44	Tray
TS80C58X2xxx-MCE	-5 to +/-10%	Commercial	VQFP44	Tray
TS80C58X2xxx-VCA	-5 to +/-10%	Commercial	PDIL40	Stick
TS80C58X2xxx-VCB	-5 to +/-10%	Commercial	PLCC44	Stick
TS80C58X2xxx-VCC	-5 to +/-10%	Commercial	PQFP44	Tray
TS80C58X2xxx-VCE	-5 to +/-10%	Commercial	VQFP44	Tray
TS80C58X2xxx-LCA	-5 to +/-10%	Commercial	PDIL40	Stick
TS80C58X2xxx-LCB	-5 to +/-10%	Commercial	PLCC44	Stick
TS80C58X2xxx-LCC	-5 to +/-10%	Commercial	PQFP44	Tray
TS80C58X2xxx-LCE	-5 to +/-10%	Commercial	VQFP44	Tray
TS80C58X2xxx-MIA	-5 to +/-10%	Industrial	PDIL40	Stick
TS80C58X2xxx-MIB	-5 to +/-10%	Industrial	PLCC44	Stick
TS80C58X2xxx-MIC	-5 to +/-10%	Industrial	PQFP44	Tray
TS80C58X2xxx-MIE	-5 to +/-10%	Industrial	VQFP44	Tray
TS80C58X2xxx-VIA	-5 to +/-10%	Industrial	PDIL40	Stick
TS80C58X2xxx-VIB	-5 to +/-10%	Industrial	PLCC44	Stick
TS80C58X2xxx-VIC	-5 to +/-10%	Industrial	PQFP44	Tray
TS80C58X2xxx-VIE	-5 to +/-10%	Industrial	VQFP44	Tray
TS80C58X2xxx-LIA	-5 to +/-10%	Industrial	PDIL40	Stick
TS80C58X2xxx-LIB	-5 to +/-10%	Industrial	PLCC44	Stick
TS80C58X2xxx-LIC	-5 to +/-10%	Industrial	PQFP44	Tray
TS80C58X2xxx-LIE	-5 to +/-10%	Industrial	VQFP44	Tray
AT80C58X2zzz-3CSUM	-5 to +/-10%	Industrial & Green	PDIL40	Stick
AT80C58X2zzz-SLSUM	-5 to +/-10%	Industrial & Green	PLCC44	Stick
AT80C58X2zzz-RLTUM	-5 to +/-10%	Industrial & Green	VQFP44	Tray
AT80C58X2zzz-3CSUL	-5 to +/-10%	Industrial & Green	PDIL40	Stick
AT80C58X2zzz-SLSUL	-5 to +/-10%	Industrial & Green	PLCC44	Stick
AT80C58X2zzz-RLTUL	-5 to +/-10%	Industrial & Green	VQFP44	Tray
AT80C58X2zzz-3CSUV	-5 to +/-10%	Industrial & Green	PDIL40	Stick
AT80C58X2zzz-SLSUV	-5 to +/-10%	Industrial & Green	PLCC44	Stick
AT80C58X2zzz-RLTUV	-5 to +/-10%	Industrial & Green	VQFP44	Tray
TS87C58X2-MCA	5V ±10%	Commercial	PDIL40	Stick
TS87C58X2-MCB	5V ±10%	Commercial	PLCC44	Stick
TS87C58X2-MCC	5V ±10%	Commercial	PQFP44	Tray

Part Number	Supply Voltage	Temperature Range	Package	Packing
TS87C58X2-MCE	5V ±10%	Commercial	VQFP44	Tray
TS87C58X2-VCA	5V ±10%	Commercial	PDIL40	Stick
TS87C58X2-VCB	5V ±10%	Commercial	PLCC44	Stick
TS87C58X2-VCC	5V ±10%	Commercial	PQFP44	Tray
TS87C58X2-VCE	5V ±10%	Commercial	VQFP44	Tray
TS87C58X2-LCA	2.7 to 5.5V	Commercial	PDIL40	Stick
TS87C58X2-LCB	2.7 to 5.5V	Commercial	PLCC44	Stick
TS87C58X2-LCC	2.7 to 5.5V	Commercial	PQFP44	Tray
TS87C58X2-LCE	2.7 to 5.5V	Commercial	VQFP44	Tray
TS87C58X2-MIA	5V ±10%	Industrial	PDIL40	Stick
TS87C58X2-MIB	5V ±10%	Industrial	PLCC44	Stick
TS87C58X2-MIC	5V ±10%	Industrial	PQFP44	Tray
TS87C58X2-MIE	5V ±10%	Industrial	VQFP44	Tray
TS87C58X2-VIA	5V ±10%	Industrial	PDIL40	Stick
TS87C58X2-VIB	5V ±10%	Industrial	PLCC44	Stick
TS87C58X2-VIC	5V ±10%	Industrial	PQFP44	Tray
TS87C58X2-VIE	5V ±10%	Industrial	VQFP44	Tray
TS87C58X2-LIA	2.7 to 5.5V	Industrial	PDIL40	Stick
TS87C58X2-LIB	2.7 to 5.5V	Industrial	PLCC44	Stick
TS87C58X2-LIC	2.7 to 5.5V	Industrial	PQFP44	Tray
TS87C58X2-LIE	2.7 to 5.5V	Industrial	VQFP44	Tray
AT87C58X2-3CSUM	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUM	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUM	5V ±10%	Industrial & Green	VQFP44	Tray
AT87C58X2-3CSUL	2.7 to 5.5V	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUL	2.7 to 5.5V	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUL	2.7 to 5.5V	Industrial & Green	VQFP44	Tray
AT87C58X2-3CSUV	5V ±10%	Industrial & Green	PDIL40	Stick
AT87C58X2-SLSUV	5V ±10%	Industrial & Green	PLCC44	Stick
AT87C58X2-RLTUV	5V ±10%	Industrial & Green	VQFP44	Tray

## 21. Datasheet Revision History

### 21.1 Changes from Rev. C 01/01 to Rev. D 11/05

1. Added green product Ordering Information.

### 21.2 Changes from Rev. D 11/05 to Rev. E 04/06

1. Changed value of AUXR register.