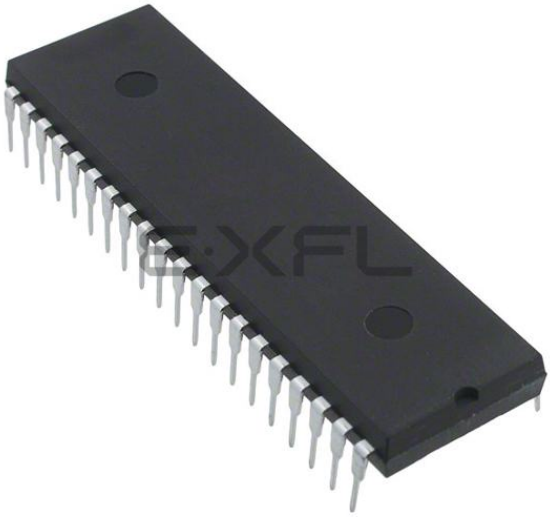

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | 80C51 |
| Core Size | 8-Bit |
| Speed | 40/30MHz |
| Connectivity | UART/USART |
| Peripherals | POR, WDT |
| Number of I/O | 32 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 40-DIP (0.600", 15.24mm) |
| Supplier Device Package | 40-PDIL |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/ts87c58x2-via |

**Table 5-1.** Pin Description for 40/44 pin packages

| MNEMONIC | PIN NUMBER | | | TYPE | Name And Function |
|---|---|---|---|---|---|
| | DIL | LCC | VQFP 1.4 | | |
| $V_{SS}$ | 20 | 22 | 16 | I | **Ground:** 0V reference |
| Vss1 | | 1 | 39 | I | Optional Ground: **Contact the Sales Office for ground connection.** |
| $V_{CC}$ | 40 | 44 | 38 | I | **Power Supply:** This is the power supply voltage for normal, idle and power-down operation |
| P0.0-P0.7 | 39-32 | 43-36 | 37-30 | I/O | **Port 0**: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. Port 0 pins must be polarized to Vcc or Vss in order to prevent any parasitic current consumption. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-up when emitting 1s. Port 0 also inputs the code bytes during EPROM programming. External pull-ups are required during program verification during which P0 outputs the code bytes. |
| | | | | | |
| P1.0-P1.7 | 1-8 | 2-9 | 40-44<br>1-3 | I/O | Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups. Port 1 also receives the low-order address byte during memory programming and verification.<br>Alternate functions for Port 1 include: |
| | | | | | |
| | 1 | 2 | 40 | I/O | **T2 (P1.0):** Timer/Counter 2 external count input/Clockout |
| | 2 | 3 | 41 | I | **T2EX (P1.1):** Timer/Counter 2 Reload/Capture/Direction Control |
| P2.0-P2.7 | 21-28 | 24-31 | 18-25 | I/O | **Port 2**: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR).In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 emits the contents of the P2 SFR. Some Port 2 pins receive the high order address bits during EPROM programming and verification:<br>P2.0 to P2.5 for A8 to A13 |
| | | | | | |
| P3.0-P3.7 | 10-17 | 11,<br>13-19 | 5,<br>7-13 | I/O | **Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Some Port 3 pin P3.4 receive the high order address bits during EPROM programming and verification for TS8xC58X2 devices.<br>Port 3 also serves the special features of the 80C51 family, as listed below. |
| | | | | | |
| | 10 | 11 | 5 | I | **RXD (P3.0):** Serial input port |
| | 11 | 13 | 7 | O | **TXD (P3.1):** Serial output port |
| | 12 | 14 | 8 | I | **$\overline{\text{INT0}}$ (P3.2):** External interrupt 0 |
| | 13 | 15 | 9 | I | **$\overline{\text{INT1}}$ (P3.3):** External interrupt 1 |
| | 14 | 16 | 10 | I | **T0 (P3.4):** Timer 0 external input |
| | 15 | 17 | 11 | I | **T1 (P3.5):** Timer 1 external input |
| | 16 | 18 | 12 | O | **$\overline{\text{WR}}$ (P3.6):** External data memory write strobe |
| | 17 | 19 | 13 | O | **$\overline{\text{RD}}$ (P3.7):** External data memory read strobe<br>P3.4 also receives A14 during TS87C58X2 EPROM Programming. |
| Reset | 9 | 10 | 4 | I | **Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to $V_{SS}$ permits a power-on reset using only an external capacitor to $V_{CC}$. |
| | | | | | |

# 6. TS80C54/58X2 Enhanced Features

In comparison to the original 80C52, the TS80C54/58X2 implements some new features, which are:

- The X2 option.
- The Dual Data Pointer.
- The Watchdog.
- The 4 level interrupt priority system.
- The power-off flag.
- The ONCE mode.
- The ALE disabling.
- Some enhanced features are also located in the UART and the timer 2.

## 6.1 X2 Feature

The TS80C54/58X2 core needs only 6 clock periods per machine cycle. This feature called ”X2” provides the following advantages:

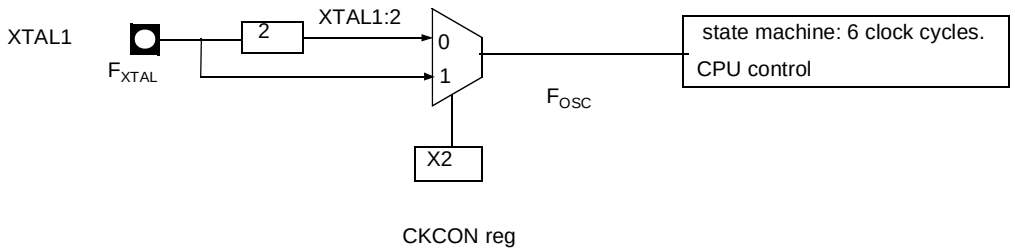
- Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power.
- Save power consumption while keeping same CPU power (oscillator power saving).
- Save power consumption by dividing dynamically operating frequency by 2 in operating and idle modes.
- Increase CPU power by 2 while keeping same crystal frequency.

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

### 6.1.1 Description

The clock for the whole circuit and peripheral is first divided by two before being used by the CPU core and peripherals. This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%. Figure 6-2. shows the clock generation block diagram. X2 bit is validated on XTAL1÷2 rising edge to avoid glitches when switching from X2 to STD mode. Figure 6-2. shows the mode switching waveforms.

**Figure 6-1.** Clock Generation Diagram



## 7. Dual Data Pointer Register Ddptr

The additional data pointer can be used to speed up code execution and reduce code size in a number of ways.

The dual DPTR structure is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called
DPS = AUXR1/bit0 (See Table 7-1.) that allows the program code to switch between them (Refer to Figure 7-1).

**Figure 7-1.** Use of Dual Pointer

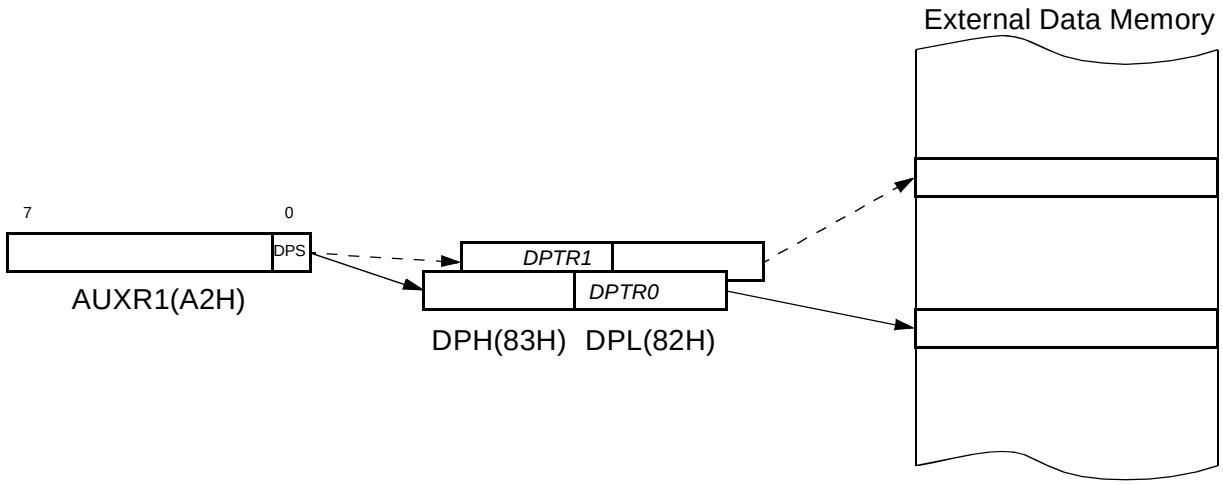


**Table 7-1.** AUXR1: Auxiliary Register 1

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | - | - | - | GF3 | 0 | - | DPS |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 6 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 5 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 4 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 3 | GF3 | This bit is a general purpose user flag |
| 2 | 0 | **Reserved**<br>Always stuck at 0. |
| 1 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 0 | DPS | **Data Pointer Selection**<br>Clear to select DPTR0.<br>Set to select DPTR1. |

Reset Value = XXXX 00X0
Not bit addressable

User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new feature. In that case, the reset value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

**Table 8-2.** T2MOD Register

T2MOD - Timer 2 Mode Control Register (C9h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | - | - | - | - | - | T2OE | DCEN |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 6 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 5 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 4 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 3 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 2 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 1 | T2OE | **Timer 2 Output Enable bit**<br>Clear to program P1.0/T2 as clock input or I/O port.<br>Set to program P1.0/T2 as clock output. |
| 0 | DCEN | **Down Counter Enable bit**<br>Clear to disable timer 2 as up/down counter.<br>Set to enable timer 2 as up/down counter. |

Reset Value = XXXX XX00b

Not bit addressable

**Table 9-3.** SCON Register

SCON - Serial Control Register (98h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **FE/SM0** | **SM1** | **SM2** | **REN** | **TB8** | **RB8** | **TI** | **RI** |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | FE | **Framing Error bit (SMOD0=1**)<br>Clear to reset the error state, not cleared by a valid stop bit.<br>Set by hardware when an invalid stop bit is detected.<br>SMOD0 must be set to enable access to the FE bit |
| | SM0 | **Serial port Mode bit 0**<br>Refer to SM1 for serial port mode selection.<br>SMOD0 must be cleared to enable access to the SM0 bit |
| 6 | SM1 | **Serial port Mode bit 1**<br>SM0 SM1Mode Description Baud Rate<br>0 0 0 Shift Register $F_{XTAL}$/12 (/6 in X2 mode)<br>0 1 1 8-bit UARTVariable<br>1 0 2 9-bit UART $F_{XTAL}$/64 or $F_{XTAL}$/32 (/32, /16 in X2 mode)<br>1 1 3 9-bit UARTVariable |
| 5 | SM2 | **Serial port Mode 2 bit / Multiprocessor Communication Enable bit**<br>Clear to disable multiprocessor communication feature.<br>Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0. |
| 4 | REN | **Reception Enable bit**<br>Clear to disable serial reception.<br>Set to enable serial reception. |
| 3 | TB8 | Transmitter Bit 8 / Ninth bit to transmit in modes 2 and 3.<br>Clear to transmit a logic 0 in the 9th bit.<br>Set to transmit a logic 1 in the 9th bit. |
| 2 | RB8 | **Receiver Bit 8 / Ninth bit received in modes 2 and 3**<br>Cleared by hardware if 9th bit received is a logic 0.<br>Set by hardware if 9th bit received is a logic 1.<br>In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used. |
| 1 | TI | **Transmit Interrupt flag**<br>Clear to acknowledge interrupt.<br>Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes. |
| 0 | RI | **Receive Interrupt flag**<br>Clear to acknowledge interrupt.<br>Set by hardware at the end of the 8th bit time in mode 0, see Figure 9-2. and Figure 9-3. in the other modes. |

Reset Value = 0000 0000b

Bit addressable

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

**Table 10-2.** IE Register

IE - Interrupt Enable Register (A8h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **EA** | **-** | **ET2** | **ES** | **ET1** | **EX1** | **ET0** | **EX0** |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | EA | Enable All interrupt bit<br>Clear to disable all interrupts.<br>Set to enable all interrupts.<br>If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its own interrupt enable bit. |
| 6 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 5 | ET2 | Timer 2 overflow interrupt Enable bit<br>Clear to disable timer 2 overflow interrupt.<br>Set to enable timer 2 overflow interrupt. |
| 4 | ES | Serial port Enable bit<br>Clear to disable serial port interrupt.<br>Set to enable serial port interrupt. |
| 3 | ET1 | Timer 1 overflow interrupt Enable bit<br>Clear to disable timer 1 overflow interrupt.<br>Set to enable timer 1 overflow interrupt. |
| 2 | EX1 | External interrupt 1 Enable bit<br>Clear to disable external interrupt 1.<br>Set to enable external interrupt 1. |
| 1 | ET0 | Timer 0 overflow interrupt Enable bit<br>Clear to disable timer 0 overflow interrupt.<br>Set to enable timer 0 overflow interrupt. |
| 0 | EX0 | External interrupt 0 Enable bit<br>Clear to disable external interrupt 0.<br>Set to enable external interrupt 0. |

Reset Value = 0X00 0000b

Bit addressable

**Table 10-4.** IPH Register

IPH - Interrupt Priority High Register (B7h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | - | PT2H | PSH | PT1H | PX1H | PT0H | PX0H |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 6 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 5 | PT2H | Timer 2 overflow interrupt Priority High bit<br>PT2H PT2 Priority Level<br>0 0 Lowest<br>0 1<br>1 0<br>1 1 Highest |
| 4 | PSH | Serial port Priority High bit<br>PSH PS Priority Level<br>0 0 Lowest<br>0 1<br>1 0<br>1 1 Highest |
| 3 | PT1H | Timer 1 overflow interrupt Priority High bit<br>PT1H PT1 Priority Level<br>0 0 Lowest<br>0 1<br>1 0<br>1 1 Highest |
| 2 | PX1H | External interrupt 1 Priority High bit<br>PX1H PX1 Priority Level<br>0 0 Lowest<br>0 1<br>1 0<br>1 1 Highest |
| 1 | PT0H | Timer 0 overflow interrupt Priority High bit<br>PT0H PT0 Priority Level<br>0 0 Lowest<br>0 1<br>1 0<br>1 1 Highest |
| 0 | PX0H | External interrupt 0 Priority High bit<br>PX0H PX0 Priority Level<br>0 0 Lowest<br>0 1<br>1 0<br>1 1 Highest |

Reset Value = XX00 0000b

Not bit addressable

# 11. Idle mode

An instruction that sets PCON.0 causes that to be the last instruction executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer, and Serial Port functions. The CPU status is preserved in its entirely : the Stack Pointer, Program Counter, Program Status Word, Accumulator and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels.

There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bits GF0 and GF1 can be used to give an indication if an interrupt occured during normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

## 11.1 Power-Down Mode

To save maximum power, a power-down mode can be invoked by software (Refer to Table 9-4., PCON register).

In power-down mode, the oscillator is stopped and the instruction that invoked power-down mode is the last instruction executed. The internal RAM and SFRs retain their value until the power-down mode is terminated. $V_{CC}$ can be lowered to save further power. Either a hardware reset or an external interrupt can cause an exit from power-down. To properly terminate power-down, the reset or external interrupt should not be executed before $V_{CC}$ is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.

Only external interrupts $\overline{INT0}$ and $\overline{INT1}$ are useful to exit from power-down. For that, interrupt must be enabled and configured as level or edge sensitive interrupt input.
Holding the pin low restarts the oscillator but bringing the pin high completes the exit as detailed in Figure 11-1. When both interrupts are enabled, the oscillator restarts as soon as one of the two inputs is held low and power down exit will be completed when the first input will be released. In this case the higher priority interrupt service routine is executed.
Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put TS80C54/58X2 into power-down mode.

# 12. Hardware Watchdog Timer

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upset. The WDT consists of a 14-bit counter and the WatchDog Timer ReSeT (WDTRST) SFR. The WDT is by default disabled from exiting reset. To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, it will increment every machine cycle while the oscillator is running and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST-pin.

## 12.1 Using the WDT

To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, the user needs to service it by writing to 01EH and 0E1H to WDTRST to avoid WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH) and this will reset the device. When WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycle. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST-pin. The RESET pulse duration is 96 x $T_{OSC}$ , where $T_{OSC}$ = $1/F_{OSC}$ . To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

To have a more powerful WDT, a $2^7$ counter has been added to extend the Time-out capability, ranking from 16ms to 2s @ $F_{OSC}$ = 12MHz. To manage this feature, refer to WDTPRG register description, Table 12-2. (SFR0A7h).

**Table 12-1.** WDTRST Register
WDTRST Address (0A6h)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|
| Reset value | X | X | X | X | X | X | X |

Write only, this SFR is used to reset/enable the WDT by writing 01EH then 0E1H in sequence.

# 13. ONCE™ Mode (ON Chip Emulation)

The ONCE mode facilitates testing and debugging of systems using TS80C54/58X2 without removing the circuit from the board. The ONCE mode is invoked by driving certain pins of the TS80C54/58X2; the following sequence must be exercised:

- Pull ALE low while the device is in reset (RST high) and $\overline{\text{PSEN}}$ is high.
- Hold ALE low as RST is deactivated.

While the TS80C54/58X2 is in ONCE mode, an emulator or test CPU can be used to drive the circuit Table 13-1 shows the status of the port pins during ONCE mode.

Normal operation is restored when normal reset is applied.

**Table 13-1.** External Pin Status during ONCE Mode

| ALE | PSEN | Port 0 | Port 1 | Port 2 | Port 3 | XTAL1/2 |
|---|---|---|---|---|---|---|
| Weak pull-up | Weak pull-up | Float | Weak pull-up | Weak pull-up | Weak pull-up | Active |

# 14. Power-Off Flag

The power-off flag allows the user to distinguish between a “cold start” reset and a “warm start” reset.

A cold start reset is the one induced by $V_{CC}$ switch-on. A warm start reset occurs while $V_{CC}$ is still applied to the device and could be generated for example by an exit from power-down.

The power-off flag (POF) is located in PCON register (See Table 14-1.). POF is set by hardware when $V_{CC}$ rises from 0 to its nominal voltage. The POF can be set or cleared by software allowing the user to determine the type of reset.

The POF value is only relevant with a Vcc range from 4.5V to 5.5V. For lower Vcc value, reading POF bit will return indeterminate value.

**Table 14-1.** PCON Register

PCON - Power Control Register (87h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **SMOD1** | **SMOD0** | **-** | **POF** | **GF1** | **GF0** | **PD** | **IDL** |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | SMOD1 | **Serial port Mode bit 1**<br>Set to select double baud rate in mode 1, 2 or 3. |
| 6 | SMOD0 | **Serial port Mode bit 0**<br>Clear to select SM0 bit in SCON register.<br>Set to to select FE bit in SCON register. |
| 5 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 4 | POF | **Power-Off Flag**<br>Clear to recognize next reset type.<br>Set by hardware when $V_{CC}$ rises from 0 to its nominal voltage. Can also be set by software. |
| 3 | GF1 | **General purpose Flag**<br>Cleared by user for general purpose usage.<br>Set by user for general purpose usage. |
| 2 | GF0 | **General purpose Flag**<br>Cleared by user for general purpose usage.<br>Set by user for general purpose usage. |
| 1 | PD | **Power-Down mode bit**<br>Cleared by hardware when reset occurs.<br>Set to enter power-down mode. |
| 0 | IDL | **Idle mode bit**<br>Clear by hardware when interrupt or reset occurs.<br>Set to enter idle mode. |

Reset Value = 00X1 0000b
Not bit addressable

# 17. TS87C54/58X2 EPROM

## 17.1 EPROM Structure

The TS87C54/58X2 EPROM is divided in two different arrays:

- the code array:16/32 Kbytes.
- the encryption array:64 bytes.
- In addition a third non programmable array is implemented:
- the signature array: 4 bytes.

## 17.2 EPROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

### 17.2.1 Encryption Array

Within the EPROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

### 17.2.2 Program Lock Bits

The three lock bits, when programmed according to Table 17-1., will provide different level of protection for the on-chip code and data.

**Table 17-1.** Program Lock bits

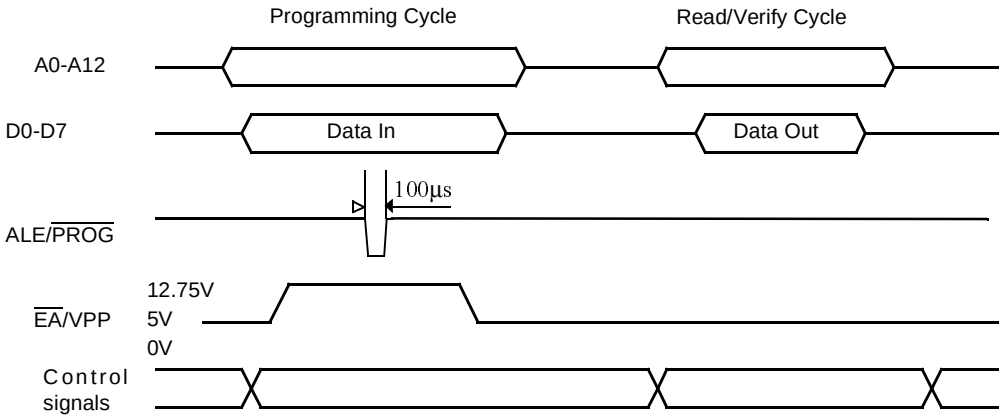
| Program Lock Bits | | | | |
|---|---|---|---|---|
| **Security level** | **LB1** | **LB2** | **LB3** | **Protection Description** |
| 1 | U | U | U | No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data. |
| 2 | P | U | U | MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the EPROM is disabled. |
| 3 | U | P | U | Same as 2, also verify is disabled. |
| 4 | U | U | P | Same as 3, also external execution is disabled. |

U: unprogrammed,
P: programmed

WARNING: Security level 2 and 3 should only be programmed after EPROM and Core verification.

The encryption array cannot be directly verified. Verification of the encryption array is done by observing that the code array is well encrypted.

**Figure 17-2.** Programming and Verification Signal's Waveform




## 17.4 EPROM Erasure (Windowed Packages Only)

Erasing the EPROM erases the code array, the encryption array and the lock bits returning the parts to full functionality.

Erasure leaves all the EPROM cells in a 1's state (FF).

### 17.4.1 Erasure Characteristics

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Å) to an integrated dose at least 15 W-sec/cm$^2$. Exposing the EPROM to an ultraviolet lamp of 12,000 µW/cm$^2$ rating for 30 minutes, at a distance of about 25 mm, should be sufficient. An exposure of 1 hour is recommended with most of standard erasers.

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Å. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

# 18. Signature Bytes

The TS87C54/58X2 has four signature bytes in location 30h, 31h, 60h and 61h. To read these bytes follow the procedure for EPROM verify but activate the control lines provided in Table 31. for Read Signature Bytes. Table 18-1. shows the content of the signature byte for the TS80C54/58X2.

### 19.5.2 External Program Memory Characteristics

**Table 19-5.** Symbol Description

| Symbol | Parameter |
|---|---|
| T | Oscillator clock period |
| $T_{LHLL}$ | ALE pulse width |
| $T_{AVLL}$ | Address Valid to ALE |
| $T_{LLAX}$ | Address Hold After ALE |
| $T_{LLIV}$ | ALE to Valid Instruction In |
| $T_{LLPL}$ | ALE to $\overline{PSEN}$ |
| $T_{PLPH}$ | $\overline{PSEN}$ Pulse Width |
| $T_{PLIV}$ | $\overline{PSEN}$ to Valid Instruction In |
| $T_{PXIX}$ | Input Instruction Hold After $\overline{PSEN}$ |
| $T_{PXIZ}$ | Input Instruction FloatAfter $\overline{PSEN}$ |
| $T_{PXAV}$ | $\overline{PSEN}$ to Address Valid |
| $T_{AVIV}$ | Address to Valid Instruction In |
| $T_{PLAZ}$ | $\overline{PSEN}$ Low to Address Float |

**Table 19-6.** AC Parameters for Fix Clock

| Speed | -M 40 MHz | | -V X2 mode 30 MHz 60 MHz equiv. | | -V standard mode 40 MHz | | -L X2 mode 20 MHz 40 MHz equiv. | | -L standard mode 30 MHz | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| T | 25 | | 33 | | 25 | | 50 | | 33 | | ns |
| $T_{LHLL}$ | 40 | | 25 | | 42 | | 35 | | 52 | | ns |
| $T_{AVLL}$ | 10 | | 4 | | 12 | | 5 | | 13 | | ns |
| $T_{LLAX}$ | 10 | | 4 | | 12 | | 5 | | 13 | | ns |
| $T_{LLIV}$ | | 70 | | 45 | | 78 | | 65 | | 98 | ns |
| $T_{LLPL}$ | 15 | | 9 | | 17 | | 10 | | 18 | | ns |
| $T_{PLPH}$ | 55 | | 35 | | 60 | | 50 | | 75 | | ns |
| $T_{PLIV}$ | | 35 | | 25 | | 50 | | 30 | | 55 | ns |
| $T_{PXIX}$ | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $T_{PXIZ}$ | | 18 | | 12 | | 20 | | 10 | | 18 | ns |
| $T_{AVIV}$ | | 85 | | 53 | | 95 | | 80 | | 122 | ns |
| $T_{PLAZ}$ | | 10 | | 10 | | 10 | | 10 | | 10 | ns |

### 19.5.4 External Data Memory Characteristics

**Table 19-8.** Symbol Description

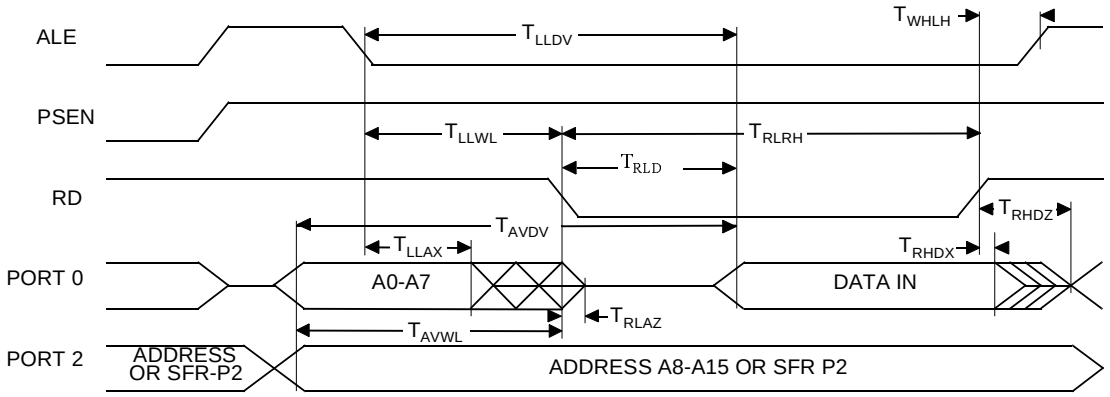
| Symbol | Parameter |
|---|---|
| $T_{RLRH}$ | $\overline{RD}$ Pulse Width |
| $T_{WLWH}$ | $\overline{WR}$ Pulse Width |
| $T_{RLDV}$ | $\overline{RD}$ to Valid Data In |
| $T_{RHDX}$ | Data Hold After $\overline{RD}$ |
| $T_{RHDZ}$ | Data Float After $\overline{RD}$ |
| $T_{LLDV}$ | ALE to Valid Data In |
| $T_{AVDV}$ | Address to Valid Data In |
| $T_{LLWL}$ | ALE to $\overline{WR}$ or $\overline{RD}$ |
| $T_{AVWL}$ | Address to $\overline{WR}$ or $\overline{RD}$ |
| $T_{QVWX}$ | Data Valid to $\overline{WR}$ Transition |
| $T_{QVWH}$ | Data set-up to $\overline{WR}$ High |
| $T_{WHQX}$ | Data Hold After $\overline{WR}$ |
| $T_{RLAZ}$ | $\overline{RD}$ Low to Address Float |
| $T_{WHLH}$ | $\overline{RD}$ or $\overline{WR}$ High to ALE high |

**Table 19-9.** AC Parameters for a Fix Clock

| Speed | -M 40 MHz | | -V X2 mode 30 MHz 60 MHz equiv. | | -V standard mode 40 MHz | | -L X2 mode 20 MHz 40 MHz equiv. | | -L standard mode 30 MHz | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Symbol | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| $T_{RLRH}$ | 130 | | 85 | | 135 | | 125 | | 175 | | ns |
| $T_{WLWH}$ | 130 | | 85 | | 135 | | 125 | | 175 | | ns |
| $T_{RLDV}$ | | 100 | | 60 | | 102 | | 95 | | 137 | ns |
| $T_{RHDX}$ | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $T_{RHDZ}$ | | 30 | | 18 | | 35 | | 25 | | 42 | ns |
| $T_{LLDV}$ | | 160 | | 98 | | 165 | | 155 | | 222 | ns |
| $T_{AVDV}$ | | 165 | | 100 | | 175 | | 160 | | 235 | ns |
| $T_{LLWL}$ | 50 | 100 | 30 | 70 | 55 | 95 | 45 | 105 | 70 | 130 | ns |
| $T_{AVWL}$ | 75 | | 47 | | 80 | | 70 | | 103 | | ns |
| $T_{QVWX}$ | 10 | | 7 | | 15 | | 5 | | 13 | | ns |
| $T_{QVWH}$ | 160 | | 107 | | 165 | | 155 | | 213 | | ns |
| $T_{WHQX}$ | 15 | | 9 | | 17 | | 10 | | 18 | | ns |
| $T_{RLAZ}$ | | 0 | | 0 | | 0 | | 0 | | 0 | ns |
| $T_{WHLH}$ | 10 | 40 | 7 | 27 | 15 | 35 | 5 | 45 | 13 | 53 | ns |

### 19.5.6 External Data Memory Read Cycle

**Figure 19-8.** External Data Memory Read Cycle




### 19.5.7 Serial Port Timing - Shift Register Mode

**Table 19-11.** Symbol Description

| Symbol | Parameter |
|---|---|
| $T_{XLXL}$ | Serial port clock cycle time |
| $T_{QVHX}$ | Output data set-up to clock rising edge |
| $T_{XHQX}$ | Output data hold after clock rising edge |
| $T_{XHDX}$ | Input data hold after clock rising edge |
| $T_{XHDV}$ | Clock rising edge to input data valid |

**Table 19-12.** AC Parameters for a Fix Clock

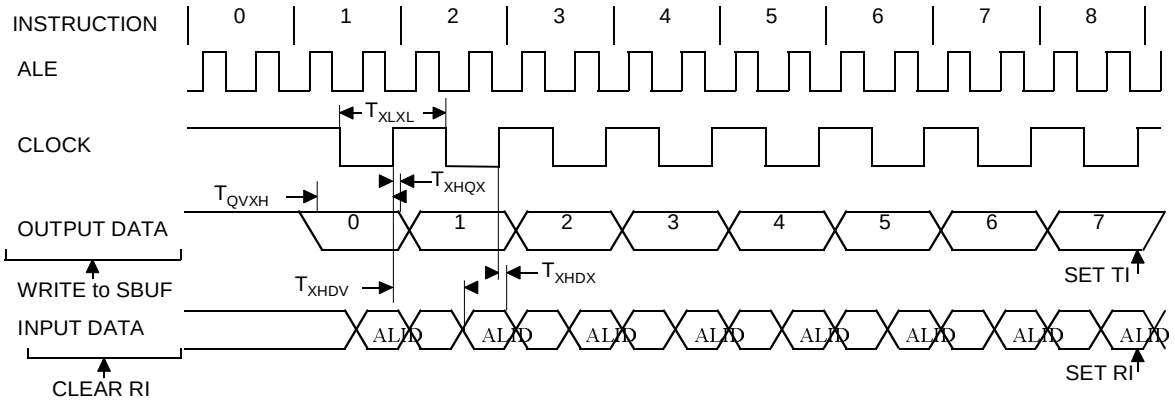
| Speed | -M 40 MHz | | -V X2 mode 30 MHz 60 MHz equiv. | | -V standard mode 40 MHz | | -L X2 mode 20 MHz 40 MHz equiv. | | -L standard mode 30 MHz | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $T_{XLXL}$ | 300 | | 200 | | 300 | | 300 | | 400 | | ns |
| $T_{QVHX}$ | 200 | | 117 | | 200 | | 200 | | 283 | | ns |
| $T_{XHQX}$ | 30 | | 13 | | 30 | | 30 | | 47 | | ns |
| $T_{XHDX}$ | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $T_{XHDV}$ | | 117 | | 34 | | 117 | | 117 | | 200 | ns |

**Table 19-13.** AC Parameters for a Variable Clock: derating formula

| Symbol | Type | Standard Clock | X2 Clock | -M | -V | -L | Units |
|---|---|---|---|---|---|---|---|
| $T_{XLXL}$ | Min | 12 T | 6 T | | | | ns |
| $T_{QVHX}$ | Min | 10 T - x | 5 T - x | 50 | 50 | 50 | ns |
| $T_{XHQX}$ | Min | 2 T - x | T - x | 20 | 20 | 20 | ns |
| $T_{XHDX}$ | Min | x | x | 0 | 0 | 0 | ns |
| $T_{XHDV}$ | Max | 10 T - x | 5 T- x | 133 | 133 | 133 | ns |

### 19.5.8 Shift Register Timing Waveforms

**Figure 19-9.** Shift Register Timing Waveforms



| Part Number | Supply Voltage | Temperature Range | Package | Packing |
|---|---|---|---|---|
| TS80C58X2xxx-MCA | -5 to +/-10% | Commercial | PDIL40 | Stick |
| TS80C58X2xxx-MCB | -5 to +/-10% | Commercial | PLCC44 | Stick |
| TS80C58X2xxx-MCC | -5 to +/-10% | Commercial | PQFP44 | Tray |
| TS80C58X2xxx-MCE | -5 to +/-10% | Commercial | VQFP44 | Tray |
| TS80C58X2xxx-VCA | -5 to +/-10% | Commercial | PDIL40 | Stick |
| TS80C58X2xxx-VCB | -5 to +/-10% | Commercial | PLCC44 | Stick |
| TS80C58X2xxx-VCC | -5 to +/-10% | Commercial | PQFP44 | Tray |
| TS80C58X2xxx-VCE | -5 to +/-10% | Commercial | VQFP44 | Tray |
| TS80C58X2xxx-LCA | -5 to +/-10% | Commercial | PDIL40 | Stick |
| TS80C58X2xxx-LCB | -5 to +/-10% | Commercial | PLCC44 | Stick |
| TS80C58X2xxx-LCC | -5 to +/-10% | Commercial | PQFP44 | Tray |
| TS80C58X2xxx-LCE | -5 to +/-10% | Commercial | VQFP44 | Tray |
| TS80C58X2xxx-MIA | -5 to +/-10% | Industrial | PDIL40 | Stick |
| TS80C58X2xxx-MIB | -5 to +/-10% | Industrial | PLCC44 | Stick |
| TS80C58X2xxx-MIC | -5 to +/-10% | Industrial | PQFP44 | Tray |
| TS80C58X2xxx-MIE | -5 to +/-10% | Industrial | VQFP44 | Tray |
| TS80C58X2xxx-VIA | -5 to +/-10% | Industrial | PDIL40 | Stick |
| TS80C58X2xxx-VIB | -5 to +/-10% | Industrial | PLCC44 | Stick |
| TS80C58X2xxx-VIC | -5 to +/-10% | Industrial | PQFP44 | Tray |
| TS80C58X2xxx-VIE | -5 to +/-10% | Industrial | VQFP44 | Tray |
| TS80C58X2xxx-LIA | -5 to +/-10% | Industrial | PDIL40 | Stick |
| TS80C58X2xxx-LIB | -5 to +/-10% | Industrial | PLCC44 | Stick |
| TS80C58X2xxx-LIC | -5 to +/-10% | Industrial | PQFP44 | Tray |
| TS80C58X2xxx-LIE | -5 to +/-10% | Industrial | VQFP44 | Tray |
| | | | | |
| AT80C58X2zzz-3CSUM | -5 to +/-10% | Industrial & Green | PDIL40 | Stick |
| AT80C58X2zzz-SLSUM | -5 to +/-10% | Industrial & Green | PLCC44 | Stick |
| AT80C58X2zzz-RLTUM | -5 to +/-10% | Industrial & Green | VQFP44 | Tray |
| AT80C58X2zzz-3CSUL | -5 to +/-10% | Industrial & Green | PDIL40 | Stick |
| AT80C58X2zzz-SLSUL | -5 to +/-10% | Industrial & Green | PLCC44 | Stick |
| AT80C58X2zzz-RLTUL | -5 to +/-10% | Industrial & Green | VQFP44 | Tray |
| AT80C58X2zzz-3CSUV | -5 to +/-10% | Industrial & Green | PDIL40 | Stick |
| AT80C58X2zzz-SLSUV | -5 to +/-10% | Industrial & Green | PLCC44 | Stick |
| AT80C58X2zzz-RLTUV | -5 to +/-10% | Industrial & Green | VQFP44 | Tray |
| | | | | |
| TS87C58X2-MCA | 5V ±10% | Commercial | PDIL40 | Stick |
| TS87C58X2-MCB | 5V ±10% | Commercial | PLCC44 | Stick |
| TS87C58X2-MCC | 5V ±10% | Commercial | PQFP44 | Tray |

| Part Number | Supply Voltage | Temperature Range | Package | Packing |
|---|---|---|---|---|
| TS87C58X2-MCE | 5V ±10% | Commercial | VQFP44 | Tray |
| TS87C58X2-VCA | 5V ±10% | Commercial | PDIL40 | Stick |
| TS87C58X2-VCB | 5V ±10% | Commercial | PLCC44 | Stick |
| TS87C58X2-VCC | 5V ±10% | Commercial | PQFP44 | Tray |
| TS87C58X2-VCE | 5V ±10% | Commercial | VQFP44 | Tray |
| TS87C58X2-LCA | 2.7 to 5.5V | Commercial | PDIL40 | Stick |
| TS87C58X2-LCB | 2.7 to 5.5V | Commercial | PLCC44 | Stick |
| TS87C58X2-LCC | 2.7 to 5.5V | Commercial | PQFP44 | Tray |
| TS87C58X2-LCE | 2.7 to 5.5V | Commercial | VQFP44 | Tray |
| TS87C58X2-MIA | 5V ±10% | Industrial | PDIL40 | Stick |
| TS87C58X2-MIB | 5V ±10% | Industrial | PLCC44 | Stick |
| TS87C58X2-MIC | 5V ±10% | Industrial | PQFP44 | Tray |
| TS87C58X2-MIE | 5V ±10% | Industrial | VQFP44 | Tray |
| TS87C58X2-VIA | 5V ±10% | Industrial | PDIL40 | Stick |
| TS87C58X2-VIB | 5V ±10% | Industrial | PLCC44 | Stick |
| TS87C58X2-VIC | 5V ±10% | Industrial | PQFP44 | Tray |
| TS87C58X2-VIE | 5V ±10% | Industrial | VQFP44 | Tray |
| TS87C58X2-LIA | 2.7 to 5.5V | Industrial | PDIL40 | Stick |
| TS87C58X2-LIB | 2.7 to 5.5V | Industrial | PLCC44 | Stick |
| TS87C58X2-LIC | 2.7 to 5.5V | Industrial | PQFP44 | Tray |
| TS87C58X2-LIE | 2.7 to 5.5V | Industrial | VQFP44 | Tray |
| | | | | |
| AT87C58X2-3CSUM | 5V ±10% | Industrial & Green | PDIL40 | Stick |
| AT87C58X2-SLSUM | 5V ±10% | Industrial & Green | PLCC44 | Stick |
| AT87C58X2-RLTUM | 5V ±10% | Industrial & Green | VQFP44 | Tray |
| AT87C58X2-3CSUL | 2.7 to 5.5V | Industrial & Green | PDIL40 | Stick |
| AT87C58X2-SLSUL | 2.7 to 5.5V | Industrial & Green | PLCC44 | Stick |
| AT87C58X2-RLTUL | 2.7 to 5.5V | Industrial & Green | VQFP44 | Tray |
| AT87C58X2-3CSUV | 5V ±10% | Industrial & Green | PDIL40 | Stick |
| AT87C58X2-SLSUV | 5V ±10% | Industrial & Green | PLCC44 | Stick |
| AT87C58X2-RLTUV | 5V ±10% | Industrial & Green | VQFP44 | Tray |

# 21. Datasheet Revision History

## 21.1 Changes from Rev. C 01/01 to Rev. D 11/05

1. Added green product Ordering Information.

## 21.2 Changes from Rev. D 11/05 to Rev. E 04/06

1. Changed value of AUXR register.