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Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40/30MHz
Connectivity	UART/USART
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-PQFP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts87c58x2-vic

4. SFR Mapping

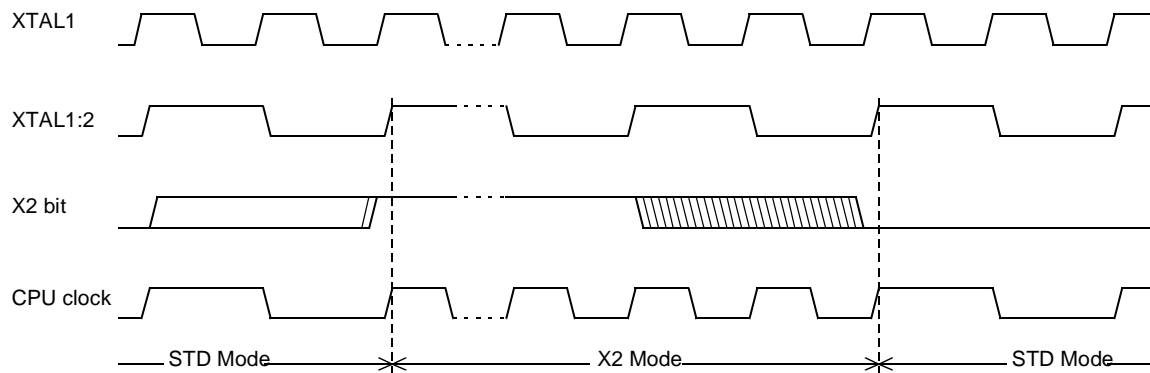
The Special Function Registers (SFRs) of the TS80C54/58X2 fall into the following categories:

- C51 core registers: ACC, B, DPH, DPL, PSW, SP, AUXR1
- I/O port registers: P0, P1, P2, P3
- Timer registers: T2CON, T2MOD, TCON, TH0, TH1, TH2, TMOD, TL0, TL1, TL2, RCAP2L, RCAP2H
- Serial I/O port registers: SADDR, SADEN, SBUF, SCON
- Power and clock control registers: PCON
- HDW Watchdog Timer Reset: WDTRST, WDTPRG
- Interrupt system registers: IE, IP, IPH
- Others: AUXR, CKCON

Table 5-1. Pin Description for 40/44 pin packages

MNEMONIC	PIN NUMBER			TYPE	Name And Function
	DIL	LCC	VQFP 1.4		
MNEMONIC	PIN NUMBER			TYPE	NAME AND FUNCTION
ALE/ $\overline{\text{PROG}}$	30	33	27	O (I)	Address Latch Enable/Program Pulse: Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (1/3 in X2 mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input ($\overline{\text{PROG}}$) during EPROM programming. ALE can be disabled by setting SFR's AUXR.0 bit. With this bit set, ALE will be inactive during internal fetches.
PSEN	29	32	26	O	Program Store ENable: The read strobe to external program memory. When executing code from the external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory.
$\overline{\text{EA}}/\text{V}_{\text{PP}}$	31	35	29	I	External Access Enable/Programming Supply Voltage: $\overline{\text{EA}}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H and 3FFFFH (54X2) or 7FFFFH (58X2). If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 3FFFFH (54X2) or 7FFFFH (58X2). This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming. If security level 1 is programmed, $\overline{\text{EA}}$ will be internally latched on Reset.
XTAL1	19	21	15	I	Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	Crystal 2: Output from the inverting oscillator amplifier

Figure 6-2. Mode Switching Waveforms



The X2 bit in the CKCON register (See Table 6-1.) allows to switch from 12 clock cycles per instruction to 6 clock cycles and vice versa. At reset, the standard speed is activated (STD mode). Setting this bit activates the X2 feature (X2 mode).

CAUTION

In order to prevent any incorrect operation while operating in X2 mode, user must be aware that all peripherals using clock frequency as time reference (UART, timers) will have their time reference divided by two. For example a free running timer generating an interrupt every 20 ms will then generate an interrupt every 10 ms. UART with 4800 baud rate will have 9600 baud rate.

7.1 Application

Software can take advantage of the additional data pointers to both increase speed and reduce code size, for example, block operations (copy, compare, search ...) are well served by using one data pointer as a 'source' pointer and the other one as a "destination" pointer.

ASSEMBLY LANGUAGE

```

; Block move using dual data pointers
; Destroys DPTR0, DPTR1, A and PSW
; note: DPS exits opposite of entry state
; unless an extra INC AUXR1 is added
;
00A2          AUXR1 EQU 0A2H
;
0000 909000   MOV  DPTR,#SOURCE      ; address of SOURCE
0003 05A2     INC   AUXR1             ; switch data pointers
0005 90A000   MOV  DPTR,#DEST        ; address of DEST
0008          LOOP:
0008 05A2     INC   AUXR1             ; switch data pointers
000A E0       MOVX A,@DPTR           ; get a byte from SOURCE
000B A3       INC   DPTR             ; increment SOURCE address
000C 05A2     INC   AUXR1            ; switch data pointers
000E F0       MOVX @DPTR,A           ; write the byte to DEST
000F A3       INC   DPTR             ; increment DEST address
0010 70F6     JNZ   LOOP             ; check for 0 terminator
0012 05A2     INC   AUXR1            ; (optional) restore DPS

```

INC is a short (2 bytes) and fast (12 clocks) way to manipulate the DPS bit in the AUXR1 SFR. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry. Observe that without the last instruction (INC AUXR1), the routine will exit with DPS in the opposite state.

- Enter a 16-bit initial value in timer registers TH2/TL2. It can be the same as the reload value or a different one depending on the application.
- To start the timer, set TR2 run control bit in T2CON register.

It is possible to use timer 2 as a baud rate generator and a clock generator simultaneously. For this configuration, the baud rates and clock frequencies are not independent since both functions use the values in the RCAP2H and RCAP2L registers.

Figure 8-2. Clock-Out Mode $C/\overline{T2} = 0$

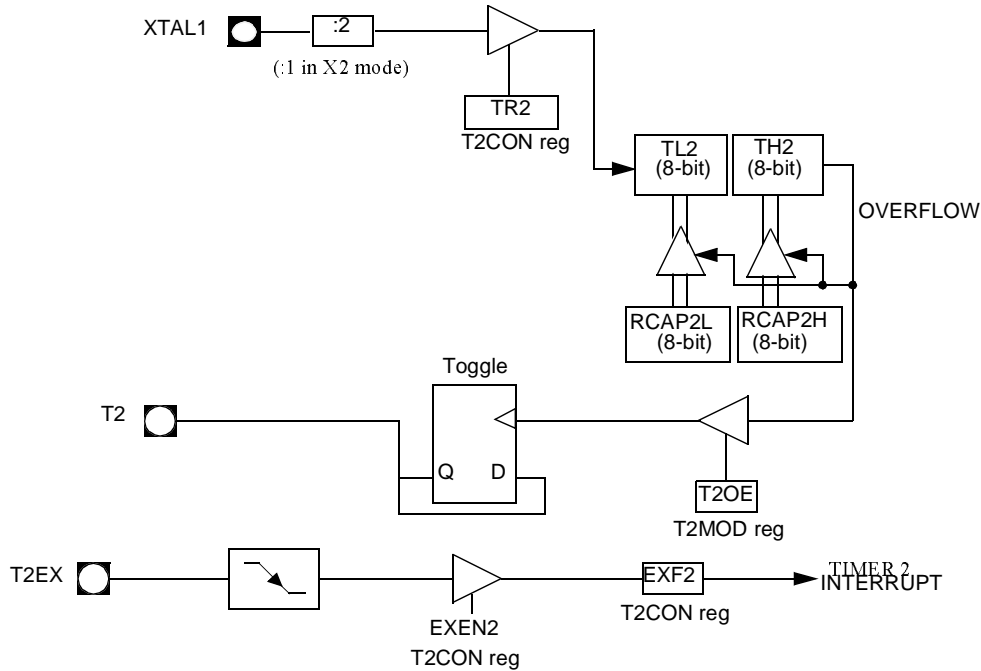


Table 8-1. T2CON Register
T2CON - Timer 2 Control Register (C8h)

7	6	5	4	3	2	1	0
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#
Bit Number	Bit Mnemonic	Description					
7	TF2	Timer 2 overflow Flag Must be cleared by software. Set by hardware on timer 2 overflow, if RCLK = 0 and TCLK = 0.					
6	EXF2	Timer 2 External Flag Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. When set, causes the CPU to vector to timer 2 interrupt routine when timer 2 interrupt is enabled. Must be cleared by software. EXF2 doesn't cause an interrupt in Up/down counter mode (DCEN = 1)					
5	RCLK	Receive Clock bit Clear to use timer 1 overflow as receive clock for serial port in mode 1 or 3. Set to use timer 2 overflow as receive clock for serial port in mode 1 or 3.					
4	TCLK	Transmit Clock bit Clear to use timer 1 overflow as transmit clock for serial port in mode 1 or 3. Set to use timer 2 overflow as transmit clock for serial port in mode 1 or 3.					
3	EXEN2	Timer 2 External Enable bit Clear to ignore events on T2EX pin for timer 2 operation. Set to cause a capture or reload when a negative transition on T2EX pin is detected, if timer 2 is not used to clock the serial port.					
2	TR2	Timer 2 Run control bit Clear to turn off timer 2. Set to turn on timer 2.					
1	C/T2#	Timer/Counter 2 select bit Clear for timer operation (input from internal clock system: F _{OSC}). Set for counter operation (input from T2 input pin, falling edge trigger). Must be 0 for clock out mode.					
0	CP/RL2#	Timer 2 Capture/Reload bit If RCLK=1 or TCLK=1, CP/RL2# is ignored and timer is forced to auto-reload on timer 2 overflow. Clear to auto-reload on timer 2 overflows or negative transitions on T2EX pin if EXEN2=1. Set to capture on negative transitions on T2EX pin if EXEN2=1.					

Reset Value = 0000 0000b

Bit addressable

The following is an example of how to use given addresses to address different slaves:

Slave A:	SADDR	1111 0001b
	<u>SADEN</u>	<u>1111 1010b</u>
	Given	1111 0X0Xb
Slave B:	SADDR	1111 0011b
	<u>SADEN</u>	<u>1111 1001b</u>
	Given	1111 0XX1b
Slave C:	SADDR	1111 0010b
	<u>SADEN</u>	<u>1111 1101b</u>
	Given	1111 00X1b

The SADEN byte is selected so that each slave may be addressed separately.

For slave A, bit 0 (the LSB) is a don't-care bit; for slaves B and C, bit 0 is a 1. To communicate with slave A only, the master must send an address where bit 0 is clear (e.g. 1111 0000b).

For slave A, bit 1 is a 1; for slaves B and C, bit 1 is a don't care bit. To communicate with slaves B and C, but not slave A, the master must send an address with bits 0 and 1 both set (e.g. 1111 0011b).

To communicate with slaves A, B and C, the master must send an address with bit 0 set, bit 1 clear, and bit 2 clear (e.g. 1111 0001b).

9.1.3 Broadcast Address

A broadcast address is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't-care bits, e.g.:

	SADDR	0101 0110b
	SADEN	1111 1100b
Broadcast =SADDR OR SADEN		1111 111Xb

The use of don't-care bits provides flexibility in defining the broadcast address, however in most applications, a broadcast address is FFh. The following is an example of using broadcast addresses:

Slave A:	SADDR	1111 0001b
	<u>SADEN</u>	<u>1111 1010b</u>
	Broadcast	1111 1X11b,
Slave B:	SADDR	1111 0011b
	<u>SADEN</u>	<u>1111 1001b</u>
	Broadcast	1111 1X11b,
Slave C:	SADDR=	1111 0010b
	<u>SADEN</u>	<u>1111 1101b</u>
	Broadcast	1111 1111b

For slaves A and B, bit 2 is a don't care bit; for slave C, bit 2 is set. To communicate with all of the slaves, the master must send an address FFh. To communicate with slaves A and B, but not slave C, the master can send an address FBh.

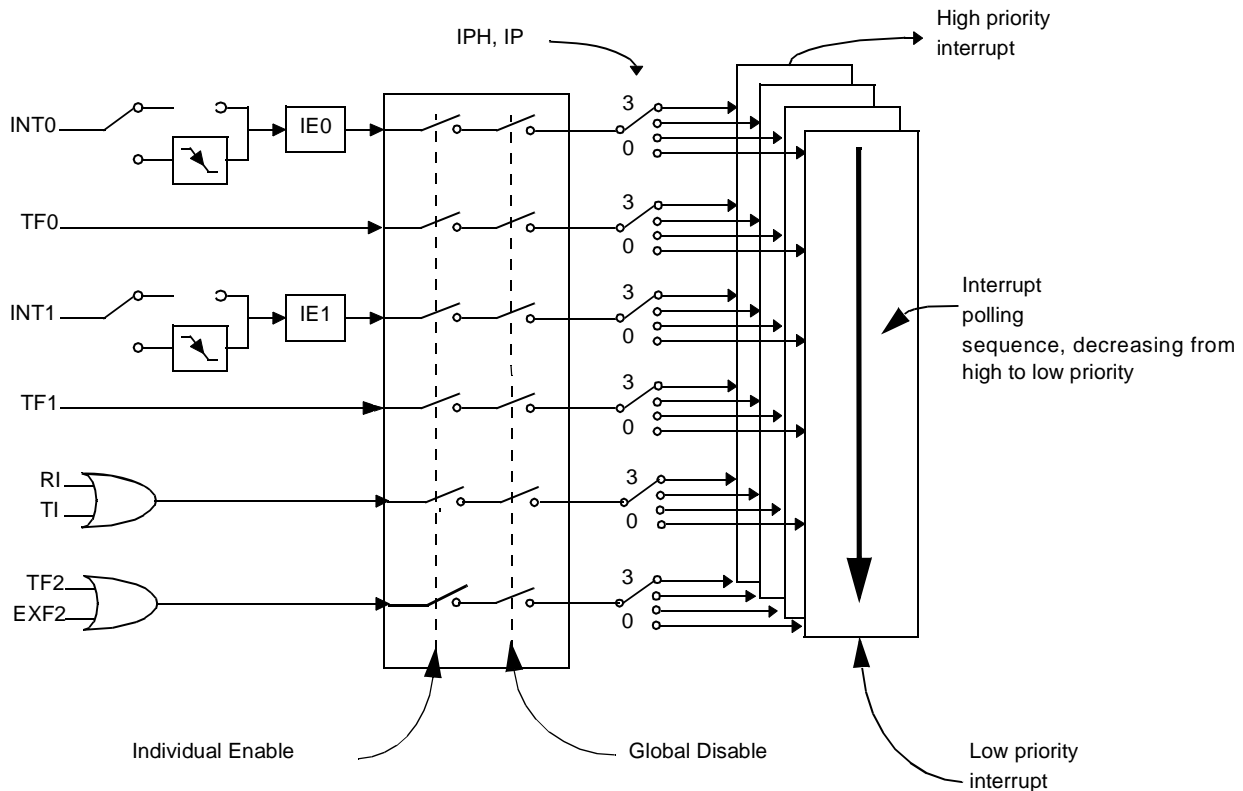
9.1.4 Reset Addresses

On reset, the SADDR and SADEN registers are initialized to 00h, i.e. the given and broadcast addresses are XXXX XXXXb (all don't-care bits). This ensures that the serial port will reply to any address, and so, that it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition.

10. Interrupt System

The TS80C54/58X2 has a total of 7 interrupt vectors: two external interrupts ($\overline{\text{INT0}}$ and $\overline{\text{INT1}}$), three timer interrupts (timers 0, 1 and 2) and the serial port interrupt. These interrupts are shown in Figure 10-1.

Figure 10-1. Interrupt Control System



Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (See Table 10-2.). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one out of four priority levels by setting or clearing a bit in the Interrupt Priority register (See Table 10-3.) and in the Interrupt Priority High register (See Table 10-4.). shows the bit values and priority levels associated with each combination.

Table 10-1. Priority Level Bit Values

IPH.x	IP.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

Table 10-3. IP Register
IP - Interrupt Priority Register (B8h)

7	6	5	4	3	2	1	0
-	-	PT2	PS	PT1	PX1	PT0	PX0

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	PT2	Timer 2 overflow interrupt Priority bit Refer to PT2H for priority level.
4	PS	Serial port Priority bit Refer to PSH for priority level.
3	PT1	Timer 1 overflow interrupt Priority bit Refer to PT1H for priority level.
2	PX1	External interrupt 1 Priority bit Refer to PX1H for priority level.
1	PT0	Timer 0 overflow interrupt Priority bit Refer to PT0H for priority level.
0	PX0	External interrupt 0 Priority bit Refer to PX0H for priority level.

Reset Value = XX00 0000b

Bit addressable

11. Idle mode

An instruction that sets PCON.0 causes that to be the last instruction executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer, and Serial Port functions. The CPU status is preserved in its entirety : the Stack Pointer, Program Counter, Program Status Word, Accumulator and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels.

There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bits GF0 and GF1 can be used to give an indication if an interrupt occurred during normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

11.1 Power-Down Mode

To save maximum power, a power-down mode can be invoked by software (Refer to Table 9-4., PCON register).

In power-down mode, the oscillator is stopped and the instruction that invoked power-down mode is the last instruction executed. The internal RAM and SFRs retain their value until the power-down mode is terminated. V_{CC} can be lowered to save further power. Either a hardware reset or an external interrupt can cause an exit from power-down. To properly terminate power-down, the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.

Only external interrupts $\overline{INT0}$ and $\overline{INT1}$ are useful to exit from power-down. For that, interrupt must be enabled and configured as level or edge sensitive interrupt input.

Holding the pin low restarts the oscillator but bringing the pin high completes the exit as detailed in Figure 11-1. When both interrupts are enabled, the oscillator restarts as soon as one of the two inputs is held low and power down exit will be completed when the first input will be released. In this case the higher priority interrupt service routine is executed.

Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put TS80C54/58X2 into power-down mode.

12. Hardware Watchdog Timer

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upset. The WDT consists of a 14-bit counter and the WatchDog Timer ReSeT (WDTRST) SFR. The WDT is by default disabled from exiting reset. To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, it will increment every machine cycle while the oscillator is running and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST-pin.

12.1 Using the WDT

To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, the user needs to service it by writing to 01EH and 0E1H to WDTRST to avoid WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH) and this will reset the device. When WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycle. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST-pin. The RESET pulse duration is $96 \times T_{OSC}$, where $T_{OSC} = 1/F_{OSC}$. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

To have a more powerful WDT, a 2^7 counter has been added to extend the Time-out capability, ranking from 16ms to 2s @ $F_{OSC} = 12\text{MHz}$. To manage this feature, refer to WDTPRG register description, Table 12-2. (SFR0A7h).

Table 12-1. WDTRST Register
WDTRST Address (0A6h)

	7	6	5	4	3	2	1
Reset value	X	X	X	X	X	X	X

Write only, this SFR is used to reset/enable the WDT by writing 01EH then 0E1H in sequence.

Table 12-2. WDTPRG Register
WDTPRG Address (0A7h)

7	6	5	4	3	2	1	0
T4	T3	T2	T1	T0	S2	S1	S0

Bit Number	Bit Mnemonic	Description																											
7	T4	Reserved Do not try to set or clear this bit.																											
6	T3																												
5	T2																												
4	T1																												
3	T0																												
2	S2	WDT Time-out select bit 2																											
1	S1	WDT Time-out select bit 1																											
0	S0	WDT Time-out select bit 0																											
		<table> <tr> <th>S2S1</th><th>S0</th><th>Selected Time-out</th></tr> <tr> <td>0</td><td>0</td><td>$(2^{14} - 1)$ machine cycles, 16.3 ms @ 12 MHz</td></tr> <tr> <td>0</td><td>0</td><td>$(2^{15} - 1)$ machine cycles, 32.7 ms @ 12 MHz</td></tr> <tr> <td>0</td><td>1</td><td>$(2^{16} - 1)$ machine cycles, 65.5 ms @ 12 MHz</td></tr> <tr> <td>0</td><td>1</td><td>$(2^{17} - 1)$ machine cycles, 131 ms @ 12 MHz</td></tr> <tr> <td>1</td><td>0</td><td>$(2^{18} - 1)$ machine cycles, 262 ms @ 12 MHz</td></tr> <tr> <td>1</td><td>0</td><td>$(2^{19} - 1)$ machine cycles, 542 ms @ 12 MHz</td></tr> <tr> <td>1</td><td>1</td><td>$(2^{20} - 1)$ machine cycles, 1.05 s @ 12 MHz</td></tr> <tr> <td>1</td><td>1</td><td>$(2^{21} - 1)$ machine cycles, 2.09 s @ 12 MHz</td></tr> </table>	S2S1	S0	Selected Time-out	0	0	$(2^{14} - 1)$ machine cycles, 16.3 ms @ 12 MHz	0	0	$(2^{15} - 1)$ machine cycles, 32.7 ms @ 12 MHz	0	1	$(2^{16} - 1)$ machine cycles, 65.5 ms @ 12 MHz	0	1	$(2^{17} - 1)$ machine cycles, 131 ms @ 12 MHz	1	0	$(2^{18} - 1)$ machine cycles, 262 ms @ 12 MHz	1	0	$(2^{19} - 1)$ machine cycles, 542 ms @ 12 MHz	1	1	$(2^{20} - 1)$ machine cycles, 1.05 s @ 12 MHz	1	1	$(2^{21} - 1)$ machine cycles, 2.09 s @ 12 MHz
S2S1	S0	Selected Time-out																											
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1	0	$(2^{19} - 1)$ machine cycles, 542 ms @ 12 MHz																											
1	1	$(2^{20} - 1)$ machine cycles, 1.05 s @ 12 MHz																											
1	1	$(2^{21} - 1)$ machine cycles, 2.09 s @ 12 MHz																											

Reset value XXXX X000

12.1.1 WDT during Power Down and Idle

In Power Down mode the oscillator stops, which means the WDT also stops. While in Power Down mode the user does not need to service the WDT. There are 2 methods of exiting Power Down mode: by a hardware reset or via a level activated external interrupt which is enabled prior to entering Power Down mode. When Power Down is exited with hardware reset, servicing the WDT should occur as it normally should whenever the TS80C54/58X2 is reset. Exiting Power Down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service routine.

To ensure that the WDT does not overflow within a few states of exiting of powerdown, it is best to reset the WDT just before entering powerdown.

In the Idle mode, the oscillator continues to run. To prevent the WDT from resetting the TS80C54/58X2 while in Idle mode, the user should always set up a timer that will periodically exit Idle, service the WDT, and re-enter Idle mode.

14. Power-Off Flag

The power-off flag allows the user to distinguish between a “cold start” reset and a “warm start” reset.

A cold start reset is the one induced by V_{CC} switch-on. A warm start reset occurs while V_{CC} is still applied to the device and could be generated for example by an exit from power-down.

The power-off flag (POF) is located in PCON register (See Table 14-1.). POF is set by hardware when V_{CC} rises from 0 to its nominal voltage. The POF can be set or cleared by software allowing the user to determine the type of reset.

The POF value is only relevant with a V_{CC} range from 4.5V to 5.5V. For lower V_{CC} value, reading POF bit will return indeterminate value.

Table 14-1. PCON Register
PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL

Bit Number	Bit Mnemonic	Description
7	SMOD1	Serial port Mode bit 1 Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	Serial port Mode bit 0 Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	POF	Power-Off Flag Clear to recognize next reset type. Set by hardware when V_{CC} rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	Power-Down mode bit Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	Idle mode bit Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b

Not bit addressable

15. Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0. As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

Table 15-1. AUXR Register
AUXR - Auxiliary Register (8Eh)

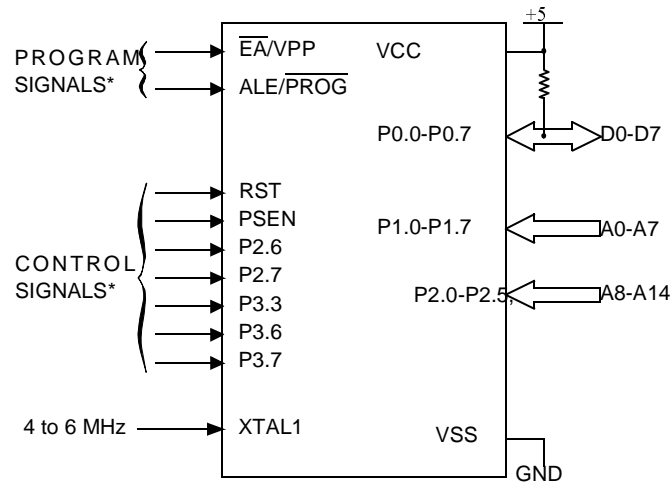
7	6	5	4	3	2	1	0
-	-	-	-	-	-	RESERVED	AO

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
3	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
1	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
0	AO	ALE Output bit Clear to restore ALE operation during internal fetches. Set to disable ALE operation during internal fetches.

Reset Value = XXXX XXX0b

Not bit addressable

Figure 17-1. Set-Up Modes Configuration



* See Table 31. for proper value on these inputs

17.3.3 Programming Algorithm

The Improved Quick Pulse algorithm is based on the Quick Pulse algorithm and decreases the number of pulses applied during byte programming from 25 to 1.

To program the TS80C54/58X2 the following sequence must be exercised:

- Step 1: Activate the combination of control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Input the appropriate data on the data lines.
- Step 4: Raise \overline{EA}/VPP from VCC to VPP (typical 12.75V).
- Step 5: Pulse ALE/\overline{PROG} once.
- Step 6: Lower \overline{EA}/VPP from VPP to VCC

Repeat step 2 through 6 changing the address and data for the entire array or until the end of the object file is reached (See Figure 17-2.).

17.3.4 Verify algorithm

Code array verify must be done after each byte or block of bytes is programmed. In either case, a complete verify of the programmed array will ensure reliable programming of the TS87C54/58X2.

P 2.7 is used to enable data output.

To verify the TS87C54/58X2 code the following sequence must be exercised:

- Step 1: Activate the combination of program and control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Read data on the data lines.

Repeat step 2 through 3 changing the address for the entire array verification (See Figure 17-2.)

Table 18-1. Signature Bytes Content

Location	Contents	Comment
30h	58h	Manufacturer Code: Atmel Wireless & Microcontrollers
31h	57h	Family Code: C51 X2
60h	37h	Product name: TS80C58X2
60h	B7h	Product name: TS87C58X2
60h	3Bh	Product name: TS80C54X2
60h	BBh	Product name: TS87C54X2
61h	FFh	Product revision number

19.5 AC Parameters

19.5.1 Explanation of the AC Symbols

Each timing symbol has 5 characters. The first character is always a “T” (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example: T_{AVLL} = Time for Address Valid to ALE Low.

T_{LLPL} = Time for ALE Low to PSEN Low.

$T_A = 0$ to $+70^{\circ}\text{C}$ (commercial temperature range); $V_{SS} = 0\text{ V}$; $V_{CC} = 5\text{ V} \pm 10\%$; -M and -V ranges.
 $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (industrial temperature range); $V_{SS} = 0\text{ V}$; $V_{CC} = 5\text{ V} \pm 10\%$; -M and -V ranges.

$T_A = 0$ to $+70^{\circ}\text{C}$ (commercial temperature range); $V_{SS} = 0\text{ V}$; $2.7\text{ V} < V_{CC} < 5.5\text{ V}$; -L range.

$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (industrial temperature range); $V_{SS} = 0\text{ V}$; $2.7\text{ V} < V_{CC} < 5.5\text{ V}$; -L range.

Table 19-3. gives the maximum applicable load capacitance for Port 0, Port 1, 2 and 3, and ALE and PSEN signals. Timings will be guaranteed if these capacitances are respected. Higher capacitance values can be used, but timings will then be degraded.

Table 19-3. Load Capacitance versus speed range, in pF

	-M	-V	-L
Port 0	100	50	100
Port 1, 2, 3	80	50	80
ALE / $\overline{\text{PSEN}}$	100	30	100

Table 19-5., Table 19-8. and Table 19-11. give the description of each AC symbols.

Table 19-6., Table 19-9. and Table 19-12. give for each range the AC parameter.

Table 19-7., Table 19-10. and Table 19-13. give the frequency derating formula of the AC parameter. To calculate each AC symbols, take the x value corresponding to the speed grade you need (-M, -V or -L) and replace this value in the formula. Values of the frequency must be limited to the corresponding speed grade:

Table 19-4. Max frequency for derating formula regarding the speed grade

	-M X1 mode	-M X2 mode	-V X1 mode	-V X2 mode	-L X1 mode	-L X2 mode
Freq (MHz)	40	20	40	30	30	20
T (ns)	25	50	25	33.3	33.3	50

Example:

T_{LLIV} in X2 mode for a -V part at 20 MHz ($T = 1/20^{\text{E}6} = 50\text{ ns}$):

$x = 22$ (Table 19-7.)

$T = 50\text{ ns}$

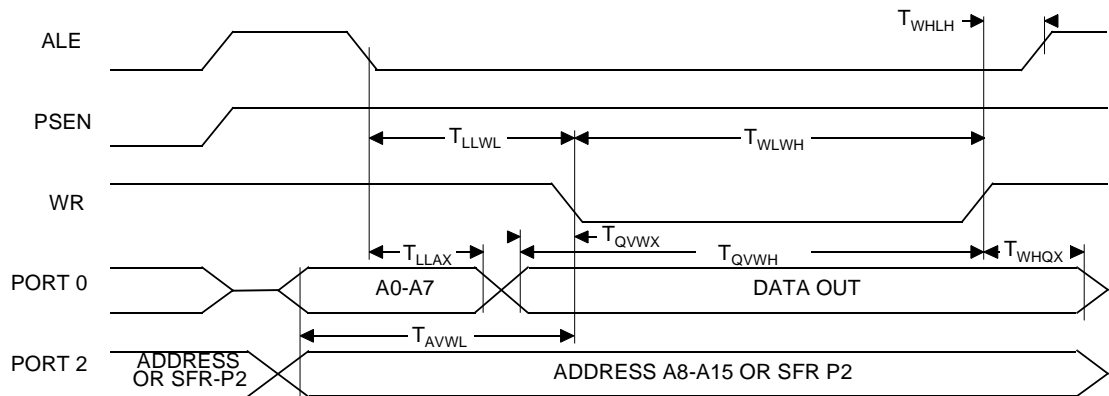
$T_{LLIV} = 2T - x = 2 \times 50 - 22 = 78\text{ ns}$

Table 19-10. AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
T_{RLRH}	Min	$6 T - x$	$3 T - x$	20	15	25	ns
T_{WLWH}	Min	$6 T - x$	$3 T - x$	20	15	25	ns
T_{RLDV}	Max	$5 T - x$	$2.5 T - x$	25	23	30	ns
T_{RHDZ}	Max	$2 T - x$	$T - x$	20	15	25	ns
T_{LLDV}	Max	$8 T - x$	$4 T - x$	40	35	45	ns
T_{AVDV}	Max	$9 T - x$	$4.5 T - x$	60	50	65	ns
T_{LLWL}	Min	$3 T - x$	$1.5 T - x$	25	20	30	ns
T_{LLWL}	Max	$3 T + x$	$1.5 T + x$	25	20	30	ns
T_{AVWL}	Min	$4 T - x$	$2 T - x$	25	20	30	ns
T_{QVWX}	Min	$T - x$	$0.5 T - x$	15	10	20	ns
T_{QVWH}	Min	$7 T - x$	$3.5 T - x$	15	10	20	ns
T_{WHQX}	Min	$T - x$	$0.5 T - x$	10	8	15	ns
T_{RLAZ}	Max	x	x	0	0	0	ns
T_{WHLH}	Min	$T - x$	$0.5 T - x$	15	10	20	ns
T_{WHLH}	Max	$T + x$	$0.5 T + x$	15	10	20	ns

19.5.5 External Data Memory Write Cycle

Figure 19-7. External Data Memory Write Cycle



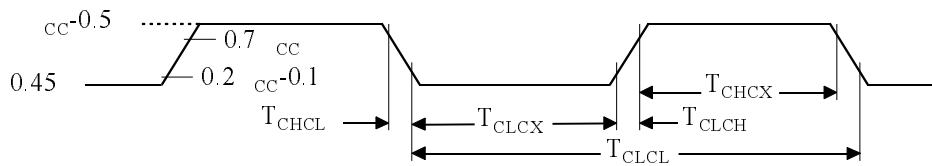
19.5.11 External Clock Drive Characteristics (XTAL1)

Table 19-15. AC Parameters

Symbol	Parameter	Min	Max	Units
T_{CLCL}	Oscillator Period	25		ns
T_{CHCX}	High Time	5		ns
T_{CLCX}	Low Time	5		ns
T_{CLCH}	Rise Time		5	ns
T_{CHCL}	Fall Time		5	ns
T_{CHCX}/T_{CLCX}	Cyclic ratio in X2 mode	40	60	%

19.5.12 External Clock Drive Waveforms

Figure 19-11. External Clock Drive Waveforms





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