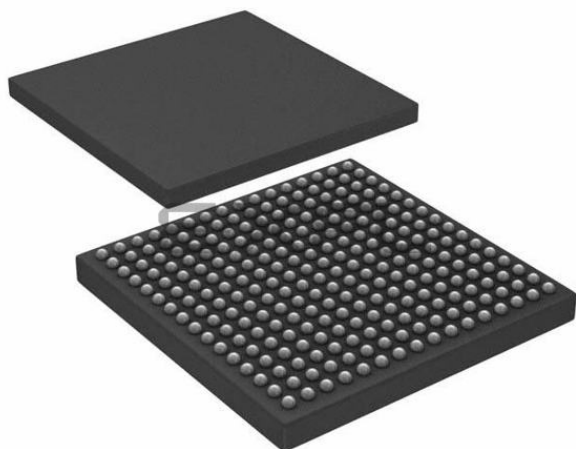




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	6060
Total RAM Bits	719872
Number of I/O	161
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LFBGA
Supplier Device Package	256-FPBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2gl005-1vf256



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Table 4 • Recommended Operating Conditions (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
3.3 V DC supply voltage	V_{DDIX}	3.15	3.3	3.45	V	
LVDS differential I/O	V_{DDIX}	2.375	2.5	3.45	V	
B-LVDS, M-LVDS, Mini-LVDS, RSDS differential I/O	V_{DDIX}	2.375	2.5	2.625	V	
LVPECL differential I/O	V_{DDIX}	3.15	3.3	3.45	V	
Reference voltage supply for FDDR (Bank0) and MDDR (Bank5)	V_{REFX}	$0.49 \times V_{DDIX}$	$0.5 \times V_{DDIX}$	$0.51 \times V_{DDIX}$	V	
Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to V_{PP} .	V_{PPNVM}	2.375	2.5	2.625	V	2.5 V range
		3.15	3.3	3.45	V	3.3 V range

1. Programming at Industrial temperature range is available only with $V_{PP} = 3.3$ V.

Note: Power supply ramps must all be strictly monotonic, without plateaus.

Table 5 • FPGA Operating Limits

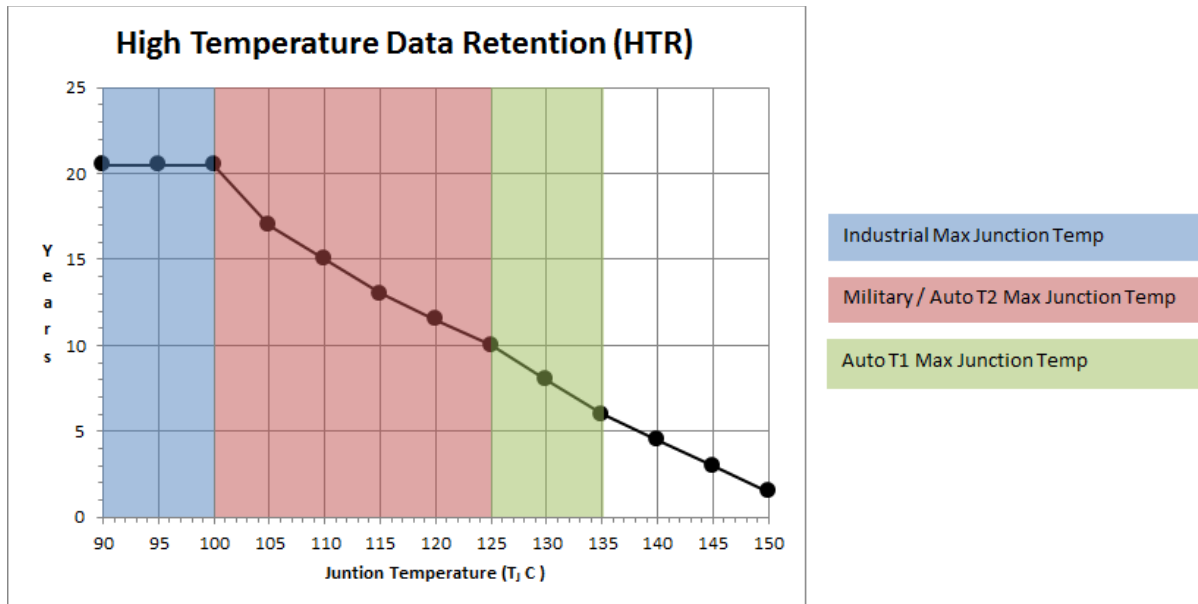
Product Grade	Element	Programming Temperature	Operating Temperature	Programming Cycles	Digest Temperature	Digest Cycles	Retention (Biased/Unbiased)
Commercial	FPGA	Min $T_J = 0$ °C Max $T_J = 85$ °C	Min $T_J = 0$ °C Max $T_J = 85$ °C	500	Min $T_J = 0$ °C Max $T_J = 85$ °C	2000	20 years
Industrial ¹	FPGA	Min $T_J = -40$ °C Max $T_J = 100$ °C	Min $T_J = -40$ °C Max $T_J = 100$ °C	500	Min $T_J = -40$ °C Max $T_J = 100$ °C	2000	20 years

1. Programming at Industrial temperature range is available only with $V_{PP} = 3.3$ V.

Note: The retention specification is defined as the total number of programing and digest cycles. For example, 20 years of retention after 500 programming cycles.

Note: The digest cycle specification is 2000 digest cycles for every program cycle with a maximum of 500 programming cycles.

Note: If your product qualification requires accelerated programming cycles, see [Microsemi SoC Products Quality and Reliability Report](#) about recommended methodologies.

Figure 1 • High Temperature Data Retention (HTR)

2.3.1.1 Overshoot/Undershoot Limits

For AC signals, the input signal may undershoot during transitions to -1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

For AC signals, the input signal may overshoot during transitions to $V_{CCI} + 1.0$ V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

Note: The above specifications do not apply to the PCI standard. The IGLOO2 and SmartFusion2 PCI I/Os are compliant with the PCI standard including the PCI overshoot/undershoot specifications.

2.3.1.2 Thermal Characteristics

The temperature variable in the Microsemi SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption causes the chip's junction temperature to be higher than the ambient, case, or board temperatures.

EQ1 through EQ3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P} \quad \text{EQ 1}$$

$$\theta_{JB} = \frac{T_J - T_B}{P} \quad \text{EQ 2}$$

$$\theta_{JC} = \frac{T_J - T_C}{P} \quad \text{EQ 3}$$

Table 9 • Package Thermal Resistance of SmartFusion2 and IGLOO2 Devices (continued)

	Still Air	1.0 m/s	2.5 m/s			
Device	θ_{JA}			θ_{JB}	θ_{JC}	Unit
150						
FC1152	9.08	6.81	5.87	2.56	0.38	°C/W
FCS536	15.01	12.06	10.76	3.69	1.55	°C/W
FCV484	16.21	13.11	11.84	6.73	0.10	°C/W

2.3.1.2.1 Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in the actual performance of the product. It must be used with caution, but it is useful for comparing the thermal performance of one package with another.

The maximum power dissipation allowed is calculated using EQ4.

$$\text{Maximum power allowed} = \frac{T_{J(\text{MAX})} - T_{A(\text{MAX})}}{\theta_{JA}}$$

EQ 4

The absolute maximum junction temperature is 100 °C. EQ5 shows a sample calculation of the absolute maximum power dissipation allowed for the M2GL050T-FG896 package at commercial temperature and in still air, where:

$$\theta_{JA} = 14.7 \text{ °C/W (taken from Table 9, page 10).}$$

$$T_A = 85 \text{ °C}$$

$$\text{Maximum power allowed} = \frac{100 \text{ °C} - 85 \text{ °C}}{14.7 \text{ °C/W}} = 1.088 \text{ W}$$

EQ 5

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package.

If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink may be attached to the top of the case, or the airflow inside the system must be increased.

2.3.1.2.2 Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from the junction to the board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

2.3.1.2.3 Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable to packages used with external heat sinks. Constant temperature is applied to the surface, which acts as a boundary condition.

This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

2.3.1.3 ESD Performance

See *RT0001: Microsemi Corporation - SoC Products Reliability Report* for information about ESD.

2.3.5 User I/O Characteristics

There are three types of I/Os supported in the IGLOO2 FPGA and SmartFusion2 SoC FPGA families: MSIO, MSIOD, and DDRIO I/O banks. The I/O standards supported by the different I/O banks is described in the I/Os section of the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.

2.3.5.1 Input Buffer and AC Loading

The following figure shows the input buffer and AC loading.

Figure 3 • Input Buffer AC Loading

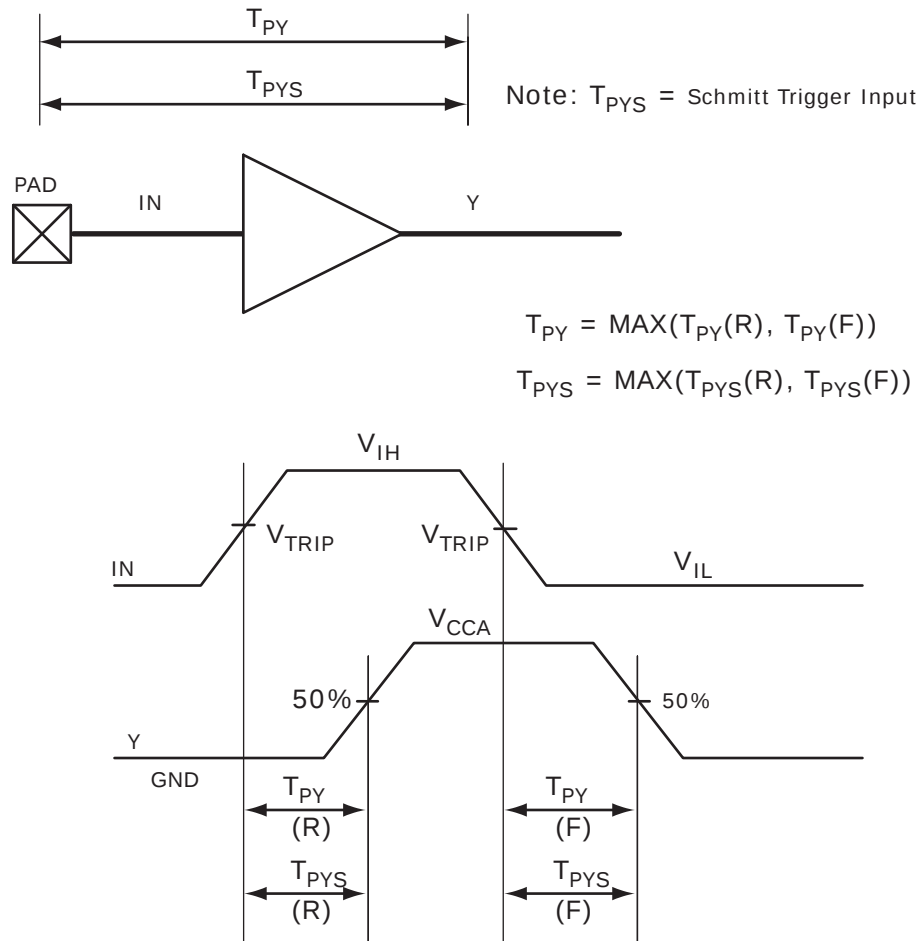


Table 48 • LVCMOS 2.5 V Transmitter Characteristics for MSIOD Bank (Output and Tristate Buffers)

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}^1		T_{LZ}^1		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	2.206	2.596	2.678	3.15	2.64	3.106	4.935	5.805	4.74	5.576	ns
4 mA	Slow	1.835	2.159	2.242	2.637	2.256	2.654	5.413	6.368	5.15	6.059	ns
6 mA	Slow	1.709	2.01	2.132	2.508	2.167	2.549	5.813	6.838	5.499	6.469	ns
8 mA	Slow	1.63	1.918	1.958	2.303	2.012	2.367	6.226	7.324	5.816	6.842	ns
12 mA	Slow	1.648	1.939	1.86	2.187	1.921	2.259	6.519	7.669	6.027	7.09	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

2.3.5.8 1.8 V LVCMOS

LVCMOS 1.8 is a general standard for 1.8 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-7A.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 49 • LVCMOS 1.8 V DC Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
LVCMOS 1.8 V DC Recommended Operating Conditions					
Supply voltage	V_{DDI}	1.710	1.8	1.89	V

Table 50 • LVCMOS 1.8 V DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC input logic high (for MSIOD and DDRIO I/O banks)	$V_{IH} (DC)$	$0.65 \times V_{DDI}$	1.89	V
DC input logic high (for MSIO I/O bank)	$V_{IH} (DC)$	$0.65 \times V_{DDI}$	3.45	V
DC input logic low	$V_{IL} (DC)$	-0.3	$0.35 \times V_{DDI}$	V
Input current high ¹	$I_{IH} (DC)$			–
Input current low ¹	$I_{IL} (DC)$			–

1. See Table 24, page 22.

Table 51 • LVCMOS 1.8 V DC Output Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC output logic high	V_{OH}	$V_{DDI} - 0.45$		V
DC output logic low	V_{OL}		0.45	V

Table 52 • LVCMOS 1.8 V Minimum and Maximum AC Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank) ¹	D_{MAX}	400	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIO I/O bank)	D_{MAX}	295	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIOD I/O bank) ¹	D_{MAX}	400	Mbps	AC loading: 17 pF load, maximum drive/slew

1. Maximum Data Rate applies for Drive Strength 8 mA and above, All Slews.

Table 62 • LVCMOS 1.5 V DC Output Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC output logic high	VOH	$V_{DDI} \times 0.75$		V
DC output logic low	VOL		$V_{DDI} \times 0.25$	V

Table 63 • LVCMOS 1.5 V AC Minimum and Maximum Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	D _{MAX}	235	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIO I/O bank)	D _{MAX}	160	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIOD I/O bank)	D _{MAX}	220	Mbps	AC loading: 17 pF load, maximum drive/slew

Table 64 • LVCMOS 1.5 V AC Calibrated Impedance Option

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	RODT_CA L	75, 60, 50, 40	Ω

Table 65 • LVCMOS 1.5 V AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point	V _{TRIP}	0.75	V
Resistance for enable path (T _{ZH} , T _{ZL} , T _{HZ} , T _{LZ})	R _{ENT}	2K	Ω
Capacitive loading for enable path (T _{ZH} , T _{ZL} , T _{HZ} , T _{LZ})	C _{ENT}	5	pF
Capacitive loading for data path (T _{DP})	C _{LOAD}	5	pF

Table 66 • LVCMOS 1.5 V Transmitter Drive Strength Specifications

Output Drive Selection			V _{OH} (V)	V _{OL} (V)	IOH (at V _{OH}) mA	IOL (at V _{OL}) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min	Max		
2 mA	2 mA	2 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	2	2
4 mA	4 mA	4 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	4	4
6 mA	6 mA	6 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	6	6
8 mA		8 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	8	8
		10 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	10	10
		12 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	12	12

Note: For a detailed I/V curve, use the corresponding IBIS models:

www.microsemi.com/soc/download/ibis/default.aspx.

Table 95 • HSTL DC Output Voltage Specification Applicable to DDRIO I/O Bank Only

Parameter	Symbol	Min	Max	Unit
HSTL Class I				
DC output logic high	V_{OH}	$V_{DDI} - 0.4$		V
DC output logic low	V_{OL}		0.4	V
Output minimum source DC current (MSIO and DDRIO I/O banks)	I_{OH} at V_{OH}	-8.0		mA
Output minimum sink current (MSIO and DDRIO I/O banks)	I_{OL} at V_{OL}	8.0		mA
HSTL Class II				
DC output logic high	V_{OH}	$V_{DDI} - 0.4$		V
DC output logic low	V_{OL}		0.4	V
Output minimum source DC current	I_{OH} at V_{OH}	-16.0		mA
Output minimum sink current	I_{OL} at V_{OL}	16.0		mA

Table 96 • HSTL DC Differential Voltage Specification

Parameter	Symbol	Min	Unit
DC input differential voltage	V_{ID} (DC)	0.2	V

Table 97 • HSTL AC Differential Voltage Specifications

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	V_{DIFF}	0.4		V
AC differential cross point voltage	V_x	0.68	0.9	V

Table 98 • HSTL Minimum and Maximum AC Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	D_{MAX}	400	Mbps	AC loading: per JEDEC specifications

Table 99 • HSTL Impedance Specification

Parameter	Symbol	Typ	Unit	Conditions
Supported output driver calibrated impedance (for DDRIO I/O bank)	R_{REF}	25.5, 47.8	Ω	Reference resistance = 191 Ω
Effective impedance value (ODT for DDRIO I/O bank only)	R_{TT}	47.8	Ω	Reference resistance = 191 Ω

Table 112 • SSTL2 Receiver Characteristics for MSIO I/O Bank (Input Buffers)

		T_{PY}		Unit
	On-Die Termination (ODT)	-1	-Std	
Pseudo differential	None	2.798	3.293	ns
True differential	None	2.733	3.215	ns

Table 113 • DDR1/SSTL2 Receiver Characteristics for MSIOD I/O Bank (Input Buffers)

		T_{PY}		Unit
	On-Die Termination (ODT)	-1	-Std	
Pseudo differential	None	2.476	2.913	ns
True differential	None	2.475	2.911	ns

Table 114 • SSTL2 Class I Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
Single-ended	2.26	2.66	1.99	2.341	1.985	2.335	2.135	2.512	2.13	2.505	ns
Differential	2.26	2.658	2.202	2.591	2.201	2.589	2.393	2.815	2.392	2.814	ns

Table 115 • DDR1/SSTL2 Class I Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
Single-ended	2.055	2.417	2.037	2.396	2.03	2.388	2.068	2.433	2.061	2.425	ns
Differential	2.192	2.58	2.434	2.864	2.425	2.852	2.164	2.545	2.156	2.536	ns

Table 116 • DDR1/SSTL2 Class I Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
Single-ended	1.512	1.779	1.462	1.72	1.462	1.72	1.676	1.972	1.676	1.971	ns
Differential	1.676	1.971	1.774	2.087	1.766	2.077	1.854	2.181	1.845	2.171	ns

Table 117 • DDR1/SSTL2 Class II Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
Single-ended	2.122	2.497	1.906	2.243	1.902	2.237	2.061	2.424	2.056	2.418	ns
Differential	2.127	2.501	2.042	2.402	2.043	2.403	2.363	2.78	2.365	2.781	ns

Table 159 • LPDDR-LVCMOS 1.8 V AC Switching Characteristics for Transmitter for DDRIO I/O Bank (Output and Tristate Buffers) (continued)

10 mA	medium	3.246	3.819	2.686	3.16	3.236	3.807	5.542	6.52	4.936	5.807	ns
	medium_fast	3.066	3.607	2.525	2.971	3.054	3.593	5.405	6.359	4.811	5.66	ns
	fast	3.046	3.584	2.513	2.957	3.034	3.57	5.401	6.353	4.803	5.651	ns
	slow	3.498	4.115	2.878	3.386	3.481	4.096	6.046	7.113	5.444	6.404	ns
12 mA	medium	3.138	3.692	2.569	3.023	3.126	3.678	5.782	6.803	5.129	6.034	ns
	medium_fast	2.966	3.489	2.414	2.841	2.951	3.472	5.666	6.665	5.013	5.897	ns
	fast	2.945	3.464	2.401	2.826	2.93	3.448	5.659	6.658	5.003	5.886	ns
	slow	3.417	4.02	2.807	3.303	3.401	4.002	6.083	7.156	5.464	6.428	ns
16 mA	medium	3.076	3.618	2.519	2.964	3.063	3.604	5.828	6.856	5.176	6.089	ns
	medium_fast	2.913	3.427	2.376	2.795	2.898	3.41	5.725	6.736	5.072	5.966	ns
	fast	2.894	3.405	2.362	2.78	2.879	3.388	5.715	6.724	5.064	5.957	ns
	slow	3.366	3.96	2.751	3.237	3.348	3.939	6.226	7.324	5.576	6.56	ns
	medium	3.03	3.565	2.47	2.906	3.017	3.55	5.981	7.036	5.282	6.214	ns
	medium_fast	2.87	3.377	2.328	2.739	2.854	3.358	5.895	6.935	5.18	6.094	ns
	fast	2.853	3.357	2.314	2.723	2.837	3.338	5.889	6.929	5.177	6.09	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management).

2.3.7 Differential I/O Standards

Configuration of the I/O modules as a differential pair is handled by Microsemi SoC Products Group Libero software when the user instantiates a differential I/O macro in the design. Differential I/Os can also be used in conjunction with the embedded Input register (InReg), Output register (OutReg), Enable register (EnReg), and Double Data Rate registers (DDR).

2.3.7.1 LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard.

Minimum and Maximum Input and Output Levels

Table 160 • LVDS Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	V_{DDI}	2.375	2.5	2.625	V	2.5 V range
Supply voltage	V_{DDI}	3.15	3.3	3.45	V	3.3 V range

Table 161 • LVDS DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit	Conditions
DC Input voltage	V_I	0	2.925	V	2.5 V range
DC input voltage	V_I	0	3.45	V	3.3 V range
Input current high ¹	I_{IH} (DC)				
Input current low ¹	I_{IL} (DC)				

1. See Table 24, page 22.

Table 162 • LVDS DC Output Voltage Specification

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V_{OH}	1.25	1.425	1.6	V
DC output logic low	V_{OL}	0.9	1.075	1.25	V

Table 163 • LVDS DC Differential Voltage Specification

Parameter	Symbol	Min	Typ	Max	Unit
Differential output voltage swing	V_{OD}	250	350	450	mV
Output common mode voltage	V_{OCM}	1.125	1.25	1.375	V
Input common mode voltage	V_{ICM}	0.05	1.25	2.35	V
Input differential voltage	V_{ID}	100	350	600	mV

Table 164 • LVDS Minimum and Maximum AC Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	D_{MAX}	535	Mbps	AC loading: 12 pF / 100 Ω differential load
Maximum data rate (for MSIOD I/O bank) no pre-emphasis	D_{MAX}	620	Mbps	AC loading: 10 pF / 100 Ω differential load
		700	Mbps	AC loading: 2 pF / 100 Ω differential load

Table 165 • LVDS AC Impedance Specifications

Parameter	Symbol	Typ	Max	Unit
Termination resistance	R_T	100		Ω

Table 166 • LVDS AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	Cross point	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF

LVDS25 AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

Table 167 • LVDS25 Receiver Characteristics for MSIO I/O Bank (Input Buffers)

On-Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.774	3.263	ns
100	2.775	3.264	ns

Table 185 • M-LVDS DC Voltage Specification Output Voltage Specification (for MSIO I/O Bank Only)

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V_{OH}	1.25	1.425	1.6	V
DC output logic low	V_{OL}	0.9	1.075	1.25	V

Table 186 • M-LVDS Differential Voltage Specification

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing (for MSIO I/O bank only)	V_{OD}	300	650	mV
Output common mode voltage (for MSIO I/O bank only)	V_{OCM}	0.3	2.1	V
Input common mode voltage	V_{ICM}	0.3	1.2	V
Input differential voltage	V_{ID}	50	2400	mV

Table 187 • M-LVDS Minimum and Maximum AC Switching Speed for MSIO I/O Bank

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	D_{MAX}	500	Mbps	AC loading: 2 pF / 100 Ω differential load

Table 188 • M-LVDS AC Impedance Specifications

Parameter	Symbol	Typ	Unit
Termination resistance	R_T	50	Ω

Table 189 • M-LVDS AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	Cross point	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

Table 190 • M-LVDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)

On-Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.738	3.221	ns
100	2.735	3.218	ns

2.3.11 Global Resource Characteristics

The IGLOO2 and SmartFusion2 SoC FPGA devices offer a powerful, low skew global routing network which provides an effective clock distribution throughout the FPGA fabric. See [UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide](#) for the positions of various global routing resources.

The following table lists the 150 device global resources in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 225 • 150 Device Global Resource

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	T_{RCKL}	0.83	0.911	0.831	0.913	ns
Input high delay for global clock	T_{RCKH}	1.457	1.588	1.715	1.869	ns
Maximum skew for global clock	T_{RCKSW}		0.131		0.154	ns

The following table lists the 090 device global resources in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 226 • 090 Device Global Resource

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	T_{RCKL}	0.835	0.888	0.833	0.886	ns
Input high delay for global clock	T_{RCKH}	1.405	1.489	1.654	1.752	ns
Maximum skew for global clock	T_{RCKSW}		0.084		0.098	ns

The following table lists the 050 device global resources in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 227 • 050 Device Global Resource

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	T_{RCKL}	0.827	0.897	0.826	0.896	ns
Input high delay for global clock	T_{RCKH}	1.419	1.53	1.671	1.8	ns
Maximum skew for global clock	T_{RCKSW}		0.111		0.129	ns

The following table lists the 025 device global resources in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 228 • 025 Device Global Resource

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	T_{RCKL}	0.747	0.799	0.745	0.797	ns
Input high delay for global clock	T_{RCKH}	1.294	1.378	1.522	1.621	ns
Maximum skew for global clock	T_{RCKSW}		0.084		0.099	ns

Table 242 • μ SRAM (RAM512x2) in 512 × 2 Mode (continued)

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.101		0.118		ns
Write input data hold time	T_{DINCHD}	0.137		0.161		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.247		0.29		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	–0.03		–0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

The following table lists the μ SRAM in 1024 × 1 mode in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 243 • μ SRAM (RAM1024x1) in 1024 × 1 Mode

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.27		0.31	ns
Read access time without pipeline register			1.78		2.1	ns
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode		1.978		2.327		ns
Read address hold time in synchronous mode	T_{ADDRHD}	0.137		0.161		ns
Read address hold time in asynchronous mode		–0.6		–0.71		ns
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	–0.65		–0.77		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.16		2.54	ns
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	–0.02		–0.03		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns

Table 276 • Cryptographic Block Characteristics (continued)

Service	Conditions	Timing	Unit
SHA256	512 bits	540	kbps
	1024 bits	780	kbps
	2048 bits	950	kbps
	24 kbits	1140	kbps
HMAC	512 bytes	820	kbps
	1024 bytes	890	kbps
	2048 bytes	930	kbps
	24 kbytes	980	kbps
KeyTree		1.8	ms
Challenge-response	PUF = OFF	25	ms
	PUF = ON	7	ms
ECC point multiplication		590	ms
ECC point addition		8	ms

1. Using cypher block chaining (CBC) mode.

2.3.19 Crystal Oscillator

The following table describes the electrical characteristics of the crystal oscillator in the IGLOO2 FPGA and SmartFusion2 SoC FPGAs.

Table 277 • Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Operating frequency	FXTAL		20		MHz	
Accuracy	ACCXTAL			0.0047	%	005, 010, 025, 050, 060, and 090 devices
				0.0058	%	150 devices
Output duty cycle	CYCXTAL		49–51	47–53	%	
Output period jitter (peak to peak)	JITPERXTAL		200	300	ps	
Output cycle to cycle jitter (peak to peak)	JITCYCXTAL		200	300	ps	010, 025, 050, and 060 devices
			250	410	ps	150 devices
			250	550	ps	005 and 090 devices
Operating current	IDYNXTAL		1.5		mA	010, 050, and 060 devices
			1.65		mA	005, 025, 090, and 150 devices
Input logic level high	VIHXTAL	0.9 V _{PP}			V	
Input logic level low	VILXTAL			0.1 V _{PP}	V	

2.3.22 JTAG

Table 284 • JTAG 1532 for 005, 010, 025, and 050 Devices

Parameter	Symbol	005		010		025		050		Unit
		–1	–Std	–1	–Std	–1	–Std	–1	–Std	
Clock to Q (data out)	T_{TCK2Q}	7.47	8.79	7.73	9.09	7.75	9.12	7.89	9.28	ns
Reset to Q (data out)	T_{RSTB2Q}	7.65	9	6.43	7.56	6.13	7.21	7.40	8.70	ns
Test data input setup time	T_{DISU}	–1.05	–0.89	–0.69	–0.59	–0.67	–0.57	–0.30	–0.25	ns
Test data input hold time	T_{DIHD}	2.38	2.8	2.38	2.8	2.42	2.85	2.09	2.45	ns
Test mode select setup time	T_{TMSSU}	–0.73	–0.62	–1.03	–1.21	–1.1	–0.94	0.28	0.33	ns
Test mode select hold time	T_{TMDHD}	1.36	1.6	1.43	1.68	1.93	2.27	0.16	0.19	ns
ResetB removal time	$T_{TRSTREM}$	–0.77	–0.65	–1.08	–0.92	–1.33	–1.13	–0.45	–0.38	ns
ResetB recovery time	$T_{TRSTREC}$	–0.76	–0.65	–1.07	–0.91	–1.34	–1.14	–0.45	–0.38	ns
TCK maximum frequency	F_{TCKMAX}	25	21.25	25	21.25	25	21.25	25.00	21.25	MHz

Table 285 • JTAG 1532 for 060, 090, and 150 Devices

Parameter	Symbol	060		090		150		Unit
		–1	–Std	–1	–Std	–1	–Std	
Clock to Q (data out)	T_{TCK2Q}	8.38	9.86	8.96	10.54	8.66	10.19	ns
Reset to Q (data out)	T_{RSTB2Q}	8.54	10.04	7.75	9.12	8.79	10.34	ns
Test data input setup time	T_{DISU}	–1.18	–1	–1.31	–1.11	–0.96	–0.82	ns
Test data input hold time	T_{DIHD}	2.52	2.97	2.68	3.15	2.57	3.02	ns
Test mode select setup time	T_{TMSSU}	–0.97	–0.83	–1.02	–0.87	–0.53	–0.45	ns
Test mode select hold time	T_{TMDHD}	1.7	2	1.67	1.96	1.02	1.2	ns
ResetB removal time	$T_{TRSTREM}$	–1.21	–1.03	–0.76	–0.65	–1.03	–0.88	ns
ResetB recovery time	$T_{TRSTREC}$	–1.21	–1.03	–0.77	–0.65	–1.03	–0.88	ns
TCK maximum frequency	F_{TCKMAX}	25	21.25	25	21.25	25	21.25	MHz

2.3.23 System Controller SPI Characteristics

Table 305 • SPI Characteristics for All Devices (continued)

Symbol	Description	Min	Typ	Max	Unit	Conditions
sp5	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS fall time (10%– 90%) ¹		2.906		ns	IO Configuration: LVCMOS 2.5 V-8 mA AC Loading: 35 pF Test Conditions: Typical Voltage, 25 °C
SPI master configuration (applicable for 005, 010, 025, and 050 devices)						
sp6m	SPI_[0 1]_DO setup time ²	$(\text{SPI_x_CLK_period}/2) - 8.0$			ns	
sp7m	SPI_[0 1]_DO hold time ²	$(\text{SPI_x_CLK_period}/2) - 2.5$			ns	
sp8m	SPI_[0 1]_DI setup time ²	12			ns	
sp9m	SPI_[0 1]_DI hold time ²	2.5			ns	
SPI slave configuration (applicable for 005, 010, 025, and 050 devices)						
sp6s	SPI_[0 1]_DO setup time ²	$(\text{SPI_x_CLK_period}/2) - 17.0$			ns	
sp7s	SPI_[0 1]_DO hold time ²	$(\text{SPI_x_CLK_period}/2) + 3.0$			ns	
sp8s	SPI_[0 1]_DI setup time ²	2			ns	
sp9s	SPI_[0 1]_DI hold time ²	7			ns	
SPI master configuration (applicable for 060, 090, and 150 devices)						
sp6m	SPI_[0 1]_DO setup time ²	$(\text{SPI_x_CLK_period}/2) - 7.0$			ns	
sp7m	SPI_[0 1]_DO hold time ²	$(\text{SPI_x_CLK_period}/2) - 9.5$			ns	
sp8m	SPI_[0 1]_DI setup time ²	15			ns	
sp9m	SPI_[0 1]_DI hold time ²	-2.5			ns	
SPI slave configuration (applicable for 060, 090, and 150 devices)						
sp6s	SPI_[0 1]_DO setup time ²	$(\text{SPI_x_CLK_period}/2) - 16.0$			ns	
sp7s	SPI_[0 1]_DO hold time ²	$(\text{SPI_x_CLK_period}/2) - 3.5$			ns	
sp8s	SPI_[0 1]_DI setup time ²	3			ns	
sp9s	SPI_[0 1]_DI hold time ²	2.5			ns	

1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. For allowable pclk configurations, see Serial Peripheral Interface Controller section in the *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.

2.3.34 MMUART Characteristics

The following table lists the MMUART characteristics in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 308 • MMUART Characteristics

Parameter	Description	–1	–Std	Unit
FMMUART_REF_CLK	Internally sourced MMUART reference clock frequency.	166	142	MHz
BAUDMMUARTTx	Maximum transmit baud rate	10.375	8.875	Mbps
BAUDMMUARTRx	Maximum receive baud rate	10.375	8.875	Mbps

2.3.35 IGLOO2 Specifications

2.3.35.1 HPMS Clock Frequency

The following table lists the maximum frequency for HPMS main clock in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 309 • Maximum Frequency for HPMS Main Clock

Symbol	Description	–1	–Std	Unit
HPMS_CLK	Maximum frequency for the HPMS main clock	166	142	MHz

2.3.35.2 IGLOO2 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_0_CLK. For timing parameter definitions, see [Figure 23](#), page 131.

The following table lists the SPI characteristics in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 310 • SPI Characteristics for All Devices

Symbol	Description	Min	Typ	Max	Unit	Conditions
SPIFMAX	Maximum operating frequency of SPI interface			20	MHz	
sp1	SPI_[0 1]_CLK minimum period					
	SPI_[0 1]_CLK = PCLK/2	12			ns	
	SPI_[0 1]_CLK = PCLK/4	24.1			ns	
	SPI_[0 1]_CLK = PCLK/8	48.2			ns	
	SPI_[0 1]_CLK = PCLK/16	0.1			μs	
	SPI_[0 1]_CLK = PCLK/32	0.19			μs	
	SPI_[0 1]_CLK = PCLK/64	0.39			μs	
	SPI_[0 1]_CLK = PCLK/128	0.77			μs	