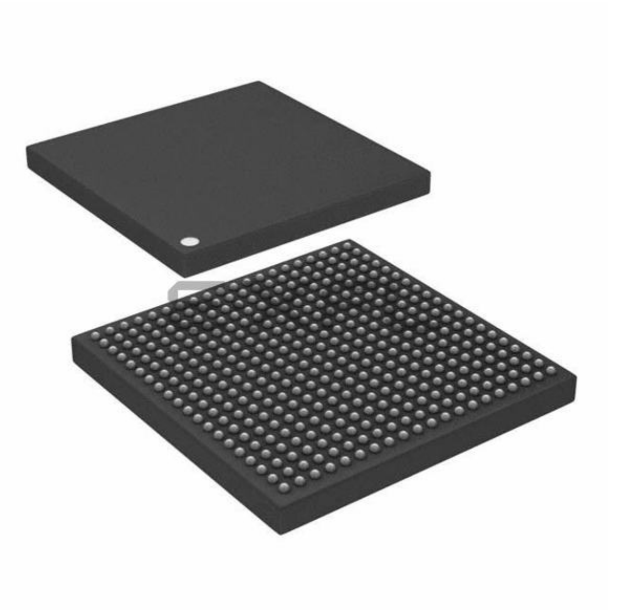
# Microchip Technology - M2GL005-VF400I Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 6060 |
| Total RAM Bits | 719872 |
| Number of I/O | 169 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 400-LFBGA |
| Supplier Device Package | 400-VFBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m2gl005-vf400i |

# Contents

1. For flash programming and retention maximum limits, see Table 5, page 7. For recommended operating conditions, see Table 4, page 6.

***Table 4 •*** **Recommended Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Operating junction temperature | $T_J$ | 0 | 25 | 85 | °C | Commercial |
| | | –40 | 25 | 100 | °C | Industrial |
| Programming junction temperatures[1] | $T_J$ | 0 | 25 | 85 | °C | Commercial |
| | | –40 | 25 | 100 | °C | Industrial |
| DC core supply voltage. Must always power this pin. | $V_{DD}$ | 1.14 | 1.2 | 1.26 | V | |
| Power supply for charge pumps (for normal operation and programming) for the 005, 010, 025, 050, 060 devices | $V_{PP}$ | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| | | 3.15 | 3.3 | 3.45 | V | 3.3 V range |
| Power supply for charge pumps (for normal operation and programming) for the 090 and 150 devices | $V_{PP}$ | 3.15 | 3.3 | 3.45 | V | 3.3 V range |
| Analog power pad for MDDR PLL | MSS_MDDR_PLL_VDDA | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| | | 3.15 | 3.3 | 3.45 | V | 3.3 V range |
| Analog power pad for MDDR PLL | HPMS_MDDR_PLL_VDDA | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| | | 3.15 | 3.3 | 3.45 | V | 3.3 V range |
| Analog power pad for FDDR PLL | FDDR_PLL_VDDA | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| | | 3.15 | 3.3 | 3.45 | V | 3.3 V range |
| Analog power pad for MDDR PLL | PLL0_PLL1_MSS_MDDR_VDDA | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| | | 3.15 | 3.3 | 3.45 | V | 3.3 V range |
| Analog power pad for MDDR PLL | PLL0_PLL1_HPMS_MDDR_VDDA | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| | | 3.15 | 3.3 | 3.45 | V | 3.3 V range |
| Analog power pad for PLL0 to PLL5 | CCC_XX[01]_PLL_VDDA | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| | | 3.15 | 3.3 | 3.45 | V | 3.3 V range |
| High supply voltage for PLL SerDes[01] | SERDES_[01]_PLL_VDDA | 2.375 | 2.5 | 2.625 | V | 2.5 V range |
| | | 3.15 | 3.3 | 3.45 | V | 3.3 V range |
| Analog power for SerDes[01] PLL Lane 0 to Lane 3. This is a 2.5 V SerDes internal PLL supply. | SERDES_[01]_L[0123]_VDDAPLL | 2.375 | 2.5 | 2.625 | V | |
| TX/RX analog I/O voltage. Low voltage power for the lanes of SerDesIF0. This is a 1.2 V SerDes PMA supply. | SERDES_[01]_L[0123]_VDDAIO | 1.14 | 1.2 | 1.26 | V | |
| PCIe/PCS power supply | SERDES_[01]_VDD | 1.14 | 1.2 | 1.26 | V | |
| 1.2 V DC supply voltage | $V_{DDIx}$ | 1.14 | 1.2 | 1.26 | V | |
| 1.5 V DC supply voltage | $V_{DDIx}$ | 1.425 | 1.5 | 1.575 | V | |
| 1.8 V DC supply voltage | $V_{DDIx}$ | 1.71 | 1.8 | 1.89 | V | |
| 2.5 V DC supply voltage | $V_{DDIx}$ | 2.375 | 2.5 | 2.625 | V | |

## 2.3.2 Power Consumption

The following sections describe the power consumptions of the devices.

### 2.3.2.1 Quiescent Supply Current

***Table 10 •*** **Quiescent Supply Current Characteristics**

| | **Modes and Configurations** | |
|---|---|---|
| **Power Supplies/Blocks** | **Non-Flash*Freeze** | **Flash*Freeze** |
| FPGA Core | On | Off |
| $V_{DD}$/SERDES_[01]_VDD[1] | On | On |
| $V_{PP}$/$V_{PPNVM}$ | On | On |
| HPMS_MDDR_PLL_VDDA/FDDR_PLL_VDDA/ CCC_XX[01]_PLL_VDDA/PLL0_PLL1_HPMS_MDDR_VDDA | 0 V | 0 V |
| SERDES_[01]_PLL_VDDA[2] | 0 V | 0 V |
| SERDES_[01]_L[0123]_VDDAPLL/VDD_2V5[2] | On | On |
| SERDES_[01]_L[0123]_VDDAIIO[2] | On | On |
| $V_{DDIx}$[3, 4] | On | On |
| $V_{REFx}$ | On | On |
| MSSDDR CLK | 32 kHz | 32 kHz |
| RAM | On | Sleep state |
| System controller | 50 MHz | 50 MHz |
| 50 MHz oscillator (enable/disable) | Enable | Disabled |
| 1 MHz oscillator (enable/disable) | Disabled | Disabled |
| Crystal oscillator (enable/disable) | Disabled | Disabled |

1. SERDES_[01]_VDD Power Supply is shorted to $V_{DD}$.
2. SerDes and DDR blocks to be unused.
3. $V_{DDIx}$ has been set to ON for test conditions as described. Banks on the east side should always be powered with the appropriate $V_{DDI}$ bank supplies. For details on bank power supplies, see “Recommendation for Unused Bank Supplies” table in the *AC393: SmartFusion2 and IGLOO2 Board Design Guidelines Application Note*.
4. No Differential (that is to say, LVDS) I/Os or ODT attributes to be used.

***Table 11 •*** **SmartFusion2 and IGLOO2 Quiescent Supply Current ($V_{DD}$ = 1.2 V) – Typical Process**

| **Symbol** | **Modes** | **005** | **010** | **025** | **050** | **060** | **090** | **150** | **Unit** | **Conditions** |
|---|---|---|---|---|---|---|---|---|---|---|
| IDC1 | Non-Flash*Freeze | 6.2 | 6.9 | 8.9 | 13.1 | 15.3 | 15.4 | 27.5 | mA | Typical ($T_J$ = 25 °C) |
| | | 24.0 | 28.4 | 40.6 | 67.8 | 80.6 | 81.4 | 144.7 | mA | Commercial ($T_J$ = 85 °C) |
| | | 35.2 | 41.9 | 60.5 | 102.1 | 121.4 | 122.6 | 219.1 | mA | Industrial ($T_J$ = 100 °C) |

**Table 43 • LVCMOS 2.5 V AC Test Parameter Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | 1.2 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ωσ |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | pF |

**Table 44 • LVCMOS 2.5 V Transmitter Drive Strength Specifications**

| Output Drive Selection | | | VOH (V) | VOL (V) | IOH (at VOH) mA | IOL (at VOL) mA |
|---|---|---|---|---|---|---|
| MSIO I/O Bank | MSIOD I/O Bank | DDRIO I/O Bank (With Software Default Fixed Code) | Min | Max | | |
| 2 mA | 2 mA | 2 mA | $V_{DDI} – 0.4$ | 0.4 | 2 | 2 |
| 4 mA | 4 mA | 4 mA | $V_{DDI} – 0.4$ | 0.4 | 4 | 4 |
| 6 mA | 6 mA | 6 mA | $V_{DDI} – 0.4$ | 0.4 | 6 | 6 |
| 8 mA | 8 mA | 8 mA | $V_{DDI} – 0.4$ | 0.4 | 8 | 8 |
| 12 mA | 12 mA | 12 mA | $V_{DDI} – 0.4$ | 0.4 | 12 | 12 |
| 16 mA | | 16 mA | $V_{DDI} – 0.4$ | 0.4 | 16 | 16 |

**Note:** For board design considerations, output slew rates extraction, detailed output buffer resistances, and I/V Curve, use the corresponding IBIS models located at: www.microsemi.com/soc/download/ibis/default.aspx.

### AC Switching Characteristics

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 2.375 V

**Table 45 • LVCMOS 2.5 V Receiver Characteristics (Input Buffers)**

| | On-Die Termination (ODT) | $T_{PY}$ | | $T_{PYS}$ | | |
|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | Unit |
| **LVCMOS 2.5 V (for DDRIO I/O bank)** | None | 1.823 | 2.145 | 1.932 | 2.274 | ns |
| **LVCMOS 2.5 V (for MSIO I/O bank)** | None | 2.486 | 2.925 | 2.495 | 2.935 | ns |
| **LVCMOS 2.5 V (for MSIOD I/O bank)** | None | 2.29 | 2.694 | 2.305 | 2.712 | ns |

**Table 46 • LVCMOS 2.5 V Transmitter Characteristics for DDRIO Bank (Output and Tristate Buffers)**

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| 2 mA | Slow | 3.657 | 4.302 | 3.393 | 3.991 | 3.675 | 4.323 | 3.894 | 4.582 | 3.552 | 4.18 | ns |
| | Medium | 3.374 | 3.97 | 3.139 | 3.693 | 3.396 | 3.995 | 3.635 | 4.277 | 3.253 | 3.828 | ns |
| | Medium fast | 3.239 | 3.811 | 3.036 | 3.572 | 3.261 | 3.836 | 3.519 | 4.141 | 3.128 | 3.681 | ns |
| | Fast | 3.224 | 3.793 | 3.029 | 3.563 | 3.246 | 3.818 | 3.512 | 4.132 | 3.119 | 3.67 | ns |

***Table 57 •*** **LVCMOS 1.8 V Transmitter Characteristics for DDRIO I/O Bank with Fixed Code (Output and Tristate Buffers)**

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | |
| 2 mA | Slow | 4.234 | 4.981 | 3.646 | 4.29 | 4.245 | 4.995 | 4.908 | 5.774 | 4.434 | 5.216 | ns |
| | Medium | 3.824 | 4.498 | 3.282 | 3.861 | 3.834 | 4.511 | 4.625 | 5.441 | 4.116 | 4.843 | ns |
| | Medium fast | 3.627 | 4.267 | 3.111 | 3.66 | 3.637 | 4.279 | 4.481 | 5.272 | 3.984 | 4.687 | ns |
| | Fast | 3.605 | 4.241 | 3.097 | 3.644 | 3.615 | 4.253 | 4.472 | 5.262 | 3.973 | 4.674 | ns |
| 4 mA | Slow | 3.923 | 4.615 | 3.314 | 3.9 | 3.918 | 4.61 | 5.403 | 6.356 | 4.894 | 5.757 | ns |
| | Medium | 3.518 | 4.138 | 2.961 | 3.484 | 3.515 | 4.135 | 5.121 | 6.025 | 4.561 | 5.366 | ns |
| | Medium fast | 3.321 | 3.907 | 2.783 | 3.275 | 3.317 | 3.903 | 4.966 | 5.843 | 4.426 | 5.206 | ns |
| | Fast | 3.301 | 3.883 | 2.77 | 3.259 | 3.296 | 3.878 | 4.957 | 5.831 | 4.417 | 5.196 | ns |
| 6 mA | Slow | 3.71 | 4.364 | 3.104 | 3.652 | 3.702 | 4.355 | 5.62 | 6.612 | 5.08 | 5.977 | ns |
| | Medium | 3.333 | 3.921 | 2.779 | 3.27 | 3.325 | 3.913 | 5.346 | 6.289 | 4.777 | 5.62 | ns |
| | Medium fast | 3.155 | 3.712 | 2.62 | 3.083 | 3.146 | 3.702 | 5.21 | 6.13 | 4.657 | 5.479 | ns |
| | Fast | 3.134 | 3.688 | 2.608 | 3.068 | 3.125 | 3.677 | 5.202 | 6.12 | 4.648 | 5.468 | ns |
| 8 mA | Slow | 3.619 | 4.258 | 3.007 | 3.538 | 3.607 | 4.244 | 5.815 | 6.841 | 5.249 | 6.175 | ns |
| | Medium | 3.246 | 3.819 | 2.686 | 3.16 | 3.236 | 3.807 | 5.542 | 6.52 | 4.936 | 5.807 | ns |
| | Medium fast | 3.066 | 3.607 | 2.525 | 2.971 | 3.054 | 3.593 | 5.405 | 6.359 | 4.811 | 5.66 | ns |
| | Fast | 3.046 | 3.584 | 2.513 | 2.957 | 3.034 | 3.57 | 5.401 | 6.353 | 4.803 | 5.651 | ns |
| 10 mA | Slow | 3.498 | 4.115 | 2.878 | 3.386 | 3.481 | 4.096 | 6.046 | 7.113 | 5.444 | 6.404 | ns |
| | Medium | 3.138 | 3.692 | 2.569 | 3.023 | 3.126 | 3.678 | 5.782 | 6.803 | 5.129 | 6.034 | ns |
| | Medium fast | 2.966 | 3.489 | 2.414 | 2.841 | 2.951 | 3.472 | 5.666 | 6.665 | 5.013 | 5.897 | ns |
| | Fast | 2.945 | 3.464 | 2.401 | 2.826 | 2.93 | 3.448 | 5.659 | 6.658 | 5.003 | 5.886 | ns |
| 12 mA | Slow | 3.417 | 4.02 | 2.807 | 3.303 | 3.401 | 4.002 | 6.083 | 7.156 | 5.464 | 6.428 | ns |
| | Medium | 3.076 | 3.618 | 2.519 | 2.964 | 3.063 | 3.604 | 5.828 | 6.856 | 5.176 | 6.089 | ns |
| | Medium fast | 2.913 | 3.427 | 2.376 | 2.795 | 2.898 | 3.41 | 5.725 | 6.736 | 5.072 | 5.966 | ns |
| | Fast | 2.894 | 3.405 | 2.362 | 2.78 | 2.879 | 3.388 | 5.715 | 6.724 | 5.064 | 5.957 | ns |
| 16 mA | Slow | 3.366 | 3.96 | 2.751 | 3.237 | 3.348 | 3.939 | 6.226 | 7.324 | 5.576 | 6.56 | ns |
| | Medium | 3.03 | 3.565 | 2.47 | 2.906 | 3.017 | 3.55 | 5.981 | 7.036 | 5.282 | 6.214 | ns |
| | Medium fast | 2.87 | 3.377 | 2.328 | 2.739 | 2.854 | 3.358 | 5.895 | 6.935 | 5.18 | 6.094 | ns |
| | Fast | 2.853 | 3.357 | 2.314 | 2.723 | 2.837 | 3.338 | 5.889 | 6.929 | 5.177 | 6.09 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

*Table 62 •* **LVCMOS 1.5 V DC Output Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC output logic high | VOH | $V_{DDI}$ × 0.75 | | V |
| DC output logic low | VOL | | $V_{DDI}$ × 0.25 | V |

*Table 63 •* **LVCMOS 1.5 V AC Minimum and Maximum Switching Speed**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for DDRIO I/O bank) | $D_{MAX}$ | 235 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 160 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIOD I/O bank) | $D_{MAX}$ | 220 | Mbps | AC loading: 17 pF load, maximum drive/slew |

*Table 64 •* **LVCMOS 1.5 V AC Calibrated Impedance Option**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | RODT_CAL | 75, 60, 50, 40 | Ω |

*Table 65 •* **LVCMOS 1.5 V AC Test Parameter Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point | $V_{TRIP}$ | 0.75 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | pF |

*Table 66 •* **LVCMOS 1.5 V Transmitter Drive Strength Specifications**

| Output Drive Selection | | | $V_{OH}$ (V) | $V_{OL}$ (V) | IOH (at $V_{OH}$) mA | IOL (at $V_{OL}$) mA |
|---|---|---|---|---|---|---|
| **MSIO I/O Bank** | **MSIOD I/O Bank** | **DDRIO I/O Bank** | **Min** | **Max** | | |
| 2 mA | 2 mA | 2 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 2 | 2 |
| 4 mA | 4 mA | 4 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 4 | 4 |
| 6 mA | 6 mA | 6 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 6 | 6 |
| 8 mA | | 8 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 8 | 8 |
| | | 10 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 10 | 10 |
| | | 12 mA | $V_{DDI}$ × 0.75 | $V_{DDI}$ × 0.25 | 12 | 12 |

**Note:** For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

*Table 144* • **LPDDR AC Differential Voltage Specifications (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| AC input differential voltage | $V_{DIFF}$ | 0.6 × $V_{DDI}$ | | V |
| AC differential cross point voltage | $V_x$ | 0.4 × $V_{DDI}$ | 0.6 × $V_{DDI}$ | V |

*Table 145* • **LPDDR AC Specifications (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate | $D_{MAX}$ | 400 | Mbps | AC loading: per JEDEC specifications |

*Table 146* • **LPDDR AC Calibrated Impedance Option (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Typ | Unit | Conditions |
|---|---|---|---|---|
| Supported output driver calibrated impedance | $R_{REF}$ | 20, 42 | Ω | Reference resistor = 150 Ω |
| Effective impedance value (ODT) | $R_{TT}$ | 50, 70, 150 | Ω | Reference resistor = 150 Ω |

*Table 147* • **LPDDR AC Test Parameter Specifications (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | 0.9 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Reference resistance for data test path for LPDDR ($T_{DP}$) | RTT_TEST | 50 | Ω |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | Ω |

### AC Switching Characteristics

Worst-case commercial conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, worst-case $V_{DDI}$.

*Table 148* • **LPDDR Receiver Characteristics for DDRIO I/O Bank with Fixed Codes**

| | | $T_{PY}$ | | |
|---|---|---|---|---|
| | **On-Die Termination (ODT)** | **–1** | **–Std** | **Unit** |
| Pseudo differential | None | 1.568 | 1.845 | ns |
| True differential | None | 1.588 | 1.869 | ns |

*Table 149* • **LPDDR Reduced Drive for DDRIO I/O Bank (Output and Tristate Buffers)**

| | $T_{DP}$ | | $T_{ENZL}$ | | $T_{ENZH}$ | | $T_{ENHZ}$ | | $T_{ENLZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| Single-ended | 2.383 | 2.804 | 2.23 | 2.623 | 2.229 | 2.622 | 2.202 | 2.591 | 2.201 | 2.59 | ns |
| Differential | 2.396 | 2.819 | 2.764 | 3.252 | 2.764 | 3.252 | 2.255 | 2.653 | 2.255 | 2.653 | ns |

***Table 150 •*** **LPDDR Full Drive for DDRIO I/O Bank (Output and Tristate Buffers)**

| | $T_{DP}$ | | $T_{ENZL}$ | | $T_{ENZH}$ | | $T_{ENHZ}$ | | $T_{ENLZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| Single-ended | 2.281 | 2.683 | 2.196 | 2.584 | 2.195 | 2.583 | 2.171 | 2.555 | 2.17 | 2.554 | ns |
| Differential | 2.298 | 2.703 | 2.288 | 2.692 | 2.288 | 2.692 | 2.593 | 3.051 | 2.593 | 3.051 | ns |

### Minimum and Maximum DC/AC Input and Output Levels Specification using LPDDR-LVCMOS 1.8 V Mode

***Table 151 •*** **LPDDR-LVCMOS 1.8 V Mode Recommended DC Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 1.710 | 1.8 | 1.89 | V |

***Table 152 •*** **LPDDR-LVCMOS 1.8 V Mode DC Input Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high (for MSIOD and DDRIO I/O banks) | $V_{IH}$ (DC) | 0.65 × $V_{DDI}$ | 1.89 | V |
| DC input logic high (for MSIO I/O bank) | $V_{IH}$ (DC) | 0.65 × $V_{DDI}$ | 3.45 | V |
| DC input logic low | $V_{IL}$ (DC) | –0.3 | 0.35 × $V_{DDI}$ | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

***Table 153 •*** **LPDDR-LVCMOS 1.8 V Mode DC Output Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC output logic high | $V_{OH}$ | $V_{DDI}$ – 0.45 | | V |
| DC output logic low | $V_{OL}$ | | 0.45 | V |

***Table 154 •*** **LPDDR-LVCMOS 1.8 V Minimum and Maximum AC Switching Speeds**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for DDRIO I/O bank) | $D_{MAX}$ | 400 | Mbps | AC loading: 17pf load, 8 ma drive and above/all slew |

***Table 155 •*** **LPDDR-LVCMOS 1.8 V Calibrated Impedance Option**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | RODT_CAL | 75, 60, 50, 33, 25, 20 | Ω |

**Table 162 • LVDS DC Output Voltage Specification**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DC output logic high | $V_{OH}$ | 1.25 | 1.425 | 1.6 | V |
| DC output logic low | $V_{OL}$ | 0.9 | 1.075 | 1.25 | V |

**Table 163 • LVDS DC Differential Voltage Specification**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Differential output voltage swing | $V_{OD}$ | 250 | 350 | 450 | mV |
| Output common mode voltage | $V_{OCM}$ | 1.125 | 1.25 | 1.375 | V |
| Input common mode voltage | $V_{ICM}$ | 0.05 | 1.25 | 2.35 | V |
| Input differential voltage | $V_{ID}$ | 100 | 350 | 600 | mV |

**Table 164 • LVDS Minimum and Maximum AC Switching Speed**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 535 | Mbps | AC loading: 12 pF / 100 Ω differential load |
| Maximum data rate (for MSIOD I/O bank) no pre-emphasis | $D_{MAX}$ | 620 | Mbps | AC loading: 10 pF / 100 Ω differential load |
| | | 700 | Mbps | AC loading: 2 pF / 100 Ω differential load |

**Table 165 • LVDS AC Impedance Specifications**

| Parameter | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Termination resistance | RT | 100 | | Ω |

**Table 166 • LVDS AC Test Parameter Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | Cross point | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |

### LVDS25 AC Switching Characteristics

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 2.375 V

**Table 167 • LVDS25 Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

| | $T_{PY}$ | | |
|---|---|---|---|
| **On-Die Termination (ODT)** | **–1** | **–Std** | **Unit** |
| None | 2.774 | 3.263 | ns |
| 100 | 2.775 | 3.264 | ns |

**Table 198 •** **Mini-LVDS AC Impedance Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Termination resistance | $R_T$ | 100 | Ω |

**Table 199 •** **Mini-LVDS AC Test Parameter Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | Cross point | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |

### AC Switching Characteristics

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 2.375 V.

**Table 200 •** **Mini-LVDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)**

|  | $T_{PY}$ |  |  |
|---|---|---|---|
| On-Die Termination (ODT) | –1 | –Std | Unit |
| None | 2.855 | 3.359 | ns |
| 100 | 2.85 | 3.353 | ns |
| None | 2.602 | 3.061 | ns |
| 100 | 2.597 | 3.055 | ns |

**Table 201 •** **Mini-LVDS AC Switching Characteristics for Transmitter for MSIO I/O Bank (Output and Tristate Buffers)**

| $T_{DP}$ |  | $T_{ZL}$ |  | $T_{ZH}$ |  | $T_{HZ}$ |  | $T_{LZ}$ |  | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std |  |
| 2.097 | 2.467 | 2.308 | 2.715 | 2.296 | 2.701 | 1.964 | 2.31 | 1.949 | 2.293 | ns |

**Table 202 •** **Mini-LVDS AC Switching Characteristics for Transmitter (for MSIOD I/O Bank - Output and Tristate Buffers)**

|  | $T_{DP}$ |  | $T_{ZL}$ |  | $T_{ZH}$ |  | $T_{HZ}$ |  | $T_{LZ}$ |  | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
|  | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std |  |
| No pre-emphasis | 1.614 | 1.899 | 1.562 | 1.837 | 1.553 | 1.826 | 1.593 | 1.874 | 1.578 | 1.856 | ns |
| Min pre-emphasis | 1.604 | 1.887 | 1.745 | 2.053 | 1.731 | 2.036 | 1.892 | 2.225 | 1.861 | 2.189 | ns |
| Med pre-emphasis | 1.521 | 1.79 | 1.753 | 2.062 | 1.737 | 2.043 | 1.9 | 2.235 | 1.868 | 2.197 | ns |
| Max pre-emphasis | 1.492 | 1.754 | 1.762 | 2.073 | 1.745 | 2.052 | 1.91 | 2.247 | 1.876 | 2.206 | ns |

**_Table 232 •_ RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9 _(continued)_**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Address setup time | $T_{ADDRSU}$ | 0.475 | | 0.559 | | ns |
| Address hold time | $T_{ADDRHD}$ | 0.274 | | 0.322 | | ns |
| Data setup time | $T_{DSU}$ | 0.336 | | 0.395 | | ns |
| Data hold time | $T_{DHD}$ | 0.082 | | 0.096 | | ns |
| Block select setup time | $T_{BLKSU}$ | 0.207 | | 0.244 | | ns |
| Block select hold time | $T_{BLKHD}$ | 0.216 | | 0.254 | | ns |
| Block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 1.529 | | 1.799 | ns |
| Block select minimum pulse width | $T_{BLKMPW}$ | 0.186 | | 0.219 | | ns |
| Read enable setup time | $T_{RDESU}$ | 0.485 | | 0.57 | | ns |
| Read enable hold time | $T_{RDEHD}$ | 0.071 | | 0.083 | | ns |
| Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLESU}$ | 0.248 | | 0.291 | | ns |
| Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLEHD}$ | 0.102 | | 0.12 | | ns |
| Asynchronous reset to output propagation delay | $T_{R2Q}$ | | 1.514 | | 1.781 | ns |
| Asynchronous reset removal time | $T_{RSTREM}$ | 0.506 | | 0.595 | | ns |
| Asynchronous reset recovery time | $T_{RSTREC}$ | 0.004 | | 0.005 | | ns |
| Asynchronous reset minimum pulse width | $T_{RSTMPW}$ | 0.301 | | 0.354 | | ns |
| Pipelined register asynchronous reset removal time | $T_{PLRSTREM}$ | –0.279 | | –0.328 | | ns |
| Pipelined register asynchronous reset recovery time | $T_{PLRSTREC}$ | 0.327 | | 0.385 | | ns |
| Pipelined register asynchronous reset minimum pulse width | $T_{PLRSTMPW}$ | 0.282 | | 0.332 | | ns |
| Synchronous reset setup time | $T_{SRSTSU}$ | 0.226 | | 0.265 | | ns |
| Synchronous reset hold time | $T_{SRSTHD}$ | 0.036 | | 0.043 | | ns |
| Write enable setup time | $T_{WESU}$ | 0.415 | | 0.488 | | ns |
| Write enable hold time | $T_{WEHD}$ | 0.048 | | 0.057 | | ns |
| Maximum frequency | $F_{MAX}$ | | 400 | | 340 | MHz |

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 4K × 4 in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

**_Table 233 •_ RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4K × 4**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Clock period | $T_{CY}$ | 2.5 | | 2.941 | | ns |
| Clock minimum pulse width high | $T_{CLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Clock minimum pulse width low | $T_{CLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock period | $T_{PLCY}$ | 2.5 | | 2.941 | | ns |
| Pipelined clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.125 | | 1.323 | | ns |

**Table 238 •** **µSRAM (RAM64x16) in 64 × 16 Mode *(continued)***

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Read synchronous reset hold time | $T_{SRSTHD}$ | 0.061 | | 0.071 | | ns |
| Write clock period | $T_{CCY}$ | 4 | | 4 | | ns |
| Write clock minimum pulse width high | $T_{CCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Write clock minimum pulse width low | $T_{CCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Write block setup time | $T_{BLKCSU}$ | 0.404 | | 0.476 | | ns |
| Write block hold time | $T_{BLKCHD}$ | 0.007 | | 0.008 | | ns |
| Write input data setup time | $T_{DINCSU}$ | 0.115 | | 0.135 | | ns |
| Write input data hold time | $T_{DINCHD}$ | 0.15 | | 0.177 | | ns |
| Write address setup time | $T_{ADDRCSU}$ | 0.088 | | 0.104 | | ns |
| Write address hold time | $T_{ADDRCHD}$ | 0.128 | | 0.15 | | ns |
| Write enable setup time | $T_{WECSU}$ | 0.397 | | 0.467 | | ns |
| Write enable hold time | $T_{WECHD}$ | –0.026 | | –0.03 | | ns |
| Maximum frequency | $F_{MAX}$ | | 250 | | 250 | MHz |

The following table lists the µSRAM in 128 × 9 mode in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

**Table 239 •** **µSRAM (RAM128x9) in 128 × 9 Mode**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Read clock period | $T_{CY}$ | 4 | | 4 | | ns |
| Read clock minimum pulse width high | $T_{CLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read clock minimum pulse width low | $T_{CLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock period | $T_{PLCY}$ | 4 | | 4 | | ns |
| Read pipeline clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.266 | | 0.313 | ns |
| Read access time without pipeline register | | | 1.677 | | 1.973 | ns |
| Read address setup time in synchronous mode | $T_{ADDRSU}$ | 0.301 | | 0.354 | | ns |
| Read address setup time in asynchronous mode | | 1.856 | | 2.184 | | ns |
| Read address hold time in synchronous mode | $T_{ADDRHD}$ | 0.091 | | 0.107 | | ns |
| Read address hold time in asynchronous mode | | –0.778 | | –0.915 | | ns |
| Read enable setup time | $T_{RDENSU}$ | 0.278 | | 0.327 | | ns |
| Read enable hold time | $T_{RDENHD}$ | 0.057 | | 0.067 | | ns |
| Read block select setup time | $T_{BLKSU}$ | 1.839 | | 2.163 | | ns |
| Read block select hold time | $T_{BLKHD}$ | –0.65 | | –0.765 | | ns |
| Read block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 2.036 | | 2.396 | ns |

**Table 242 •** **µSRAM (RAM512x2) in 512 × 2 Mode *(continued)***

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Write clock period | $T_{CCY}$ | 4 | | 4 | | ns |
| Write clock minimum pulse width high | $T_{CCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Write clock minimum pulse width low | $T_{CCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Write block setup time | $T_{BLKCSU}$ | 0.404 | | 0.476 | | ns |
| Write block hold time | $T_{BLKCHD}$ | 0.007 | | 0.008 | | ns |
| Write input data setup time | $T_{DINCSU}$ | 0.101 | | 0.118 | | ns |
| Write input data hold time | $T_{DINCHD}$ | 0.137 | | 0.161 | | ns |
| Write address setup time | $T_{ADDRCSU}$ | 0.088 | | 0.104 | | ns |
| Write address hold time | $T_{ADDRCHD}$ | 0.247 | | 0.29 | | ns |
| Write enable setup time | $T_{WECSU}$ | 0.397 | | 0.467 | | ns |
| Write enable hold time | $T_{WECHD}$ | –0.03 | | –0.03 | | ns |
| Maximum frequency | $F_{MAX}$ | | 250 | | 250 | MHz |

The following table lists the µSRAM in 1024 × 1 mode in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

**Table 243 •** **µSRAM (RAM1024x1) in 1024 × 1 Mode**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Read clock period | $T_{CY}$ | 4 | | 4 | | ns |
| Read clock minimum pulse width high | $T_{CLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read clock minimum pulse width low | $T_{CLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock period | $T_{PLCY}$ | 4 | | 4 | | ns |
| Read pipeline clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.27 | | 0.31 | ns |
| Read access time without pipeline register | | | 1.78 | | 2.1 | ns |
| Read address setup time in synchronous mode | $T_{ADDRSU}$ | 0.301 | | 0.354 | | ns |
| Read address setup time in asynchronous mode | | 1.978 | | 2.327 | | ns |
| Read address hold time in synchronous mode | $T_{ADDRHD}$ | 0.137 | | 0.161 | | ns |
| Read address hold time in asynchronous mode | | –0.6 | | –0.71 | | ns |
| Read enable setup time | $T_{RDENSU}$ | 0.278 | | 0.327 | | ns |
| Read enable hold time | $T_{RDENHD}$ | 0.057 | | 0.067 | | ns |
| Read block select setup time | $T_{BLKSU}$ | 1.839 | | 2.163 | | ns |
| Read block select hold time | $T_{BLKHD}$ | –0.65 | | –0.77 | | ns |
| Read block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 2.16 | | 2.54 | ns |
| Read asynchronous reset removal time (pipelined clock) | $T_{RSTREM}$ | –0.02 | | –0.03 | | ns |
| Read asynchronous reset removal time (non-pipelined clock) | | 0.046 | | 0.054 | | ns |

***Table 277 •*** **Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz) *(continued)***

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Startup time (with regard to stable oscillator output) | SUXTAL | | | 0.8 | ms | 005, 010, 025, and 050 devices |
| | | | | 1.0 | ms | 090 and 150 devices |

***Table 278 •*** **Electrical Characteristics of the Crystal Oscillator – Medium Gain Mode (2 MHz)**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Operating frequency | FXTAL | | 2 | | MHz | |
| Accuracy | ACCXTAL | | | 0.00105 | % | 050 devices |
| | | | | 0.003 | % | 005, 010, 025, 090, and 150 devices |
| | | | | 0.004 | % | 060 devices |
| Output duty cycle | CYCXTAL | | 49–51 | 47–53 | % | |
| Output period jitter (peak to peak) | JITPERXTAL | | 1 | 5 | ns | |
| Output cycle to cycle jitter (peak to peak) | JITCYCXTAL | | 1 | 5 | ns | |
| Operating current | IDYNXTAL | | 0.3 | | mA | |
| Input logic level high | VIHXTAL | 0.9 $V_{PP}$ | | | V | |
| Input logic level low | VILXTAL | | | 0.1 $V_{PP}$ | V | |
| Startup time (with regard to stable oscillator output) | SUXTAL | | | 4.5 | ms | 010 and 050 devices |
| | | | | 5 | ms | 005 and 025 devices |
| | | | | 7 | ms | 090 and 150 devices |

***Table 279 •*** **Electrical Characteristics of the Crystal Oscillator – Low Gain Mode (32 kHz)**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Operating frequency | FXTAL | | 32 | | kHz | |
| Accuracy | ACCXTAL | | | 0.004 | % | 005, 010, 025, 050, 060, and 090 devices |
| | | | | 0.005 | % | 150 devices |
| Output duty cycle | CYCXTAL | | 49–51 | 47–53 | % | |
| Output period jitter (peak to peak) | JITPERXTAL | | 150 | 300 | ns | |
| Output cycle to cycle jitter (peak to peak) | JITCYCXTAL | | 150 | 300 | ns | |
| Operating current | IDYNXTAL | | 0.044 | | mA | 010 and 050 devices |
| | | | 0.060 | | mA | 005, 025, 060, 090, and 150 devices |
| Input logic level high | VIHXTAL | 0.9 $V_{PP}$ | | | V | |
| Input logic level low | VILXTAL | | | 0.1 $V_{PP}$ | V | |
| Startup time (with regard to stable oscillator output) | SUXTAL | | | 115 | ms | 005, 025, 050, 090, and 150 devices |
| | | | | 126 | ms | 010 devices |

## 2.3.21 Clock Conditioning Circuits (CCC)

The following table lists the CCC/PLL specifications in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 282 •*** **IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification**

| Parameter | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|
| Clock conditioning circuitry input frequency $F_{IN\_CCC}$ | 1 | | 200 | MHz | All CCC |
| | 0.032 | | 200 | MHz | 32 kHz capable CCC |
| Clock conditioning circuitry output frequency $F_{OUT\_CCC}$[1] | 0.078 | | 400 | MHz | |
| PLL VCO frequency[2] | 500 | | 1000 | MHz | |
| Delay increments in programmable delay blocks | | 75 | 100 | ps | |
| Number of programmable values in each programmable delay block | | | 64 | | |
| Acquisition time | | 70 | 100 | µs | $F_{IN}$ >= 1 MHz |
| | | 1 | 16 | ms | $F_{IN}$ = 32 kHz |
| Input duty cycle (reference clock) | | | | | Internal Feedback |
| | 10 | | 90 | % | 1 MHz ≤ $F_{IN\_CCC}$ ≤ 25 MHz |
| | 25 | | 75 | % | 25 MHz ≤ $F_{IN\_CCC}$≤ 100 MHz |
| | 35 | | 65 | % | 100 MHz ≤ $F_{IN\_CCC}$ ≤ 150 MHz |
| | 45 | | 55 | % | 150 MHz ≤ $F_{IN\_CCC}$ ≤ 200 MHz |
| | | | | | External Feedback (CCC, FPGA, Off-chip) |
| | 25 | | 75 | % | 1 MHz ≤ $F_{IN\_CCC}$ ≤ 25 MHz |
| | 35 | | 65 | % | 25 MHz ≤ $F_{IN\_CCC}$ ≤ 35 MHz |
| | 45 | | 55 | % | 35 MHz ≤ $F_{IN\_CCC}$ ≤ 50 MHz |
| Output duty cycle | 48 | | 52 | % | 050 devices $F_{OUT}$ ≤ 400 MHz |
| | 48 | | 52 | % | 005, 010, and 025 devices<br>$F_{OUT}$ < 350 MHz |
| | 46 | | 54 | % | 005, 010, and 025 devices<br>350 MHz ≤ $F_{out}$ ≤ 400 MHz |
| | 48 | | 52 | % | 060 and 090 devices<br>$F_{OUT}$ ≤ 100 MHz |
| | 44 | | 52 | % | 060 and 090 devices<br>100 MHz ≤ $F_{OUT}$ ≤ 400 MHz |
| | 48 | | 52 | % | 150 devices<br>$F_{OUT}$ ≤ 120 MHz |
| | 45 | | 52 | % | 150 devices<br>120 MHz ≤ $F_{OUT}$ ≤ 400 MHz |
| **Spread Spectrum Characteristics** | | | | | |
| Modulation frequency range | 25 | 35 | 50 | k | |
| Modulation depth range | 0 | | 1.5 | % | |
| Modulation depth control | | 0.5 | | % | |

1. The minimum output clock frequency is limited by the PLL. For more information, see *UG0449: SmartFusion2 and IGLOO2 Clocking Resources User Guide*.
2. The PLL is used in conjunction with the Clock Conditioning Circuitry. Performance is limited by the CCC output frequency.

The following table lists the CCC/PLL jitter specifications in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 283 •*** **IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Jitter Specifications**

| **CCC Output Maximum Peak-to-Peak Period Jitter $F_{OUT\_CCC}$** | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Conditions/Package Combinations** | | | | | **Unit** |
| **10 FG484, 050 FG896/FG484/FCS325 Packages[1]** | SSO = 0 | 0 < SSO <= 2 | SSO <= 4 | SSO <= 8 | SSO <= 16 | |
| 20 MHz to 100 MHz | Max(110, ± 1% x (1/$F_{OUT\_CCC}$)) | Max(150, ± 1% x (1/$F_{OUT\_CCC}$)) | | | | ps |
| 100 MHz to 400 MHz | Max(120, ± 1% x (1/$F_{OUT\_CCC}$)) | Max(150, ± 1% x (1/$F_{OUT\_CCC}$)) | | | Max(170, ± 1% x (1/$F_{OUT\_CCC}$)) | ps |
| **025 FG484/FCS325 Package[1]** | 0 < SSO <=16 | | | | | |
| 20 MHz to 74 MHz | ± 1% x (1/$F_{OUT\_CCC}$)) | | | | | ps |
| 74 MHz to 400 MHz | 210 | | | | | ps |
| **005 FG484 Package[1]** | 0 < SSO <=16 | | | | | |
| 20 MHz to 53 MHz | ± 1% x (1/$F_{OUT\_CCC}$)) | | | | | ps |
| 53 MHz to 400 MHz | 270 | | | | | ps |
| **090 FG676 and FC325 Package[1]** | 0 < SSO <=16 | | | | | |
| 20 MHz to 100 MHz | ± 1% x (1/$F_{OUT\_CCC}$)) | | | | | ps |
| 100 MHz to 400 MHz | 150 | | | | | ps |
| **060 FG676 Package[1]** | 0 < SSO <=16 | | | | | |
| 20 MHz to 100 MHz | ± 1% x (1/$F_{OUT\_CCC}$) | | | | | ps |
| 100 MHz to 400 MHz | 150 | | | | | |
| **150 FC1152 Package[1]** | 0 < SSO <=16 | | | | | |
| 20 MHz to 100 MHz | ± 1% x (1/$F_{OUT\_CCC}$)) | | | | | ps |
| 100 MHz to 400 MHz | 120 | | | | | ps |

1. SSO data is based on LVCMOS 2.5 V MSIO and/or MSIOD bank I/Os.

## 2.3.24 Power-up to Functional Times

The following table lists the SmartFusion2 power-up to functional times in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 288 •*** **Power-up to Functional Times for SmartFusion2**

| | | | | **Maximum Power-up to Functional Time for SmartFusion2 (uS)** | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **From** | **To** | **Description** | **005** | **010** | **025** | **050** | **060** | **090** | **150** |
| $T_{POR2OUT}$ | POWER_ON_RESET_N | Output available at I/O | Fabric to output | 647 | 500 | 531 | 483 | 474 | 524 | 647 |
| $T_{POR2MSSRST}$ | POWER_ON_RESET_N | MSS_RESET_N_M2F | Fabric to MSS | 644 | 497 | 528 | 480 | 468 | 518 | 641 |
| $T_{MSSRST2OUT}$ | MSS_RESET_N_M2F | Output available at I/O | MSS to output | 3.6 | 3.6 | 3.6 | 3.4 | 4.9 | 4.8 | 4.8 |
| $T_{VDD2OUT}$ | $V_{DD}$ | Output available at I/O | $V_{DD}$ at its minimum threshold level to output | 3096 | 2975 | 3012 | 2959 | 2869 | 2992 | 3225 |
| $T_{VDD2POR}$ | $V_{DD}$ | POWER_ON_RESET_N | $V_{DD}$ at its minimum threshold level to fabric | 2476 | 2487 | 2496 | 2486 | 2406 | 2563 | 2602 |
| $T_{VDD2MSSRST}$ | $V_{DD}$ | MSS_RESET_N_M2F | $V_{DD}$ at its minimum threshold level to MSS | 3093 | 2972 | 3008 | 2956 | 2864 | 2987 | 3220 |
| $T_{VDD2WPU}$ | DEVRST_N | DDRIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 2500 | 2487 | 2509 | 2475 | 2507 | 2519 | 2617 |
| | DEVRST_N | MSIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 2504 | 2491 | 2510 | 2478 | 2517 | 2525 | 2620 |
| | DEVRST_N | MSIOD Inbuf weak pull | DEVRST_N to Inbuf weak pull | 2479 | 2468 | 2493 | 2458 | 2486 | 2499 | 2595 |

**Note:** For more information about power-up times, see *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.

**Table 303 • I2C Characteristics *(continued)***

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Maximum data rate | $D_{MAX}$ | | | 400 | Kbps | Fast mode |
| | | | | 100 | Kbps | Standard mode |
| Pulse width of spikes which must be suppressed by the input filter | $T_{FILT}$ | | 50 | | ns | Fast mode |

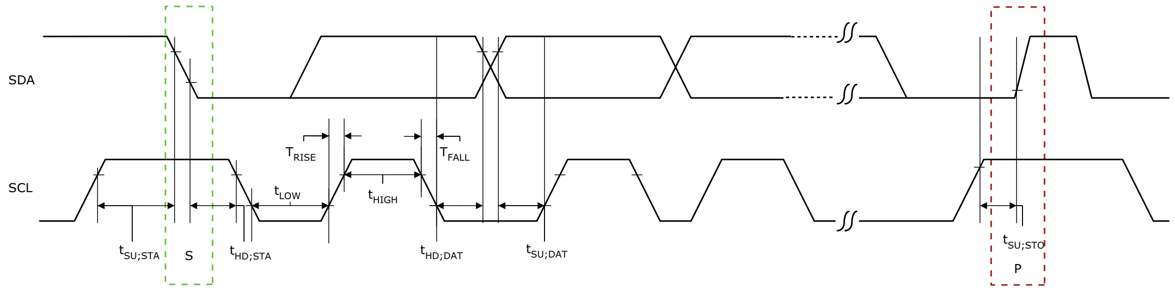
1. These values are provided for MSIO Bank–LVTTL 8 mA Low Drive at 25 °C, typical conditions. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.
2. These maximum values are provided for information only. Minimum output buffer resistance values depend on $V_{DDIx}$, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.
3. R(PULL-DOWN-MAX) = (VOLspec)/IOLspec.
4. R(PULL-UP-MAX) = (VDDImax–VOHspec)/IOHspec.

The following table lists the $I^2C$ switching characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V

**Table 304 • I2C Switching Characteristics**

| | | –1 | Std | |
|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Min** | **Unit** |
| Low period of I2C_x_SCL | $T_{LOW}$ | 1 | 1 | PCLK cycles |
| High period of I2C_x_SCL | $T_{HIGH}$ | 1 | 1 | PCLK cycles |
| START hold time | $T_{HD;STA}$ | 1 | 1 | PCLK cycles |
| START setup time | $T_{SU;STA}$ | 1 | 1 | PCLK cycles |
| DATA hold time | $T_{HD;DAT}$ | 1 | 1 | PCLK cycles |
| DATA setup time | $T_{SU;DAT}$ | 1 | 1 | PCLK cycles |
| STOP setup time | $T_{SU;STO}$ | 1 | 1 | PCLK cycles |

**Figure 21 • $I^2C$ Timing Parameter Definition**



## 2.3.34 MMUART Characteristics

The following table lists the MMUART characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 308 •*** **MMUART Characteristics**

| Parameter | Description | –1 | –Std | Unit |
|---|---|---|---|---|
| FMMUART_REF_CLK | Internally sourced MMUART reference clock frequency. | 166 | 142 | MHz |
| BAUDMMUARTTx | Maximum transmit baud rate | 10.375 | 8.875 | Mbps |
| BAUDMMUARTRx | Maximum receive baud rate | 10.375 | 8.875 | Mbps |

## 2.3.35 IGLOO2 Specifications

### 2.3.35.1 HPMS Clock Frequency

The following table lists the maximum frequency for HPMS main clock in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 309 •*** **Maximum Frequency for HPMS Main Clock**

| Symbol | Description | –1 | –Std | Unit |
|---|---|---|---|---|
| HPMS_CLK | Maximum frequency for the HPMS main clock | 166 | 142 | MHz |

### 2.3.35.2 IGLOO2 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_0_CLK. For timing parameter definitions, see Figure 23, page 131.

The following table lists the SPI characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 310 •*** **SPI Characteristics for All Devices**

| Symbol | Description | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| SPIFMAX | Maximum operating frequency of SPI interface | | | 20 | MHz | |
| sp1 | SPI_[0\|1]_CLK minimum period | | | | | |
| | SPI_[0\|1]_CLK = PCLK/2 | 12 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/4 | 24.1 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/8 | 48.2 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/16 | 0.1 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/32 | 0.19 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/64 | 0.39 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/128 | 0.77 | | | µs | |