Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	12084
Total RAM Bits	933888
Number of I/O	138
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LFBGA
Supplier Device Package	256-FPBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2gl010t-1vfg256

2 IGLOO2 FPGA and SmartFusion2 SoC FPGA

Microsemi's mainstream SmartFusion®2 SoC and IGLOO®2 FPGA families integrate an industry standard 4-input lookup table-based (LUT) FPGA fabric with integrated math blocks, multiple embedded memory blocks, and high-performance SerDes communication interfaces on a single chip. Both families benefit from low-power flash technology and are the most secure and reliable FPGAs in the industry. These next generation devices offer up to 150K Logic Elements, up to 5 MBs of embedded RAM, up to 16 SerDes lanes, and up to four PCI Express Gen 2 endpoints, as well as integrated hard DDR3 memory controllers with error correction.

SmartFusion2 devices integrate an entire low-power, real-time microcontroller subsystem (MSS) with a rich set of industry-standard peripherals including Ethernet, USB, and CAN, while IGLOO2 devices integrate a high-performance memory subsystem with on-chip flash, 32 Kbyte embedded SRAM, and multiple DMA controllers.

2.1 Device Status

The following table shows the design security densities and development status of the IGLOO2 FPGA and SmartFusion2 SoC FPGA devices.

Table 1 • **IGLOO2 and SmartFusion2 Design Security Densities**

Design Security Device Densities	Status
005	Production
010, 010T	Production
025, 025T	Production
050, 050T	Production
060, 060T	Production
090, 090T	Production
150, 150T	Production

The following table shows the data security densities and development status of the IGLOO2 FPGA and SmartFusion2 SoC FPGA devices.

Table 2 • **IGLOO2 and SmartFusion2 Data Security Densities**

Data Security Device Densities	Status
005S	Production
010TS	Production
025TS	Production
050TS	Production
060TS	Production
090TS	Production
150TS	Production

Figure 1 • **High Temperature Data Retention (HTR)**

2.3.1.1 Overshoot/Undershoot Limits

For AC signals, the input signal may undershoot during transitions to –1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

For AC signals, the input signal may overshoot during transitions to V_{CCI} + 1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

Note: The above specifications do not apply to the PCI standard. The IGLOO2 and SmartFusion2 PCI I/Os are compliant with the PCI standard including the PCI overshoot/undershoot specifications.

2.3.1.2 Thermal Characteristics

The temperature variable in the Microsemi SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption causes the chip's junction temperature to be higher than the ambient, case, or board temperatures.

EQ1 through EQ3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

EQ 1

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

EQ 2

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

EQ 3

2.3.2 Power Consumption

The following sections describe the power consumptions of the devices.

2.3.2.1 Quiescent Supply Current

Table 10 • **Quiescent Supply Current Characteristics**

	Modes and Configurations	
Power Supplies/Blocks	**Non-Flash*Freeze**	**Flash*Freeze**
FPGA Core	On	Off
V_{DD}/SERDES_[01]_VDD[1]	On	On
V_{PP}/V_{PPNVM}	On	On
HPMS_MDDR_PLL_VDDA/FDDR_PLL_VDDA/ CCC_XX[01]_PLL_VDDA/PLL0_PLL1_HPMS_MDDR_VDDA	0 V	0 V
SERDES_[01]_PLL_VDDA[2]	0 V	0 V
SERDES_[01]_L[0123]_VDDAPLL/VDD_2V5[2]	On	On
SERDES_[01]_L[0123]_VDDAIIO[2]	On	On
V_{DDIx}[3, 4]	On	On
V_{REFx}	On	On
MSSDDR CLK	32 kHz	32 kHz
RAM	On	Sleep state
System controller	50 MHz	50 MHz
50 MHz oscillator (enable/disable)	Enable	Disabled
1 MHz oscillator (enable/disable)	Disabled	Disabled
Crystal oscillator (enable/disable)	Disabled	Disabled

1. SERDES_[01]_VDD Power Supply is shorted to V_{DD}.
2. SerDes and DDR blocks to be unused.
3. V_{DDIx} has been set to ON for test conditions as described. Banks on the east side should always be powered with the appropriate V_{DDI} bank supplies. For details on bank power supplies, see “Recommendation for Unused Bank Supplies” table in the *AC393: SmartFusion2 and IGLOO2 Board Design Guidelines Application Note*.
4. No Differential (that is to say, LVDS) I/Os or ODT attributes to be used.

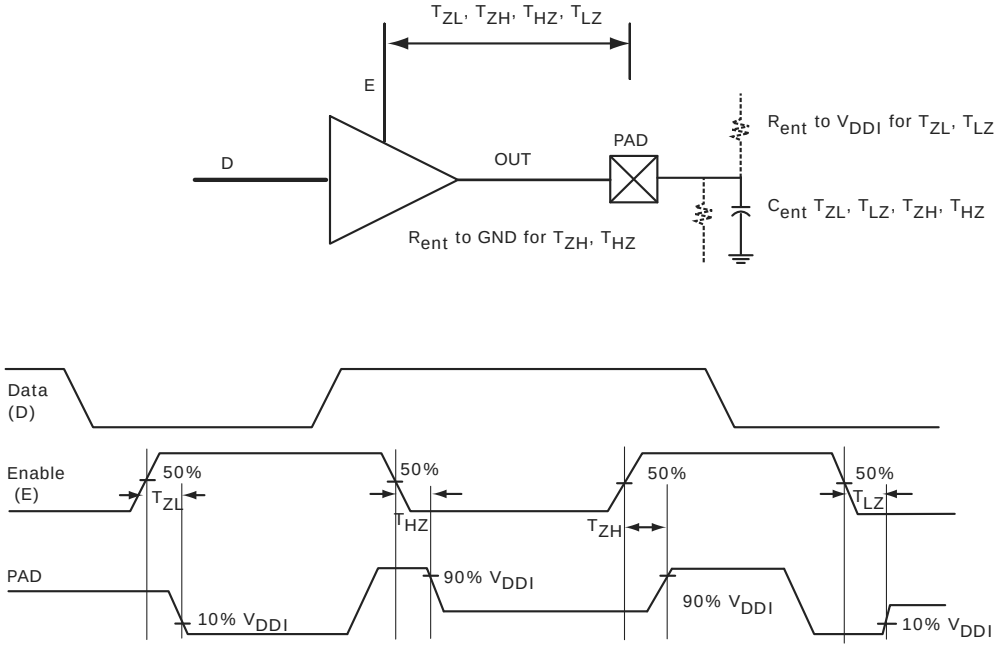
Table 11 • **SmartFusion2 and IGLOO2 Quiescent Supply Current (V_{DD} = 1.2 V) – Typical Process**

Symbol	Modes	005	010	025	050	060	090	150	Unit	Conditions
IDC1	Non-Flash*Freeze	6.2	6.9	8.9	13.1	15.3	15.4	27.5	mA	Typical (T_J = 25 °C)
		24.0	28.4	40.6	67.8	80.6	81.4	144.7	mA	Commercial (T_J = 85 °C)
		35.2	41.9	60.5	102.1	121.4	122.6	219.1	mA	Industrial (T_J = 100 °C)

2.3.5.3 Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The following figure shows the methodology of characterization illustrated by the enable path test point.

Figure 5 • **Tristate Buffer for Enable Path Test Point**



2.3.5.4 I/O Speeds

This section describes the maximum data rate summary of I/O in worst-case industrial conditions. See the individual I/O standards for operating conditions.

Table 18 • **Maximum Data Rate Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions**

I/O	MSIO	MSIOD	DDRIO	Unit
PCI 3.3 V	630			Mbps
LVTTL 3.3 V	600			Mbps
LVCMOS 3.3 V	600			Mbps
LVCMOS 2.5 V	410	420	400	Mbps
LVCMOS 1.8 V	295	400	400	Mbps
LVCMOS 1.5 V	160	220	235	Mbps
LVCMOS 1.2 V	120	160	200	Mbps
LPDDR-LVCMOS 1.8 V mode			400	Mbps

2.3.5.5 Detailed I/O Characteristics

Table 24 • **Input Capacitance, Leakage Current, and Ramp Time**

Symbol	Description	Maximum	Unit	Conditions
C_{IN}	Input capacitance	10	pF	
I_{IL} (dc)	Input current low (Applicable to HSTL/SSTL inputs only)	400	µA	V_{DDI} = 2.5 V
		500	µA	V_{DDI} = 1.8 V
		600	µA	V_{DDI} = 1.5 V[1]
	Input current low (Applicable to all other digital inputs)	10	µA	
I_{IH} (dc)	Input current high (Applicable to HSTL/SSTL inputs only)	400	µA	V_{DDI} = 2.5 V
		500	µA	V_{DDI} = 1.8 V
		600	µA	V_{DDI} = 1.5 V[1]
	Input current high (Applicable to all other digital inputs)	10	µA	
T_{RAMPIN}[2]	Input ramp time (Applicable to all digital inputs)	50	ns	

1. Applicable when I/O pair is programmed with an HSTL/SSTL I/O type on IOP and an un-terminated I/O type (LVCMOS, for example) on ION pad.
2. Voltage ramp must be monotonic.

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of DDRIO I/O bank at V_{OH}/V_{OL} Level.

Table 25 • **I/O Weak Pull-up/Pull-down Resistances for DDRIO I/O Bank**

	R(WEAK PULL-UP) at V_{OH} (Ω)		R(WEAK PULL-DOWN) at V_{OL} (Ω)	
V_{DDI} Domain	**Min**	**Max**	**Min**	**Max**
2.5 V[1, 2]	10K	17.8K	9.98K	18K
1.8 V[1, 2]	10.3K	19.1K	10.3K	19.5K
1.5 V[1, 2]	10.6K	20.2K	10.6K	21.1K
1.2 V[1, 2]	11.1K	22.7K	11.2K	24.6K

1. R(WEAK PULL-DOWN) = (VOLspec)/I(WEAK PULL-DOWN MAX).
2. R(WEAK PULL-UP) = (VDDImax – VOHspec)/I(WEAK PULL-UP MIN).

Table 46 • **LVCMOS 2.5 V Transmitter Characteristics for DDRIO Bank (Output and Tristate Buffers) *(continued)***

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}[1]		T_{LZ}[1]		Unit
		–1	–Std	–1	–Std	–1	–Std	–1	–Std	–1	–Std	
4 mA	Slow	3.095	3.641	2.705	3.182	3.088	3.633	4.738	5.575	4.348	5.116	ns
	Medium	2.825	3.324	2.488	2.927	2.823	3.321	4.492	5.285	4.063	4.781	ns
	Medium fast	2.701	3.178	2.384	2.804	2.698	3.173	4.364	5.135	3.945	4.642	ns
	Fast	2.69	3.165	2.377	2.796	2.687	3.161	4.359	5.129	3.94	4.636	ns
6 mA	Slow	2.919	3.434	2.491	2.93	2.902	3.414	5.085	5.983	4.674	5.5	ns
	Medium	2.65	3.118	2.279	2.681	2.642	3.108	4.845	5.701	4.375	5.148	ns
	Medium fast	2.529	2.975	2.176	2.56	2.521	2.965	4.724	5.558	4.259	5.011	ns
	Fast	2.516	2.96	2.168	2.551	2.508	2.95	4.717	5.55	4.251	5.002	ns
8 mA	Slow	2.863	3.368	2.427	2.855	2.844	3.346	5.196	6.114	4.769	5.612	ns
	Medium	2.599	3.058	2.217	2.608	2.59	3.047	4.952	5.827	4.471	5.261	ns
	Medium fast	2.483	2.921	2.114	2.487	2.473	2.91	4.832	5.685	4.364	5.134	ns
	Fast	2.467	2.902	2.106	2.478	2.457	2.89	4.826	5.678	4.348	5.116	ns
12 mA	Slow	2.747	3.232	2.296	2.701	2.724	3.204	5.39	6.342	4.938	5.81	ns
	Medium	2.493	2.934	2.102	2.473	2.483	2.921	5.166	6.078	4.65	5.471	ns
	Medium fast	2.382	2.803	2.006	2.36	2.371	2.789	5.067	5.962	4.546	5.349	ns
	Fast	2.369	2.787	1.999	2.352	2.357	2.773	5.063	5.958	4.538	5.339	ns
16 mA	Slow	2.677	3.149	2.213	2.604	2.649	3.116	5.575	6.56	5.08	5.977	ns
	Medium	2.432	2.862	2.028	2.386	2.421	2.848	5.372	6.32	4.801	5.649	ns
	Medium fast	2.324	2.734	1.937	2.278	2.311	2.718	5.297	6.233	4.7	5.531	ns
	Fast	2.313	2.721	1.929	2.269	2.3	2.706	5.296	6.231	4.699	5.529	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 47 • **LVCMOS 2.5 V Transmitter Characteristics for MSIO Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}[1]		T_{LZ}[1]		Unit
		–1	–Std	–1	–Std	–1	–Std	–1	–Std	–1	–Std	
2 mA	Slow	3.48	4.095	3.855	4.534	3.785	4.453	2.12	2.494	3.45	4.059	ns
4 mA	Slow	2.583	3.039	3.042	3.579	3.138	3.691	4.143	4.874	4.687	5.513	ns
6 mA	Slow	2.392	2.815	2.669	3.139	2.82	3.317	4.909	5.775	5.083	5.98	ns
8 mA	Slow	2.309	2.717	2.565	3.017	2.74	3.223	5.812	6.837	5.523	6.497	ns
12 mA	Slow	2.333	2.745	2.437	2.867	2.626	3.089	6.131	7.213	5.712	6.72	ns
16 mA	Slow	2.412	2.838	2.335	2.747	2.533	2.979	6.54	7.694	6.007	7.067	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 70 • **LVCMOS 1.5 V Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers) *(continued)***

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}[1]		T_{LZ}[1]		
		–1	–Std	–1	–Std	–1	–Std	–1	–Std	–1	–Std	Unit
6 mA	Slow	4.244	4.993	3.465	4.076	4.233	4.979	6.39	7.518	5.736	6.748	ns
	Medium	3.774	4.44	3.05	3.587	3.762	4.426	6.114	7.193	5.397	6.35	ns
	Medium fast	3.544	4.17	2.839	3.339	3.529	4.152	5.978	7.033	5.27	6.2	ns
	Fast	3.519	4.14	2.82	3.317	3.504	4.122	5.965	7.017	5.259	6.187	ns
8 mA	Slow	4.099	4.823	3.311	3.894	4.087	4.807	6.584	7.746	5.854	6.888	ns
	Medium	3.656	4.301	2.927	3.443	3.642	4.284	6.311	7.425	5.553	6.533	ns
	Medium fast	3.437	4.044	2.731	3.213	3.42	4.023	6.182	7.273	5.435	6.394	ns
	Fast	3.41	4.012	2.715	3.193	3.393	3.991	6.178	7.269	5.425	6.383	ns
10 mA	Slow	4.029	4.74	3.238	3.809	4.015	4.723	6.732	7.921	5.965	7.018	ns
	Medium	3.601	4.237	2.867	3.372	3.586	4.218	6.473	7.615	5.669	6.669	ns
	Medium fast	3.384	3.981	2.672	3.143	3.365	3.958	6.351	7.471	5.55	6.529	ns
	Fast	3.357	3.949	2.655	3.123	3.338	3.927	6.345	7.464	5.54	6.518	ns
12 mA	Slow	3.974	4.675	3.196	3.759	3.958	4.656	6.842	8.049	6.068	7.139	ns
	Medium	3.55	4.176	2.827	3.326	3.534	4.157	6.584	7.746	5.751	6.766	ns
	Medium fast	3.345	3.935	2.638	3.103	3.325	3.911	6.488	7.633	5.641	6.637	ns
	Fast	3.316	3.902	2.621	3.083	3.297	3.878	6.486	7.63	5.626	6.619	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 71 • **LVCMOS 1.5 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}[1]		T_{LZ}[1]		
		–1	–Std	–1	–Std	–1	–Std	–1	–Std	–1	–Std	Unit
2 mA	Slow	4.423	5.203	5.397	6.35	5.686	6.69	5.609	6.599	5.561	6.542	ns
4 mA	Slow	4.05	4.765	4.503	5.298	4.92	5.788	7.358	8.657	6.525	7.677	ns
6 mA	Slow	4.081	4.801	4.259	5.012	4.699	5.528	7.659	9.011	6.709	7.893	ns
8 mA	Slow	4.234	4.98	4.068	4.786	4.521	5.319	8.218	9.668	7.05	8.294	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 72 • **LVCMOS 1.5 V Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)**

Output Drive Selection	Slew Control	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}[1]		T_{LZ}[1]		
		–1	–Std	–1	–Std	–1	–Std	–1	–Std	–1	–Std	Unit
2 mA	Slow	2.735	3.218	3.371	3.966	3.618	4.257	6.03	7.095	5.705	6.712	ns
4 mA	Slow	2.426	2.854	2.992	3.521	3.221	3.79	6.738	7.927	6.298	7.41	ns
6 mA	Slow	2.433	2.862	2.81	3.306	3.031	3.566	7.123	8.38	6.596	7.76	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

2.3.5.10 1.2 V LVCMOS

LVCMOS 1.2 is a general standard for 1.2 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-12A.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 73 • **LVCMOS 1.2 V DC Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	1.140	1.2	1.26	V

Table 74 • **LVCMOS 1.2 V DC Input Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC input logic high (for MSIOD and DDRIO I/O banks)	V_{IH} (DC)	0.65 × V_{DDI}	1.26	V
DC input logic high (for MSIO I/O bank)	V_{IH} (DC)	0.65 × V_{DDI}	3.45	V
DC input logic low	V_{IL} (DC)	–0.3	0.35 × V_{DDI}	V
Input current high[1]	I_{IH} (DC)			
Input current low[1]	I_{IL} (DC)			

1. See Table 24, page 22.

Table 75 • **LVCMOS 1.2 V DC Output Voltage Specification**

Parameter	Symbol	Min	Max	Unit
DC output logic high	V_{OH}	V_{DDI} × 0.75		V
DC output logic low	V_{OL}		V_{DDI} × 0.25	V

Table 76 • **LVCMOS 1.2 V Minimum and Maximum AC Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	D_{MAX}	200	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIO I/O bank)	D_{MAX}	120	Mbps	AC loading: 17 pF load, maximum drive/slew
Maximum data rate (for MSIOD I/O bank)	D_{MAX}	160	Mbps	AC loading: 17 pF load, maximum drive/slew

Table 136 • **SSTL15 AC Test Parameter Specifications (for DDRIO I/O Bank Only)**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	0.75	V
Resistance for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	C_{ENT}	5	pF
Reference resistance for data test path for SSTL15 Class I (T_{DP})	RTT_TEST	50	Ω
Reference resistance for data test path for SSTL15 Class II (T_{DP})	RTT_TEST	25	Ω
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 1.425 V

Table 137 • **DDR3/SSTL15 Receiver Characteristics for DDRIO I/O Bank – with Calibration Only**

		T_{PY}		
	On-Die Termination (ODT)	**–1**	**–Std**	**Unit**
Pseudo differential	None	1.605	1.888	ns
	20	1.616	1.901	ns
	30	1.613	1.897	ns
	40	1.611	1.895	ns
	60	1.609	1.893	ns
	120	1.607	1.89	ns
True differential	None	1.623	1.91	ns
	20	1.637	1.926	ns
	30	1.63	1.918	ns
	40	1.626	1.914	ns
	60	1.622	1.91	ns
	120	1.619	1.905	ns

Table 138 • **DDR3/SSTL15 Transmitter Characteristics (Output and Tristate Buffers)**

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		
	–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
DDR3 Reduced Drive/SSTL15 Class I (for DDRIO I/O Bank)											
Single-ended	2.533	2.98	2.522	2.967	2.523	2.968	2.427	2.855	2.428	2.856	ns
Differential	2.555	3.005	3.073	3.615	3.073	3.615	2.416	2.843	2.416	2.843	ns
DDR3 Full Drive/SSTL15 Class II (for DDRIO I/O Bank)											
Single-ended	2.53	2.977	2.514	2.958	2.516	2.96	2.422	2.849	2.425	2.852	ns
Differential	2.552	3.002	2.591	3.048	2.59	3.047	2.882	3.391	2.881	3.39	ns

Table 162 • **LVDS DC Output Voltage Specification**

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V_{OH}	1.25	1.425	1.6	V
DC output logic low	V_{OL}	0.9	1.075	1.25	V

Table 163 • **LVDS DC Differential Voltage Specification**

Parameter	Symbol	Min	Typ	Max	Unit
Differential output voltage swing	V_{OD}	250	350	450	mV
Output common mode voltage	V_{OCM}	1.125	1.25	1.375	V
Input common mode voltage	V_{ICM}	0.05	1.25	2.35	V
Input differential voltage	V_{ID}	100	350	600	mV

Table 164 • **LVDS Minimum and Maximum AC Switching Speed**

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	D_{MAX}	535	Mbps	AC loading: 12 pF / 100 Ω differential load
Maximum data rate (for MSIOD I/O bank) no pre-emphasis	D_{MAX}	620	Mbps	AC loading: 10 pF / 100 Ω differential load
		700	Mbps	AC loading: 2 pF / 100 Ω differential load

Table 165 • **LVDS AC Impedance Specifications**

Parameter	Symbol	Typ	Max	Unit
Termination resistance	RT	100		Ω

Table 166 • **LVDS AC Test Parameter Specifications**

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	Cross point	V
Resistance for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH}, T_{ZL}, T_{HZ}, T_{LZ})	C_{ENT}	5	pF

LVDS25 AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 2.375 V

Table 167 • **LVDS25 Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

	T_{PY}		
On-Die Termination (ODT)	**–1**	**–Std**	**Unit**
None	2.774	3.263	ns
100	2.775	3.264	ns

Table 191 • M-LVDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)

	T_{PY}		
On-Die Termination (ODT)	**–1**	**–Std**	**Unit**
None	2.495	2.934	ns
100	2.495	2.935	ns

Table 192 • M-LVDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		
–1	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**–1**	**–Std**	**Unit**
2.258	2.656	2.348	2.762	2.334	2.746	2.123	2.497	2.125	2.5	ns

2.3.7.4 Mini-LVDS

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

Mini-LVDS Minimum and Maximum Input and Output Levels

Table 193 • Mini-LVDS Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	2.375	2.5	2.625	V

Table 194 • Mini-LVDS DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC Input voltage	V_I	0	2.925	V

Table 195 • Mini-LVDS DC Output Voltage Specification

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V_{OH}	1.25	1.425	1.6	V
DC output logic low	V_{OL}	0.9	1.075	1.25	V

Table 196 • Mini-LVDS DC Differential Voltage Specification

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing	V_{OD}	300	600	mV
Output common mode voltage	V_{OCM}	1	1.4	V
Input common mode voltage	V_{ICM}	0.3	1.2	V
Input differential voltage	V_{ID}	100	600	mV

Table 197 • Mini-LVDS Minimum and Maximum AC Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	D_{MAX}	520	Mbps	AC loading: 2 pF / 100 Ω differential load
Maximum data rate (for MSIOD I/O bank)	D_{MAX}	700	Mbps	AC loading: 2 pF / 100 Ω differential load

Table 215 • LVPECL DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC input voltage	V_I	0	3.45	V

Table 216 • LVPECL DC Differential Voltage Specification

Parameter	Symbol	Min	Typ	Max	Unit
Input common mode voltage	V_{ICM}	0.3		2.8	V
Input differential voltage	V_{IDIFF}	100	300	1,000	mV

Table 217 • LVPECL Minimum and Maximum AC Switching Speeds

Parameter	Symbol	Max	Unit
Maximum data rate	D_{MAX}	900	Mbps

AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 2.375 V.

Table 218 • LVPECL Receiver Characteristics for MSIO I/O Bank

	T_{PY}		
On-Die Termination (ODT)	–1	–Std	Unit
None	2.572	3.025	ns
100	2.569	3.023	ns

2.3.8 I/O Register Specifications

This section describes input and output register specifications.

2.3.8.1 Input Register

Figure 6 • Timing Model for Input Register

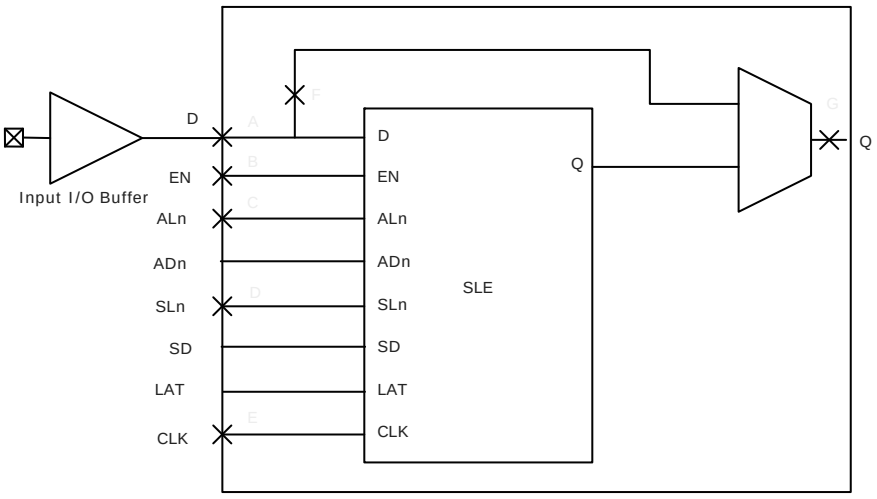


Table 222 • **Output DDR Propagation Delays *(continued)***

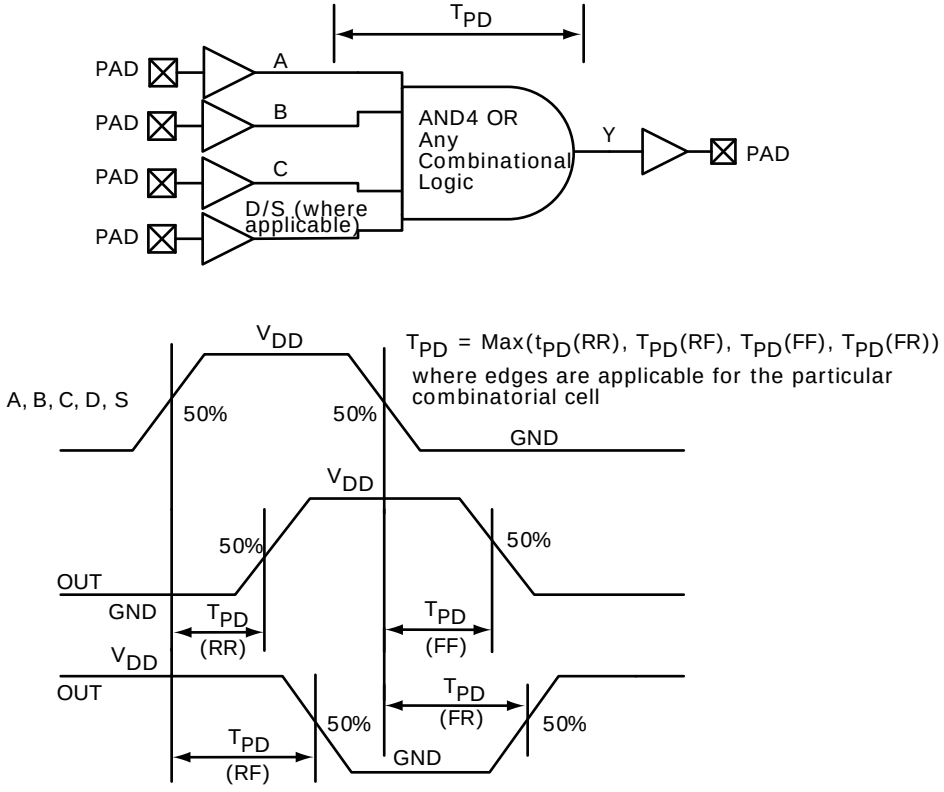
Symbol	Description	Measuring Nodes (from, to)	–1	–Std	Unit
$T_{DDROWAL}$	Asynchronous load minimum pulse width for output DDR	C, C	0.304	0.357	ns
$T_{DDROCKMPWH}$	Clock minimum pulse width high for the output DDR	E, E	0.075	0.088	ns
$T_{DDROCKMPWL}$	Clock minimum pulse width low for the output DDR	E, E	0.159	0.187	ns

2.3.10 Logic Element Specifications

2.3.10.1 4-input LUT (LUT-4)

The IGLOO2 and SmartFusion2 SoC FPGAs offer a fully permutable 4-input LUT. In this section, timing characteristics are presented for a sample of the library. For more details, see *SmartFusion2 and IGLOO2 Macro Library Guide*.

Figure 14 • **LUT-4**



2.3.11 Global Resource Characteristics

The IGLOO2 and SmartFusion2 SoC FPGA devices offer a powerful, low skew global routing network which provides an effective clock distribution throughout the FPGA fabric. See *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide* for the positions of various global routing resources.

The following table lists the 150 device global resources in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 225 • **150 Device Global Resource**

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Input low delay for global clock	T_{RCKL}	0.83	0.911	0.831	0.913	ns
Input high delay for global clock	T_{RCKH}	1.457	1.588	1.715	1.869	ns
Maximum skew for global clock	T_{RCKSW}		0.131		0.154	ns

The following table lists the 090 device global resources in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 226 • **090 Device Global Resource**

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Input low delay for global clock	T_{RCKL}	0.835	0.888	0.833	0.886	ns
Input high delay for global clock	T_{RCKH}	1.405	1.489	1.654	1.752	ns
Maximum skew for global clock	T_{RCKSW}		0.084		0.098	ns

The following table lists the 050 device global resources in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 227 • **050 Device Global Resource**

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Input low delay for global clock	T_{RCKL}	0.827	0.897	0.826	0.896	ns
Input high delay for global clock	T_{RCKH}	1.419	1.53	1.671	1.8	ns
Maximum skew for global clock	T_{RCKSW}		0.111		0.129	ns

The following table lists the 025 device global resources in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 228 • **025 Device Global Resource**

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Input low delay for global clock	T_{RCKL}	0.747	0.799	0.745	0.797	ns
Input high delay for global clock	T_{RCKH}	1.294	1.378	1.522	1.621	ns
Maximum skew for global clock	T_{RCKSW}		0.084		0.099	ns

Table 231 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1K × 18 *(continued)***

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Block select hold time	T_{BLKHD}	0.216		0.254		ns
Block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		1.529		1.799	ns
Block select minimum pulse width	T_{BLKMPW}	0.186		0.219		ns
Read enable setup time	T_{RDESU}	0.449		0.528		ns
Read enable hold time	T_{RDEHD}	0.167		0.197		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	T_{R2Q}	–	1.506	–	1.772	ns
Asynchronous reset removal time	T_{RSTREM}	0.506		0.595		ns
Asynchronous reset recovery time	T_{RSTREC}	0.004		0.005		ns
Asynchronous reset minimum pulse width	T_{RSTMPW}	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	T_{SRSTSU}	0.226		0.265		ns
Synchronous reset hold time	T_{SRSTHD}	0.036		0.043		ns
Write enable setup time	T_{WESU}	0.39		0.458		ns
Write enable hold time	T_{WEHD}	0.242		0.285		ns
Maximum frequency	F_{MAX}		400		340	MHz

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 2K × 9 in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 232 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9**

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Clock period	T_{CY}	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	T_{PLCY}	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register	T_{CLK2Q}		0.334		0.393	ns
Read access time without pipeline register			2.273		2.674	ns
Access time with feed-through write timing			1.529		1.799	ns

Table 238 • **µSRAM (RAM64x16) in 64 × 16 Mode *(continued)***

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.115		0.135		ns
Write input data hold time	T_{DINCHD}	0.15		0.177		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	–0.026		–0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

The following table lists the µSRAM in 128 × 9 mode in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 239 • **µSRAM (RAM128x9) in 128 × 9 Mode**

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.266		0.313	ns
Read access time without pipeline register			1.677		1.973	ns
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode		1.856		2.184		ns
Read address hold time in synchronous mode	T_{ADDRHD}	0.091		0.107		ns
Read address hold time in asynchronous mode		–0.778		–0.915		ns
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	–0.65		–0.765		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.036		2.396	ns

The following table lists the µSRAM in 256 × 4 mode in worst commercial-case conditions when T_J = 85 °C, V_{DD} = 1.14 V.

Table 241 • **µSRAM (RAM256x4) in 256 × 4 Mode**

		–1		–Std		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.27		0.31	ns
Read access time without pipeline register			1.75		2.06	ns
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode		1.931		2.272		ns
Read address hold time in synchronous mode	T_{ADDRHD}	0.121		0.142		ns
Read address hold time in asynchronous mode		–0.65		–0.76		ns
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	–0.65		–0.77		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.09		2.46	ns
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	–0.02		–0.03		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.83		0.98	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.101		0.118		ns
Write input data hold time	T_{DINCHD}	0.137		0.161		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns

Table 277 • **Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz)** ***(continued)***

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Startup time (with regard to stable oscillator output)	SUXTAL			0.8	ms	005, 010, 025, and 050 devices
				1.0	ms	090 and 150 devices

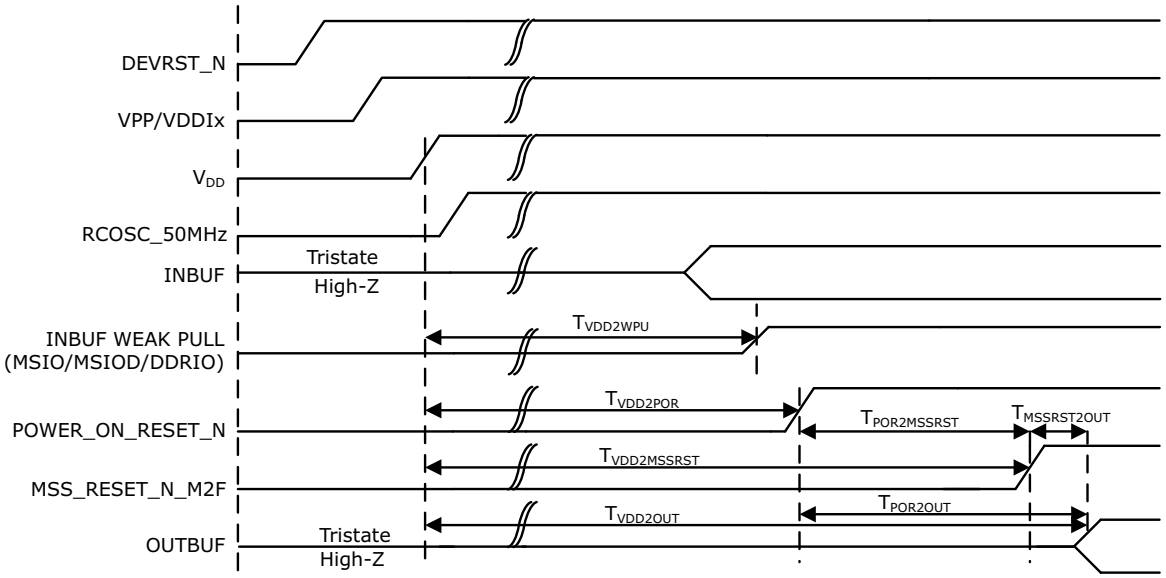
Table 278 • **Electrical Characteristics of the Crystal Oscillator – Medium Gain Mode (2 MHz)**

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Operating frequency	FXTAL		2		MHz	
Accuracy	ACCXTAL			0.00105	%	050 devices
				0.003	%	005, 010, 025, 090, and 150 devices
				0.004	%	060 devices
Output duty cycle	CYCXTAL		49–51	47–53	%	
Output period jitter (peak to peak)	JITPERXTAL		1	5	ns	
Output cycle to cycle jitter (peak to peak)	JITCYCXTAL		1	5	ns	
Operating current	IDYNXTAL		0.3		mA	
Input logic level high	VIHXTAL	0.9 V_{PP}			V	
Input logic level low	VILXTAL			0.1 V_{PP}	V	
Startup time (with regard to stable oscillator output)	SUXTAL			4.5	ms	010 and 050 devices
				5	ms	005 and 025 devices
				7	ms	090 and 150 devices

Table 279 • **Electrical Characteristics of the Crystal Oscillator – Low Gain Mode (32 kHz)**

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Operating frequency	FXTAL		32		kHz	
Accuracy	ACCXTAL			0.004	%	005, 010, 025, 050, 060, and 090 devices
				0.005	%	150 devices
Output duty cycle	CYCXTAL		49–51	47–53	%	
Output period jitter (peak to peak)	JITPERXTAL		150	300	ns	
Output cycle to cycle jitter (peak to peak)	JITCYCXTAL		150	300	ns	
Operating current	IDYNXTAL		0.044		mA	010 and 050 devices
			0.060		mA	005, 025, 060, 090, and 150 devices
Input logic level high	VIHXTAL	0.9 V_{PP}			V	
Input logic level low	VILXTAL			0.1 V_{PP}	V	
Startup time (with regard to stable oscillator output)	SUXTAL			115	ms	005, 025, 050, 090, and 150 devices
				126	ms	010 devices

Figure 17 • **Power-up to Functional Timing Diagram for SmartFusion2**



The following table lists the IGLOO2 power-up to functional times in worst-case industrial conditions when T_J = 100 °C, V_{DD} = 1.14 V.

Table 289 • **Power-up to Functional Times for IGLOO2**

				Maximum Power-up to Functional Time for IGLOO2 (uS)						
Symbol	**From**	**To**	**Description**	**005**	**010**	**025**	**050**	**060**	**090**	**150**
$T_{POR2OUT}$	POWER_ON_RESET_N	Output available at I/O	Fabric to output	114	114	114	113	114	114	114
$T_{VDD2OUT}$	V_{DD}	Output available at I/O	V_{DD} at its minimum threshold level to output	2587	2600	2607	2558	2591	2600	2699
$T_{VDD2POR}$	V_{DD}	POWER_ON_RESET_N	V_{DD} at its minimum threshold level to fabric	2474	2486	2493	2445	2477	2486	2585
$T_{VDD2WPU}$	DEVRST_N	DDRIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2500	2487	2509	2475	2507	2519	2617
	DEVRST_N	MSIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2504	2491	2510	2478	2517	2525	2620
	DEVRST_N	MSIOD Inbuf weak pull	DEVRST_N to Inbuf weak pull	2479	2468	2493	2458	2486	2499	2595

Note: For more information about power-up times, see *UG0448: IGLOO2 FPGA High Performance Memory Subsystem User Guide*.