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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 12084 |
| Total RAM Bits | 933888 |
| Number of I/O | 138 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 256-LFBGA |
| Supplier Device Package | 256-FPBGA (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m2gl010t-vfg256i |

# Tables

# 1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 11.0

The following is a summary of the changes in revision 11.0 of this document.

- Updated Table 24, page 22 with minimum and maximum values for input current low and high (SAR 73114 and 80314).
- Added Non-Deterministic Random Bit Generator (NRBG) Characteristics, page 106 (SAR 73114 and 79517).
- Added 060 device in Table 282, page 110 (SAR 79860).
- Added DEVRST_N to Functional Times, page 116 (SAR 73114).
- Added Cryptographic Block Characteristics, page 106 (SAR 73114 and 79516).
- Update Table 296, page 121 with VTX-AMP details (SAR 81756).
- Update note in Table 297, page 122 (SAR 74570 and 80677).
- Update Table 298, page 122 with generic EPCS details (SAR 75307).
- Added Table 308, page 129 (SAR 50424).

## 1.2 Revision 10.0

The following is a summary of the changes in revision 10.0 of this document.

- The Surge Current on VDD during DEVRST_B Assertion and Surge Current on VDD during Digest Check using System Services tables were deleted and added reference to *AC393: Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs Application Note*. (SAR 76865 and 76623).
- Added 060 device in Table 4, page 6 (SAR 76383).
- Updated Table 24, page 22 for ramp time input (SAR 72103).
- Added 060 device details in Table 284, page 112 (SAR 74927).
- Updated Table 290, page 116 for name change (SAR 74925).
- Updated Table 283, page 111 for 060 FG676 Package details (SAR 78849).
- Updated Table 305, page 126 for SmartFusion2 and Table 310, page 129 for IGLOO2 for SPI timing and Fmax (SAR 56645, 75331).
- Updated Table 293, page 119 for Flash*Freeze entry and exit times (SAR 75329, 75330).
- Updated Table 297, page 122 for RX-CID information (SAR 78271).
- Added Table 8, page 8 and Figure 1, page 9 (SAR 78932).
- Updated Table 223, page 76 for timing characteristics and Table 224, page 77(SAR 75998).
- Added SRAM PUF, page 105 (SAR 64406).
- Added a footnote on digest cycle in Table 5, page 7 (SAR 79812).

## 1.3 Revision 9.0

The following is a summary of the changes in revision 9.0 of this document.

- Added a note in Table 5, page 7 (SAR 71506).
- Added a note in Table 6, page 8 (SAR 74616).
- Added a note in Figure 3, page 17 (SAR 71506).
- Updated Quiescent Supply Current for 060 in Table 11, page 12 and Table 12, page 13 (SAR 74483).
- Updated programming currents for 060 in Table 13, page 13, Table 14, page 13, and Table 15, page 14.
- Added DEVRST_B assertion tables (SAR 74708).
- Updated I/O speeds for LVDS 3.3 V in Table 18, page 19 and Table 21, page 20 (SAR 69829).
- Updated Table 24, page 22 (SAR 69418).
- Updated Table 25, page 22, Table 26, page 23, Table 27, page 23 (SAR 74570).
- Updated all AC/DC table to link to the Input Capacitance, Leakage Current, and Ramp Time, page 22 for reference (SAR 69418).

## 2.3.2 Power Consumption

The following sections describe the power consumptions of the devices.

### 2.3.2.1 Quiescent Supply Current

***Table 10 •*** **Quiescent Supply Current Characteristics**

| | Modes and Configurations | |
|---|---|---|
| **Power Supplies/Blocks** | **Non-Flash*Freeze** | **Flash*Freeze** |
| FPGA Core | On | Off |
| $V_{DD}$/SERDES_[01]_VDD[1] | On | On |
| $V_{PP}$/$V_{PPNVM}$ | On | On |
| HPMS_MDDR_PLL_VDDA/FDDR_PLL_VDDA/ CCC_XX[01]_PLL_VDDA/PLL0_PLL1_HPMS_MDDR_VDDA | 0 V | 0 V |
| SERDES_[01]_PLL_VDDA[2] | 0 V | 0 V |
| SERDES_[01]_L[0123]_VDDAPLL/VDD_2V5[2] | On | On |
| SERDES_[01]_L[0123]_VDDAIIO[2] | On | On |
| $V_{DDIx}$[3, 4] | On | On |
| $V_{REFx}$ | On | On |
| MSSDDR CLK | 32 kHz | 32 kHz |
| RAM | On | Sleep state |
| System controller | 50 MHz | 50 MHz |
| 50 MHz oscillator (enable/disable) | Enable | Disabled |
| 1 MHz oscillator (enable/disable) | Disabled | Disabled |
| Crystal oscillator (enable/disable) | Disabled | Disabled |

1. SERDES_[01]_VDD Power Supply is shorted to $V_{DD}$.
2. SerDes and DDR blocks to be unused.
3. $V_{DDIx}$ has been set to ON for test conditions as described. Banks on the east side should always be powered with the appropriate $V_{DDI}$ bank supplies. For details on bank power supplies, see “Recommendation for Unused Bank Supplies” table in the *AC393: SmartFusion2 and IGLOO2 Board Design Guidelines Application Note*.
4. No Differential (that is to say, LVDS) I/Os or ODT attributes to be used.

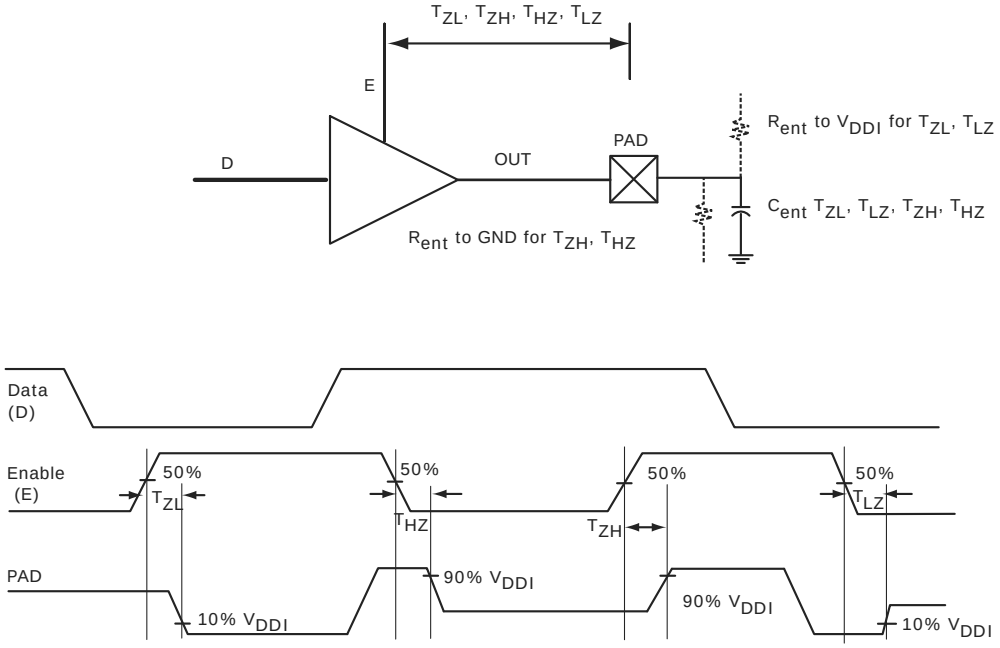
***Table 11 •*** **SmartFusion2 and IGLOO2 Quiescent Supply Current ($V_{DD}$ = 1.2 V) – Typical Process**

| Symbol | Modes | 005 | 010 | 025 | 050 | 060 | 090 | 150 | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| IDC1 | Non-Flash*Freeze | 6.2 | 6.9 | 8.9 | 13.1 | 15.3 | 15.4 | 27.5 | mA | Typical ($T_J$ = 25 °C) |
| | | 24.0 | 28.4 | 40.6 | 67.8 | 80.6 | 81.4 | 144.7 | mA | Commercial ($T_J$ = 85 °C) |
| | | 35.2 | 41.9 | 60.5 | 102.1 | 121.4 | 122.6 | 219.1 | mA | Industrial ($T_J$ = 100 °C) |

### 2.3.5.3 Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The following figure shows the methodology of characterization illustrated by the enable path test point.

***Figure 5 •*** **Tristate Buffer for Enable Path Test Point**




### 2.3.5.4 I/O Speeds

This section describes the maximum data rate summary of I/O in worst-case industrial conditions. See the individual I/O standards for operating conditions.

***Table 18 •*** **Maximum Data Rate Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions**

| I/O | MSIO | MSIOD | DDRIO | Unit |
|---|---|---|---|---|
| PCI 3.3 V | 630 | | | Mbps |
| LVTTL 3.3 V | 600 | | | Mbps |
| LVCMOS 3.3 V | 600 | | | Mbps |
| LVCMOS 2.5 V | 410 | 420 | 400 | Mbps |
| LVCMOS 1.8 V | 295 | 400 | 400 | Mbps |
| LVCMOS 1.5 V | 160 | 220 | 235 | Mbps |
| LVCMOS 1.2 V | 120 | 160 | 200 | Mbps |
| LPDDR-LVCMOS 1.8 V mode | | | 400 | Mbps |

***Table 34 •*** **LVTTL/LVCMOS 3.3 V AC Test Parameter Specifications (Applicable to MSIO I/O Bank Only)**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | 1.4 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | pF |

***Table 35 •*** **LVTTL/LVCMOS 3.3 V Transmitter Drive Strength Specifications for MSIO I/O Bank**

| Output Drive Selection | $V_{OH}$ (V) | $V_{OL}$ (V) | IOH (at $V_{OH}$) mA | IOL (at $V_{OL}$) mA |
|---|---|---|---|---|
| 2 mA | $V_{DDI}$ – 0.4 | 0.4 | 2 | 2 |
| 4 mA | $V_{DDI}$ – 0.4 | 0.4 | 4 | 4 |
| 8 mA | $V_{DDI}$ – 0.4 | 0.4 | 8 | 8 |
| 12 mA | $V_{DDI}$ – 0.4 | 0.4 | 12 | 12 |
| 16 mA | $V_{DDI}$ – 0.4 | 0.4 | 16 | 16 |
| 20 mA | $V_{DDI}$ – 0.4 | 0.4 | 20 | 20 |

**Note:** For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

**AC Switching Characteristics**

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 3.0 V

***Table 36 •*** **LVTTL/LVCMOS 3.3 V Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

| On-Die Termination (ODT) | $T_{PY}$ | | $T_{PYS}$ | | Unit |
|---|---|---|---|---|---|
| | –1 | –Std | –1 | –Std | |
| None | 2.262 | 2.663 | 2.289 | 2.695 | ns |

***Table 37 •*** **LVTTL/LVCMOS 3.3 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | |
| 2 mA | Slow | 3.192 | 3.755 | 3.47 | 4.083 | 2.969 | 3.494 | 1.856 | 2.183 | 3.337 | 3.926 | ns |
| 4 mA | Slow | 2.331 | 2.742 | 2.673 | 3.145 | 2.526 | 2.973 | 3.034 | 3.569 | 4.451 | 5.236 | ns |
| 8 mA | Slow | 2.135 | 2.511 | 2.33 | 2.741 | 2.297 | 2.703 | 4.532 | 5.331 | 4.825 | 5.676 | ns |
| 12 mA | Slow | 2.052 | 2.414 | 2.107 | 2.479 | 2.162 | 2.544 | 5.75 | 6.764 | 5.445 | 6.406 | ns |
| 16 mA | Slow | 2.062 | 2.425 | 2.072 | 2.438 | 2.145 | 2.525 | 5.993 | 7.05 | 5.625 | 6.618 | ns |
| 20 mA | Slow | 2.148 | 2.527 | 1.999 | 2.353 | 2.088 | 2.458 | 6.262 | 7.367 | 5.876 | 6.913 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

### 2.3.5.7 2.5 V LVCMOS

LVCMOS 2.5 V is a general standard for 2.5 V applications and is supported in IGLOO2 FPGA and SmartFusion2 SoC FPGAs that are in compliance with the JEDEC specification JESD8-5A.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

***Table 38 •*** **LVCMOS 2.5 V DC Recommended DC Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 2.375 | 2.5 | 2.625 | V |

***Table 39 •*** **LVCMOS 2.5 V DC Input Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high (for MSIOD and DDRIO I/O banks) | $V_{IH}$ (DC) | 1.7 | 2.625 | V |
| DC input logic high (for MSIO I/O bank) | $V_{IH}$ (DC) | 1.7 | 3.45 | V |
| DC input logic low | $V_{IL}$ (DC) | –0.3 | 0.7 | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

***Table 40 •*** **LVCMOS 2.5 V DC Output Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC output logic high | $V_{OH}$[1] | $V_{DDI}$ – 0.4 | – | V |
| DC output logic low | $V_{OL}$[2] | | 0.4 | V |

1. The VOH/VOL test points selected ensure compliance with LVCMOS 2.5 V JEDEC8-5A requirements.

***Table 41 •*** **LVCMOS 2.5 V AC Minimum and Maximum Switching Speed**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for DDRIO I/O bank) | $D_{MAX}$ | 400 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 410 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIOD I/O bank) | $D_{MAX}$ | 420 | Mbps | AC loading: 17 pF load, maximum drive/slew |

***Table 42 •*** **LVCMOS 2.5 V AC Calibrated Impedance Option**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | Rodt_cal | 75, 60, 50, 33, 25, 20 | Ω |

***Table 53 •*** **LVCMOS 1.8 V AC Calibrated Impedance Option**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | Rodt_cal | 75, 60, 50, 33, 25, 20 | Ω |

***Table 54 •*** **LVCMOS 1.8 V AC Test Parameter Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | 0.9 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2k | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | pF |

***Table 55 •*** **LVCMOS 1.8 V Transmitter Drive Strength Specifications**

| Output Drive Selection | | | $V_{OH}$ (V) | $V_{OL}$ (V) | IOH (at $V_{OH}$) | IOL (at $V_{OL}$) |
|---|---|---|---|---|---|---|
| MSIO I/O Bank | MSIOD I/O Bank | DDRIO I/O Bank | Min | Max | mA | mA |
| 2 mA | 2 mA | 2 mA | $V_{DDI}$ – 0.45 | 0.45 | 2 | 2 |
| 4 mA | 4 mA | 4 mA | $V_{DDI}$ – 0.45 | 0.45 | 4 | 4 |
| 6 mA | 6 mA | 6 mA | $V_{DDI}$ – 0.45 | 0.45 | 6 | 6 |
| 8 mA | 8 mA | 8 mA | $V_{DDI}$ – 0.45 | 0.45 | 8 | 8 |
| 10 mA | 10 mA | 10 mA | $V_{DDI}$ – 0.45 | 0.45 | 10 | 10 |
| 12 mA | | 12 mA | $V_{DDI}$ – 0.45 | 0.45 | 12 | 12 |
| | | 16 mA[1] | $V_{DDI}$ – 0.45 | 0.45 | 16 | 16 |

1. 16 mA drive strengths, all slews, meets LPDDR JEDEC electrical compliance.

### AC Switching Characteristics

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 1.71 V

***Table 56 •*** **LVCMOS 1.8 V Receiver Characteristics (Input Buffers)**

| | On-Die Termination (ODT) | $T_{PY}$ | | $T_{PYS}$ | | Unit |
|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | |
| **LVCMOS 1.8 V (for DDRIO I/O bank with Fixed Codes)** | None | 1.968 | 2.315 | 2.099 | 2.47 | ns |
| **LVCMOS 1.8 V (for MSIO I/O bank)** | None | 2.898 | 3.411 | 2.883 | 3.393 | ns |
| | 50 | 3.05 | 3.59 | 3.044 | 3.583 | ns |
| | 75 | 2.999 | 3.53 | 2.987 | 3.516 | ns |
| | 150 | 2.947 | 3.469 | 2.933 | 3.452 | ns |
| **LVCMOS 1.8 V (for MSIOD I/O bank)** | None | 2.611 | 3.071 | 2.598 | 3.057 | ns |
| | 50 | 2.775 | 3.264 | 2.775 | 3.265 | ns |
| | 75 | 2.72 | 3.2 | 2.712 | 3.19 | ns |
| | 150 | 2.666 | 3.137 | 2.655 | 3.123 | ns |

***Table 70 •*** **LVCMOS 1.5 V Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers) *(continued)***

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| 6 mA | Slow | 4.244 | 4.993 | 3.465 | 4.076 | 4.233 | 4.979 | 6.39 | 7.518 | 5.736 | 6.748 | ns |
| | Medium | 3.774 | 4.44 | 3.05 | 3.587 | 3.762 | 4.426 | 6.114 | 7.193 | 5.397 | 6.35 | ns |
| | Medium fast | 3.544 | 4.17 | 2.839 | 3.339 | 3.529 | 4.152 | 5.978 | 7.033 | 5.27 | 6.2 | ns |
| | Fast | 3.519 | 4.14 | 2.82 | 3.317 | 3.504 | 4.122 | 5.965 | 7.017 | 5.259 | 6.187 | ns |
| 8 mA | Slow | 4.099 | 4.823 | 3.311 | 3.894 | 4.087 | 4.807 | 6.584 | 7.746 | 5.854 | 6.888 | ns |
| | Medium | 3.656 | 4.301 | 2.927 | 3.443 | 3.642 | 4.284 | 6.311 | 7.425 | 5.553 | 6.533 | ns |
| | Medium fast | 3.437 | 4.044 | 2.731 | 3.213 | 3.42 | 4.023 | 6.182 | 7.273 | 5.435 | 6.394 | ns |
| | Fast | 3.41 | 4.012 | 2.715 | 3.193 | 3.393 | 3.991 | 6.178 | 7.269 | 5.425 | 6.383 | ns |
| 10 mA | Slow | 4.029 | 4.74 | 3.238 | 3.809 | 4.015 | 4.723 | 6.732 | 7.921 | 5.965 | 7.018 | ns |
| | Medium | 3.601 | 4.237 | 2.867 | 3.372 | 3.586 | 4.218 | 6.473 | 7.615 | 5.669 | 6.669 | ns |
| | Medium fast | 3.384 | 3.981 | 2.672 | 3.143 | 3.365 | 3.958 | 6.351 | 7.471 | 5.55 | 6.529 | ns |
| | Fast | 3.357 | 3.949 | 2.655 | 3.123 | 3.338 | 3.927 | 6.345 | 7.464 | 5.54 | 6.518 | ns |
| 12 mA | Slow | 3.974 | 4.675 | 3.196 | 3.759 | 3.958 | 4.656 | 6.842 | 8.049 | 6.068 | 7.139 | ns |
| | Medium | 3.55 | 4.176 | 2.827 | 3.326 | 3.534 | 4.157 | 6.584 | 7.746 | 5.751 | 6.766 | ns |
| | Medium fast | 3.345 | 3.935 | 2.638 | 3.103 | 3.325 | 3.911 | 6.488 | 7.633 | 5.641 | 6.637 | ns |
| | Fast | 3.316 | 3.902 | 2.621 | 3.083 | 3.297 | 3.878 | 6.486 | 7.63 | 5.626 | 6.619 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

***Table 71 •*** **LVCMOS 1.5 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| 2 mA | Slow | 4.423 | 5.203 | 5.397 | 6.35 | 5.686 | 6.69 | 5.609 | 6.599 | 5.561 | 6.542 | ns |
| 4 mA | Slow | 4.05 | 4.765 | 4.503 | 5.298 | 4.92 | 5.788 | 7.358 | 8.657 | 6.525 | 7.677 | ns |
| 6 mA | Slow | 4.081 | 4.801 | 4.259 | 5.012 | 4.699 | 5.528 | 7.659 | 9.011 | 6.709 | 7.893 | ns |
| 8 mA | Slow | 4.234 | 4.98 | 4.068 | 4.786 | 4.521 | 5.319 | 8.218 | 9.668 | 7.05 | 8.294 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

***Table 82 •*** **LVCMOS 1.2 V Receiver Characteristics for MSIOD I/O Bank (Input Buffers)**

| | $T_{PY}$ | | $T_{PYS}$ | | |
|---|---|---|---|---|---|
| **On-Die Termination (ODT)** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| None | 4.154 | 4.887 | 4.114 | 4.84 | ns |
| 50 | 6.918 | 8.139 | 6.806 | 8.008 | ns |
| 75 | 5.613 | 6.603 | 5.533 | 6.509 | ns |
| 150 | 4.716 | 5.549 | 4.657 | 5.479 | ns |

***Table 83 •*** **LVCMOS 1.2 V Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)**

| **Output Drive Selection** | **Slew Control** | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| 2 mA | Slow | 6.713 | 7.897 | 5.362 | 6.308 | 6.723 | 7.909 | 7.233 | 8.51 | 6.375 | 7.499 | ns |
| | Medium | 5.912 | 6.955 | 4.616 | 5.43 | 5.915 | 6.959 | 6.887 | 8.102 | 6.009 | 7.069 | ns |
| | Medium fast | 5.5 | 6.469 | 4.231 | 4.978 | 5.5 | 6.471 | 6.672 | 7.849 | 5.835 | 6.865 | ns |
| | Fast | 5.462 | 6.426 | 4.194 | 4.935 | 5.463 | 6.427 | 6.646 | 7.819 | 5.828 | 6.857 | ns |
| 4 mA | Slow | 6.109 | 7.186 | 4.708 | 5.539 | 6.098 | 7.174 | 8.005 | 9.418 | 7.033 | 8.274 | ns |
| | Medium | 5.355 | 6.299 | 4.034 | 4.746 | 5.338 | 6.28 | 7.637 | 8.985 | 6.672 | 7.849 | ns |
| | Medium fast | 4.953 | 5.826 | 3.685 | 4.336 | 4.932 | 5.802 | 7.44 | 8.752 | 6.499 | 7.646 | ns |
| | Fast | 4.911 | 5.777 | 3.658 | 4.303 | 4.89 | 5.754 | 7.427 | 8.737 | 6.488 | 7.632 | ns |
| 6 mA | Slow | 5.89 | 6.929 | 4.506 | 5.301 | 5.874 | 6.911 | 8.337 | 9.808 | 7.315 | 8.605 | ns |
| | Medium | 5.176 | 6.089 | 3.862 | 4.543 | 5.155 | 6.065 | 7.986 | 9.394 | 6.943 | 8.168 | ns |
| | Medium fast | 4.792 | 5.637 | 3.523 | 4.145 | 4.765 | 5.606 | 7.808 | 9.186 | 6.775 | 7.97 | ns |
| | Fast | 4.754 | 5.593 | 3.486 | 4.101 | 4.728 | 5.563 | 7.777 | 9.149 | 6.769 | 7.963 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

***Table 84 •*** **LVCMOS 1.2 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

| **Output Drive Selection** | **Slew Control** | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| 2 mA | Slow | 6.746 | 7.937 | 7.458 | 8.774 | 8.172 | 9.614 | 9.867 | 11.608 | 8.393 | 9.874 | ns |
| 4 mA | Slow | 7.068 | 8.315 | 6.678 | 7.857 | 7.474 | 8.793 | 10.986 | 12.924 | 9.043 | 10.638 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

**AC Switching Characteristics**

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 3.0 V

***Table 91 •*** **PCI/PCIX AC Switching Characteristics for Receiver for MSIO I/O Bank (Input Buffers)**

| | $T_{PY}$ | | $T_{PYS}$ | | |
|---|---|---|---|---|---|
| **On-Die Termination (ODT)** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| None | 2.229 | 2.623 | 2.238 | 2.633 | ns |

***Table 92 •*** **PCI/PCIX AC switching Characteristics for Transmitter for MSIO I/O Bank (Output and Tristate Buffers)**

| $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| 2.146 | 2.525 | 2.043 | 2.404 | 2.084 | 2.452 | 6.095 | 7.171 | 5.558 | 6.539 | ns |

## 2.3.6 Memory Interface and Voltage Referenced I/O Standards

This section describes High-Speed Transceiver Logic (HSTL) memory interface and voltage reference I/O standards.

### 2.3.6.1 High-Speed Transceiver Logic (HSTL)

The HSTL standard is a general purpose high-speed bus standard sponsored by IBM (EIA/JESD8-6). IGLOO2 FPGA and SmartFusion2 SoC FPGA devices support two classes of the 1.5 V HSTL. These differential versions of the standard require a differential amplifier input buffer and a push-pull output buffer.

**Minimum and Maximum DC/AC Input and Output Levels Specification (Applicable to DDRIO Bank Only)**

***Table 93 •*** **HSTL Recommended DC Operating Conditions**

| **Parameter** | **Symbol** | **Min** | **Typ** | **Max** | **Unit** |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 1.425 | 1.5 | 1.575 | V |
| Termination voltage | $V_{TT}$ | 0.698 | 0.750 | 0.803 | V |
| Input reference voltage | $V_{REF}$ | 0.698 | 0.750 | 0.803 | V |

***Table 94 •*** **HSTL DC Input Voltage Specification**

| **Parameter** | **Symbol** | **Min** | **Max** | **Unit** |
|---|---|---|---|---|
| DC input logic high | $V_{IH}$ (DC) | $V_{REF}$ + 0.1 | 1.575 | V |
| DC input logic low | $V_{IL}$ (DC) | –0.3 | $V_{REF}$ – 0.1 | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

***Table 100 •*** **HSTL AC Test Parameter Specification**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | 0.75 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Reference resistance for data test path for HSTL15 Class I ($T_{DP}$) | RTT_TEST | 50 | Ω |
| Reference resistance for data test path for HSTL15 Class II ($T_{DP}$) | RTT_TEST | 25 | Ω |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | pF |

**AC Switching Characteristics**

Worst-case commercial conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, worst-case $V_{DDI}$.

***Table 101 •*** **HSTL Receiver Characteristics for DDRIO I/O Bank with Fixed Code (Input Buffers)**

| | | $T_{PY}$ | | |
|---|---|---|---|---|
| | **On-Die Termination (ODT)** | **–1** | **–Std** | **Unit** |
| Pseudo differential | None | 1.605 | 1.888 | ns |
| | 47.8 | 1.614 | 1.898 | ns |
| True differential | None | 1.622 | 1.909 | ns |
| | 47.8 | 1.628 | 1.916 | ns |

***Table 102 •*** **HSTL Transmitter Characteristics for DDRIO I/O Bank (Output and Tristate Buffers)**

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| **HSTL Class I** | | | | | | | | | | | |
| Single-ended | 2.6 | 3.059 | 2.514 | 2.958 | 2.514 | 2.958 | 2.431 | 2.86 | 2.431 | 2.86 | ns |
| Differential | 2.621 | 3.083 | 2.648 | 3.115 | 2.647 | 3.113 | 2.925 | 3.442 | 2.923 | 3.44 | ns |
| **HSTL Class II** | | | | | | | | | | | |
| Single-ended | 2.511 | 2.954 | 2.488 | 2.927 | 2.49 | 2.93 | 2.409 | 2.833 | 2.411 | 2.836 | ns |
| Differential | 2.528 | 2.974 | 2.552 | 3.003 | 2.551 | 3.001 | 2.897 | 3.409 | 2.896 | 3.408 | ns |

### *2.3.6.2 Stub-Series Terminated Logic*

Stub-Series Terminated Logic (SSTL) for 2.5 V (SSTL2), 1.8 V (SSTL18), and 1.5 V (SSTL15) is supported in IGLOO2 and SmartFusion2 SoC FPGAs. SSTL2 is defined by JEDEC standard JESD8-9B and SSTL18 is defined by JEDEC standard JESD8-15. IGLOO2 SSTL I/O configurations are designed to meet double data rate standards DDR/2/3 for general purpose memory buses. Double data rate standards are designed to meet their JEDEC specifications as defined by JEDEC standard JESD79F for DDR, JEDEC standard JESD79-2F for DDR, JEDEC standard JESD79-3D for DDR3, and JEDEC standard JESD209A for LPDDR.

### 2.3.7.2 B-LVDS

Bus LVDS (B-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

***Table 173 •*** **B-LVDS Recommended DC Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 2.375 | 2.5 | 2.625 | V |

***Table 174 •*** **B-LVDS DC Input Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input voltage | $V_I$ | 0 | 2.925 | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

***Table 175 •*** **B-LVDS DC Output Voltage Specification (for MSIO I/O Bank Only)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DC output logic high | $V_{OH}$ | 1.25 | 1.425 | 1.6 | V |
| DC output logic low | $V_{OL}$ | 0.9 | 1.075 | 1.25 | V |

***Table 176 •*** **B-LVDS DC Differential Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Differential output voltage swing (for MSIO I/O bank only) | $V_{OD}$ | 65 | 460 | mV |
| Output common mode voltage (for MSIO I/O bank only) | $V_{OCM}$ | 1.1 | 1.5 | V |
| Input common mode voltage | $V_{ICM}$ | 0.05 | 2.4 | V |
| Input differential voltage | $V_{ID}$ | 0.1 | $V_{DDI}$ | V |

***Table 177 •*** **B-LVDS Minimum and Maximum AC Switching Speed**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 500 | Mbps | AC loading: 2 pF / 100 Ω differential load |

***Table 178 •*** **B-LVDS AC Impedance Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Termination resistance | $R_T$ | 27 | Ω |

***Table 179 •*** **B-LVDS AC Test Parameter Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | Cross point | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |

## 2.3.11 Global Resource Characteristics

The IGLOO2 and SmartFusion2 SoC FPGA devices offer a powerful, low skew global routing network which provides an effective clock distribution throughout the FPGA fabric. See *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide* for the positions of various global routing resources.

The following table lists the 150 device global resources in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 225 •*** **150 Device Global Resource**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Input low delay for global clock | $T_{RCKL}$ | 0.83 | 0.911 | 0.831 | 0.913 | ns |
| Input high delay for global clock | $T_{RCKH}$ | 1.457 | 1.588 | 1.715 | 1.869 | ns |
| Maximum skew for global clock | $T_{RCKSW}$ | | 0.131 | | 0.154 | ns |

The following table lists the 090 device global resources in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 226 •*** **090 Device Global Resource**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Input low delay for global clock | $T_{RCKL}$ | 0.835 | 0.888 | 0.833 | 0.886 | ns |
| Input high delay for global clock | $T_{RCKH}$ | 1.405 | 1.489 | 1.654 | 1.752 | ns |
| Maximum skew for global clock | $T_{RCKSW}$ | | 0.084 | | 0.098 | ns |

The following table lists the 050 device global resources in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 227 •*** **050 Device Global Resource**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Input low delay for global clock | $T_{RCKL}$ | 0.827 | 0.897 | 0.826 | 0.896 | ns |
| Input high delay for global clock | $T_{RCKH}$ | 1.419 | 1.53 | 1.671 | 1.8 | ns |
| Maximum skew for global clock | $T_{RCKSW}$ | | 0.111 | | 0.129 | ns |

The following table lists the 025 device global resources in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 228 •*** **025 Device Global Resource**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Input low delay for global clock | $T_{RCKL}$ | 0.747 | 0.799 | 0.745 | 0.797 | ns |
| Input high delay for global clock | $T_{RCKH}$ | 1.294 | 1.378 | 1.522 | 1.621 | ns |
| Maximum skew for global clock | $T_{RCKSW}$ | | 0.084 | | 0.099 | ns |

***Table 238 •*** **µSRAM (RAM64x16) in 64 × 16 Mode *(continued)***

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Read synchronous reset hold time | $T_{SRSTHD}$ | 0.061 | | 0.071 | | ns |
| Write clock period | $T_{CCY}$ | 4 | | 4 | | ns |
| Write clock minimum pulse width high | $T_{CCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Write clock minimum pulse width low | $T_{CCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Write block setup time | $T_{BLKCSU}$ | 0.404 | | 0.476 | | ns |
| Write block hold time | $T_{BLKCHD}$ | 0.007 | | 0.008 | | ns |
| Write input data setup time | $T_{DINCSU}$ | 0.115 | | 0.135 | | ns |
| Write input data hold time | $T_{DINCHD}$ | 0.15 | | 0.177 | | ns |
| Write address setup time | $T_{ADDRCSU}$ | 0.088 | | 0.104 | | ns |
| Write address hold time | $T_{ADDRCHD}$ | 0.128 | | 0.15 | | ns |
| Write enable setup time | $T_{WECSU}$ | 0.397 | | 0.467 | | ns |
| Write enable hold time | $T_{WECHD}$ | –0.026 | | –0.03 | | ns |
| Maximum frequency | $F_{MAX}$ | | 250 | | 250 | MHz |

The following table lists the µSRAM in 128 × 9 mode in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 239 •*** **µSRAM (RAM128x9) in 128 × 9 Mode**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Read clock period | $T_{CY}$ | 4 | | 4 | | ns |
| Read clock minimum pulse width high | $T_{CLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read clock minimum pulse width low | $T_{CLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock period | $T_{PLCY}$ | 4 | | 4 | | ns |
| Read pipeline clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.266 | | 0.313 | ns |
| Read access time without pipeline register | | | 1.677 | | 1.973 | ns |
| Read address setup time in synchronous mode | $T_{ADDRSU}$ | 0.301 | | 0.354 | | ns |
| Read address setup time in asynchronous mode | | 1.856 | | 2.184 | | ns |
| Read address hold time in synchronous mode | $T_{ADDRHD}$ | 0.091 | | 0.107 | | ns |
| Read address hold time in asynchronous mode | | –0.778 | | –0.915 | | ns |
| Read enable setup time | $T_{RDENSU}$ | 0.278 | | 0.327 | | ns |
| Read enable hold time | $T_{RDENHD}$ | 0.057 | | 0.067 | | ns |
| Read block select setup time | $T_{BLKSU}$ | 1.839 | | 2.163 | | ns |
| Read block select hold time | $T_{BLKHD}$ | –0.65 | | –0.765 | | ns |
| Read block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 2.036 | | 2.396 | ns |

## 2.3.14 Math Block Timing Characteristics

The fundamental building block in any digital signal processing algorithm is the multiply-accumulate function. Each IGLOO2 and SmartFusion2 SoC math block supports 18×18 signed multiplication, dot product, and built-in addition, subtraction, and accumulation units to combine multiplication results efficiently. The following table lists the math blocks with all registers used in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 268 •*** **Math Blocks with all Registers Used**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Input, control register setup time | $T_{MISU}$ | 0.149 | | 0.176 | | ns |
| Input, control register hold time | $T_{MIHD}$ | 1.68 | | 1.976 | | ns |
| CDIN input setup time | $T_{MOCDINSU}$ | 0.185 | | 0.218 | | ns |
| CDIN input hold time | $T_{MOCDINHD}$ | 0.08 | | 0.094 | | ns |
| Synchronous reset/enable setup time | $T_{MSRSTENSU}$ | –0.419 | | –0.493 | | ns |
| Synchronous reset/enable hold time | $T_{MSRSTENHD}$ | 0.011 | | 0.013 | | ns |
| Asynchronous reset removal time | $T_{MARSTREM}$ | 0 | | 0 | | ns |
| Asynchronous reset recovery time | $T_{MARSTREC}$ | 0.088 | | 0.104 | | ns |
| Output register clock to out delay | $T_{MOCQ}$ | | 0.232 | | 0.273 | ns |
| CLK minimum period | $T_{MCLKMP}$ | 2.245 | | 2.641 | | ns |

The following table lists the math blocks with input bypassed and output registers used in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 269 •*** **Math Block with Input Bypassed and Output Registers Used**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Output register setup time | $T_{MOSU}$ | 2.294 | | 2.699 | | ns |
| Output register hold time | $T_{MOHD}$ | 1.68 | | 1.976 | | ns |
| CDIN input setup time | $T_{MOCDINSU}$ | 0.115 | | 0.136 | | ns |
| CDIN input hold time | $T_{MOCDINHD}$ | –0.444 | | –0.522 | | ns |
| Synchronous reset/enable setup time | $T_{MSRSTENSU}$ | –0.419 | | –0.493 | | ns |
| Synchronous reset/enable hold time | $T_{MSRSTENHD}$ | 0.011 | | 0.013 | | ns |
| Asynchronous reset removal time | $T_{MARSTREM}$ | 0 | | 0 | | ns |
| Asynchronous reset recovery time | $T_{MARSTREC}$ | 0.014 | | 0.017 | | ns |
| Output register clock to out delay | $T_{MOCQ}$ | | 0.232 | | 0.273 | ns |
| CLK minimum period | $T_{MCLKMP}$ | 2.179 | | 2.563 | | ns |

## 2.3.17 Non-Deterministic Random Bit Generator (NRBG) Characteristics

For more information about NRBG, see *AC407: Using NRBG Services in SmartFusion2 and IGLOO2 Devices Application Note.* The following table lists the NRBG in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 275 •*** **Non-Deterministic Random Bit Generator (NRBG)**

| | | | Conditions | |
|---|---|---|---|---|
| **Service** | **Timing** | **Unit** | **Prediction Resistance** | **Additional Input** |
| Instantiate | 85 | ms | OFF | X |
| Generate (after Instantiate)[1] | 4.5 ms + (6.25 us/byte x No. of Bytes) | | OFF | 0 |
| | 6.0 ms + (6.25 us/byte x No. of Bytes) | | OFF | 64 |
| | 7.0 ms + (6.25 us/byte x No. of Bytes) | | OFF | 128 |
| Generate (after Instantiate) | 47 | ms | ON | X |
| Generate (subsequent)[1] | 0.5 ms + (6.25 us/byte x No. of Bytes) | | OFF | 0 |
| | 2.0 ms + (6.25 us/byte x No. of Bytes) | | OFF | 64 |
| | 3.0 ms + (6.25 us/byte x No. of Bytes) | | OFF | 128 |
| Generate (subsequent) | 43 | ms | ON | X |
| Reseed | 40 | ms | | |
| Uninstantiate | 0.16 | ms | | |
| Reset | 0.10 | ms | | |
| Self test | 20 | ms | First time after power-up | |
| | 6 | ms | Subsequent | |

1. If PUF_OFF, generate will incur additional PUF delay time for consecutive service calls.

## 2.3.18 Cryptographic Block Characteristics

For more information about cryptographic block and associated services, see *AC410: Using AES System Services in SmartFusion2 and IGLOO2 Devices Application Note* and *AC432: Using SHA-256 System Services in SmartFusion2 and IGLOO2 Devices Application Note*.

The following table lists the cryptographic block characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 276 •*** **Cryptographic Block Characteristics**

| **Service** | **Conditions** | **Timing** | **Unit** |
|---|---|---|---|
| Any service | First certificate check penalty at boot | 11.5 | ms |
| AES128/256 (encoding / decoding)[1] | 100 blocks up to 64k blocks | 700 | kbps |

### 2.3.31.2 SmartFusion2 Inter-Integrated Circuit ($I^2C$) Characteristics

This section describes the DC and switching of the $I^2C$ interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, see Figure 21, page 125.

The following table lists the $I^2C$ characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V

***Table 303 •*** **I2C Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Input low voltage | $V_{IL}$ | –0.3 | | 0.8 | V | See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank–LVTTL 8 mA low drive. |
| Input high voltage | $V_{IH}$ | 2 | | 3.45 | V | See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank–LVTTL 8 mA low drive. |
| Hysteresis of schmitt triggered inputs for $V_{DDI}$ > 2 V | $V_{HYS}$ | 0.05 × $V_{DDI}$ | | | V | See Table 28, page 23 for more information. |
| Input current high | $I_{IL}$ | | | 10 | µA | See Single-Ended I/O Standards, page 24 for more information. |
| Input current low | $I_{IH}$ | | | 10 | µA | See Single-Ended I/O Standards, page 24 for more information. |
| Input rise time | $T_{ir}$ | | | 1000 | ns | Standard mode |
| | | | | 300 | ns | Fast mode |
| Input fall time | $T_{if}$ | | | 300 | ns | Standard mode |
| | | | | 300 | ns | Fast mode |
| Maximum output voltage low (open drain) at 3 mA sink current for $V_{DDI}$ > 2 V | $V_{OL}$ | | | 0.4 | V | See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank–LVTTL 8 mA low drive. |
| Pin capacitance | Cin | | | 10 | pF | $V_{IN}$ = 0, f = 1.0 MHz |
| Output fall time from VIHMin to VILMax[1] | $t_{OF}$[1] | | 21.04 | | ns | $V_{IHmin}$ to $V_{ILMax}$, CLOAD = 400 pF |
| | | | 5.556 | | ns | $V_{IHmin}$ to $V_{ILMax}$, CLOAD = 100 pF |
| Output rise time from VILMax to VIHMin[1] | $t_{OR}$ [1] | | 19.887 | | ns | $V_{ILMax}$ to $V_{IHmin}$, CLOAD = 400 pF |
| | | | 5.218 | | ns | $V_{ILMax}$ to $V_{IHmin}$, CLOAD = 100 pF |
| Output buffer maximum pull-down resistance[2, 3] | $R_{pull\text{-}up}$[2,3] | | | 50 | Ω | |
| Output buffer maximum pull-up resistance[2, 4] | $R_{pull\text{-}down}$[2,4] | | | 131.25 | Ω | |

***Table 303 •*** **I2C Characteristics *(continued)***

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Maximum data rate | $D_{MAX}$ | | | 400 | Kbps | Fast mode |
| | | | | 100 | Kbps | Standard mode |
| Pulse width of spikes which must be suppressed by the input filter | $T_{FILT}$ | | 50 | | ns | Fast mode |

1. These values are provided for MSIO Bank–LVTTL 8 mA Low Drive at 25 °C, typical conditions. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.
2. These maximum values are provided for information only. Minimum output buffer resistance values depend on $V_{DDIx}$, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.
3. R(PULL-DOWN-MAX) = (VOLspec)/IOLspec.
4. R(PULL-UP-MAX) = (VDDImax–VOHspec)/IOHspec.

The following table lists the $I^2C$ switching characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V

***Table 304 •*** **I2C Switching Characteristics**

| | | –1 | Std | |
|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Min** | **Unit** |
| Low period of I2C_x_SCL | $T_{LOW}$ | 1 | 1 | PCLK cycles |
| High period of I2C_x_SCL | $T_{HIGH}$ | 1 | 1 | PCLK cycles |
| START hold time | $T_{HD;STA}$ | 1 | 1 | PCLK cycles |
| START setup time | $T_{SU;STA}$ | 1 | 1 | PCLK cycles |
| DATA hold time | $T_{HD;DAT}$ | 1 | 1 | PCLK cycles |
| DATA setup time | $T_{SU;DAT}$ | 1 | 1 | PCLK cycles |
| STOP setup time | $T_{SU;STO}$ | 1 | 1 | PCLK cycles |

***Figure 21 •*** **$I^2C$ Timing Parameter Definition**

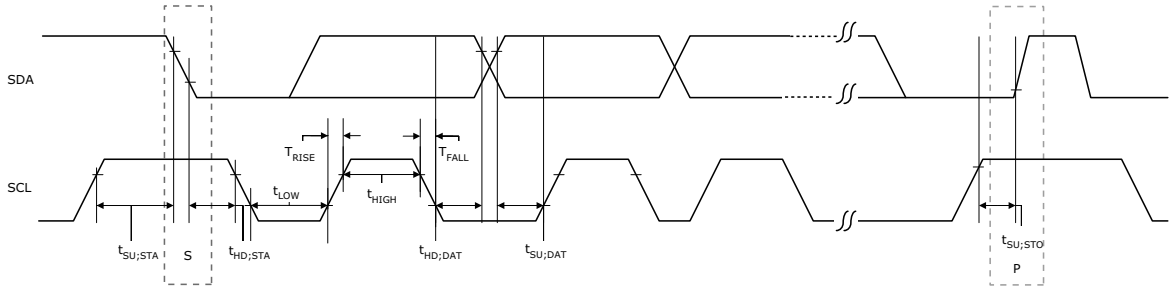
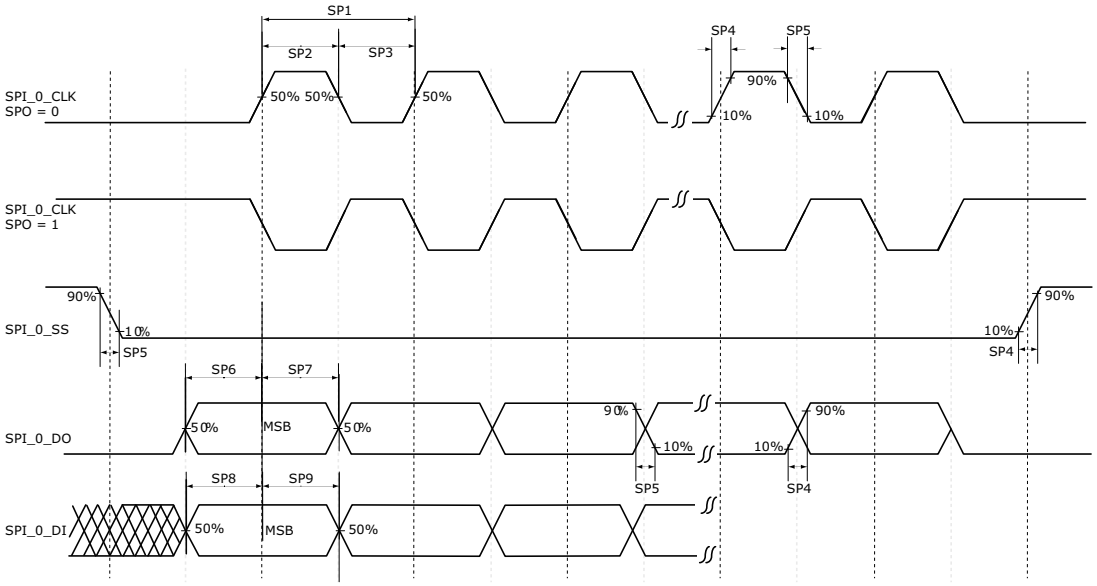


***Figure 22 •*** **SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)**




## 2.3.32 CAN Controller Characteristics

The following table lists the CAN controller characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 306 •*** **CAN Controller Characteristics**

| Parameter | Description | –1 | –Std | Unit |
|---|---|---|---|---|
| FCANREFCLK[1] | Internally sourced CAN reference clock frequency | 160 | 136 | MHz |
| BAUDCANMAX | Maximum CAN performance baud rate | 1 | 1 | Mbps |
| BAUDCANMIN | Minimum CAN performance baud rate | 0.05 | 0.05 | Mbps |

1. PCLK to CAN controller must be a multiple of 8 MHz.

## 2.3.33 USB Characteristics

The following table lists the USB characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 307 •*** **USB Characteristics**

| Parameter | Description | –1 | –Std | Unit |
|---|---|---|---|---|
| FUSBREFCLK | Internally sourced USB reference clock frequency | 166 | 142 | MHz |
| TUSBCLK | USB clock period | 16.66 | 16.66 | ns |
| TUSBPD | Clock to USB data propagation delay | 9.0 | 9.0 | ns |
| TUSBSU | Setup time for USB data | 6.0 | 6.0 | ns |
| TUSBHD | Hold time for USB data | 0 | 0 | ns |