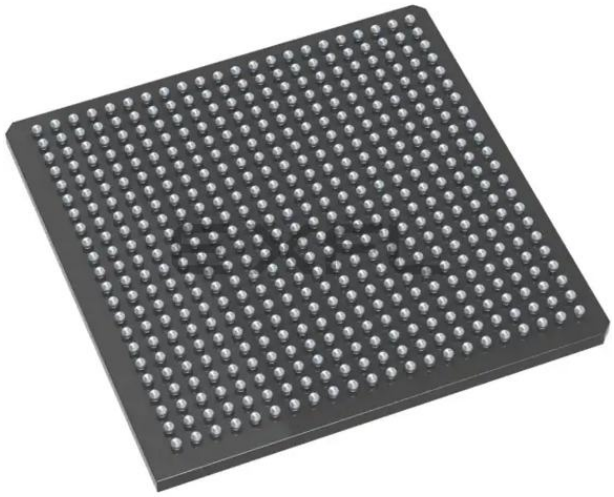

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	12084
Total RAM Bits	933888
Number of I/O	233
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2gl010ts-fg484

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 11.0

The following is a summary of the changes in revision 11.0 of this document.

Updated Table 24, page 22 with minimum and maximum values for input current low and high (SAR 73114 and 80314).
Added Non-Deterministic Random Bit Generator (NRBG) Characteristics, page 106 (SAR 73114 and 79517).
Added 060 device in Table 282, page 110 (SAR 79860).
Added DEVRST_N to Functional Times, page 116 (SAR 73114).
Added Cryptographic Block Characteristics, page 106 (SAR 73114 and 79516).
Update Table 296, page 121 with VTX-AMP details (SAR 81756).
Update note in Table 297, page 122 (SAR 74570 and 80677).
Update Table 298, page 122 with generic EPCS details (SAR 75307).
Added Table 308, page 129 (SAR 50424).

1.2 Revision 10.0

The following is a summary of the changes in revision 10.0 of this document.

The Surge Current on VDD during DEVRST_B Assertion and Surge Current on VDD during Digest Check using System Services tables were deleted and added reference to AC393: Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs Application Note. (SAR 76865 and 76623).
Added 060 device in Table 4, page 6 (SAR 76383).
Updated Table 24, page 22 for ramp time input (SAR 72103).
Added 060 device details in Table 284, page 112 (SAR 74927).
Updated Table 290, page 116 for name change (SAR 74925).
Updated Table 283, page 111 for 060 FG676 Package details (SAR 78849).
Updated Table 305, page 126 for SmartFusion2 and Table 310, page 129 for IGLOO2 for SPI timing and Fmax (SAR 56645, 75331).
Updated Table 293, page 119 for Flash*Freeze entry and exit times (SAR 75329, 75330).
Updated Table 297, page 122 for RX-CID information (SAR 78271).
Added Table 8, page 8 and Figure 1, page 9 (SAR 78932).
Updated Table 223, page 76 for timing characteristics and Table 224, page 77(SAR 75998).
Added SRAM PUF, page 105 (SAR 64406).
Added a footnote on digest cycle in Table 5, page 7 (SAR 79812).

1.3 Revision 9.0

The following is a summary of the changes in revision 9.0 of this document.

Added a note in Table 5, page 7 (SAR 71506).
Added a note in Table 6, page 8 (SAR 74616).
Added a note in Figure 3, page 17 (SAR 71506).
Updated Quiescent Supply Current for 060 in Table 11, page 12 and Table 12, page 13 (SAR 74483).
Updated programming currents for 060 in Table 13, page 13, Table 14, page 13, and Table 15, page 14.
Added DEVRST_B assertion tables (SAR 74708).
Updated I/O speeds for LVDS 3.3 V in Table 18, page 19 and Table 21, page 20 (SAR 69829).
Updated Table 24, page 22 (SAR 69418).
Updated Table 25, page 22, Table 26, page 23, Table 27, page 23 (SAR 74570).
Updated all AC/DC table to link to the Input Capacitance, Leakage Current, and Ramp Time, page 22 for reference (SAR 69418).

Table 310 • **SPI Characteristics for All Devices *(continued)***

Symbol	Description	Min	Typ	Max	Unit	Conditions
SPI master configuration (applicable for 060, 090, and 150 devices)						
sp6m	SPI_[0|1]_DO setup time[2]	(SPI_x_CLK_period/2) – 7.0			ns	
sp7m	SPI_[0|1]_DO hold time[2]	(SPI_x_CLK_period/2) – 9.5			ns	
sp8m	SPI_[0|1]_DI setup time[2]	15			ns	
sp9m	SPI_[0|1]_DI hold time[2]	–2.5			ns	
SPI slave configuration (applicable for 060, 090, and 150 devices)						
sp6s	SPI_[0|1]_DO setup time[2]	(SPI_x_CLK_period/2) – 16.0			ns	
sp7s	SPI_[0|1]_DO hold time[2]	(SPI_x_CLK_period/2) - 3.5			ns	
sp8s	SPI_[0|1]_DI setup time[2]	3			ns	
sp9s	SPI_[0|1]_DI hold time[2]	2.5			ns	

1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.
2. For allowable pclk configurations, see the Serial Peripheral Interface Controller section in the *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.
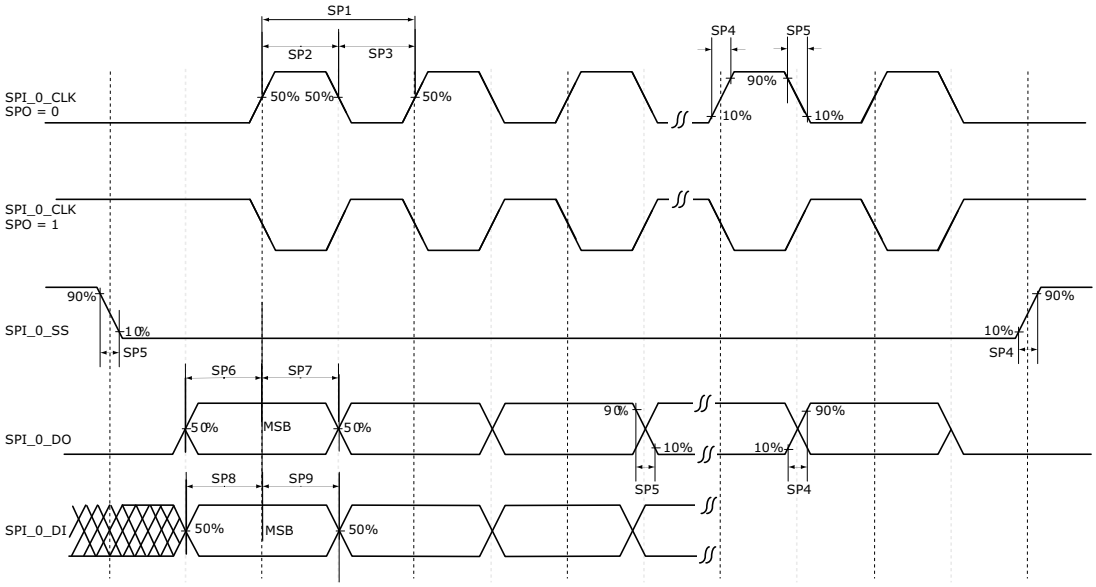
Figure 23 • **SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)**