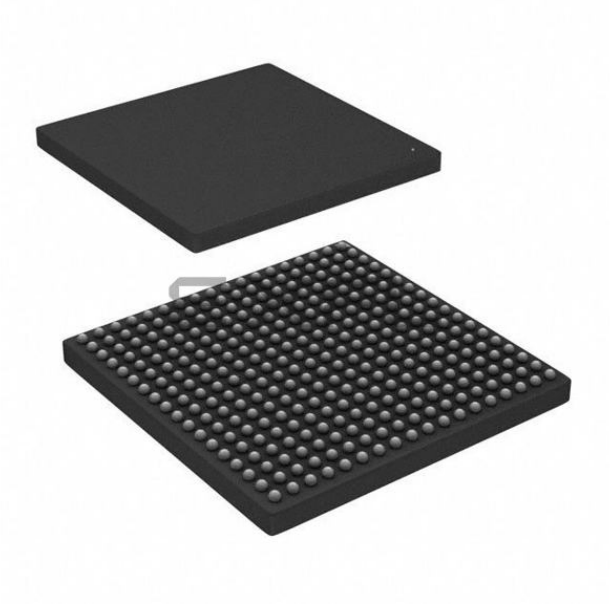

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 27696 |
| Total RAM Bits | 1130496 |
| Number of I/O | 180 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 325-TFBGA, FCBGA |
| Supplier Device Package | 325-FCBGA (11x11) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m2gl025-1fcsg325 |

where

$\theta_{JA}$ = Junction-to-air thermal resistance

$\theta_{JB}$ = Junction-to-board thermal resistance

$\theta_{JC}$ = Junction-to-case thermal resistance

$T_J$ = Junction temperature

$T_A$ = Ambient temperature

$T_B$ = Board temperature (measured 1.0 mm away from the package edge)

$T_C$ = Case temperature

P = Total power dissipated by the device

***Table 9 •*** **Package Thermal Resistance of SmartFusion2 and IGLOO2 Devices**

| | **Still Air** | **1.0 m/s** | **2.5 m/s** | | | |
|---|---|---|---|---|---|---|
| **Device** | | $\theta_{JA}$ | | $\theta_{JB}$ | $\theta_{JC}$ | **Unit** |
| **005** | | | | | | |
| FG484 | 19.36 | 15.81 | 14.63 | 9.74 | 5.27 | °C/W |
| VF256 | 41.30 | 38.16 | 35.30 | 28.41 | 3.94 | °C/W |
| VF400 | 20.19 | 16.94 | 15.41 | 8.86 | 4.95 | °C/W |
| TQ144 | 42.80 | 36.80 | 34.50 | 37.20 | 10.80 | °C/W |
| **010** | | | | | | |
| FG484 | 18.22 | 14.83 | 13.62 | 8.83 | 4.92 | °C/W |
| VF256 | 37.36 | 34.26 | 31.45 | 24.84 | 7.89 | °C/W |
| VF400 | 19.40 | 15.75 | 14.22 | 8.11 | 4.22 | °C/W |
| TQ144 | 38.60 | 32.60 | 30.30 | 31.80 | 8.60 | °C/W |
| **025** | | | | | | |
| FG484 | 17.03 | 13.66 | 12.45 | 7.66 | 4.18 | °C/W |
| VF256 | 33.85 | 30.59 | 27.85 | 21.63 | 6.13 | °C/W |
| VF400 | 18.36 | 14.89 | 13.36 | 7.12 | 3.41 | °C/W |
| FCS325 | 29.17 | 24.87 | 23.12 | 14.44 | 2.31 | °C/W |
| **050** | | | | | | |
| FG484 | 15.29 | 12.19 | 10.99 | 6.27 | 3.24 | °C/W |
| FG896 | 14.70 | 12.50 | 10.90 | 7.20 | 4.90 | °C/W |
| VF400 | 17.53 | 14.17 | 12.63 | 6.32 | 2.81 | °C/W |
| FCS325 | 27.38 | 23.18 | 21.41 | 12.47 | 1.59 | °C/W |
| **060** | | | | | | |
| FG484 | 15.40 | 12.06 | 10.85 | 6.14 | 3.15 | °C/W |
| FG676 | 15.49 | 12.21 | 11.06 | 7.07 | 3.87 | °C/W |
| VF400 | 17.45 | 14.01 | 12.47 | 6.22 | 2.69 | °C/W |
| FCS325 | 27.03 | 22.91 | 21.25 | 12.33 | 1.54 | °C/W |
| **090** | | | | | | |
| FG484 | 14.64 | 11.37 | 10.16 | 5.43 | 2.77 | °C/W |
| FG676 | 14.52 | 11.19 | 10.37 | 6.17 | 3.24 | °C/W |
| FCS325 | 26.63 | 22.26 | 20.13 | 14.24 | 2.50 | °C/W |

## 2.3.2 Power Consumption

The following sections describe the power consumptions of the devices.

### 2.3.2.1 Quiescent Supply Current

***Table 10 •*** **Quiescent Supply Current Characteristics**

| | Modes and Configurations | |
|---|---|---|
| **Power Supplies/Blocks** | **Non-Flash*Freeze** | **Flash*Freeze** |
| FPGA Core | On | Off |
| $V_{DD}$/SERDES_[01]_VDD[1] | On | On |
| $V_{PP}/V_{PPNVM}$ | On | On |
| HPMS_MDDR_PLL_VDDA/FDDR_PLL_VDDA/ CCC_XX[01]_PLL_VDDA/PLL0_PLL1_HPMS_MDDR_VDD A | 0 V | 0 V |
| SERDES_[01]_PLL_VDDA[2] | 0 V | 0 V |
| SERDES_[01]_L[0123]_VDDAPLL/VDD_2V5[2] | On | On |
| SERDES_[01]_L[0123]_VDDAIIO[2] | On | On |
| $V_{DDIx}$[3, 4] | On | On |
| $V_{REFx}$ | On | On |
| MSSDDR CLK | 32 kHz | 32 kHz |
| RAM | On | Sleep state |
| System controller | 50 MHz | 50 MHz |
| 50 MHz oscillator (enable/disable) | Enable | Disabled |
| 1 MHz oscillator (enable/disable) | Disabled | Disabled |
| Crystal oscillator (enable/disable) | Disabled | Disabled |

1. SERDES_[01]_VDD Power Supply is shorted to $V_{DD}$.
2. SerDes and DDR blocks to be unused.
3. $V_{DDIx}$ has been set to ON for test conditions as described. Banks on the east side should always be powered with the appropriate $V_{DDI}$ bank supplies. For details on bank power supplies, see “Recommendation for Unused Bank Supplies” table in the *AC393: SmartFusion2 and IGLOO2 Board Design Guidelines Application Note*.
4. No Differential (that is to say, LVDS) I/Os or ODT attributes to be used.

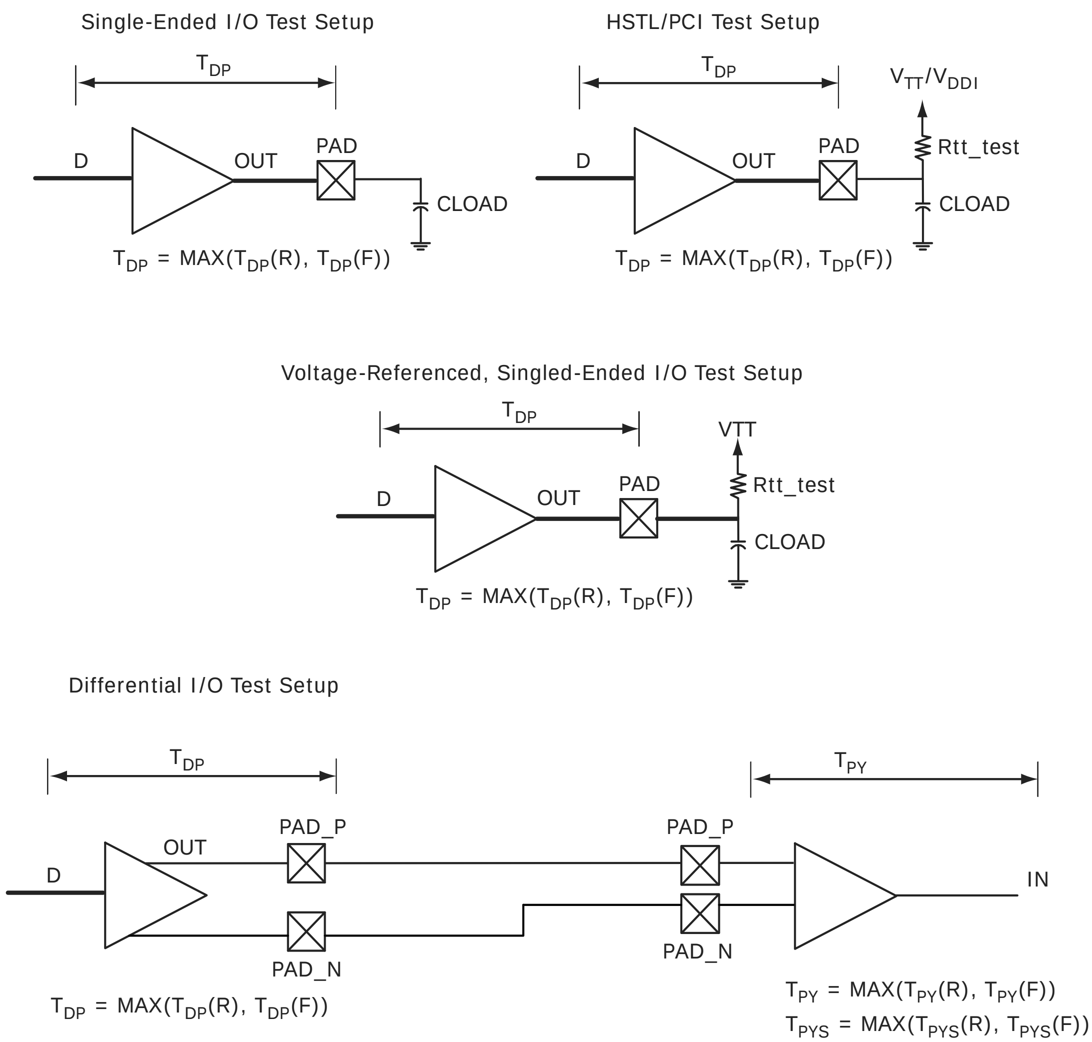
***Table 11 •*** **SmartFusion2 and IGLOO2 Quiescent Supply Current ($V_{DD}$ = 1.2 V) – Typical Process**

| Symbol | Modes | 005 | 010 | 025 | 050 | 060 | 090 | 150 | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| IDC1 | Non-Flash*Freeze | 6.2 | 6.9 | 8.9 | 13.1 | 15.3 | 15.4 | 27.5 | mA | Typical ($T_J$ = 25 °C) |
| | | 24.0 | 28.4 | 40.6 | 67.8 | 80.6 | 81.4 | 144.7 | mA | Commercial ($T_J$ = 85 °C) |
| | | 35.2 | 41.9 | 60.5 | 102.1 | 121.4 | 122.6 | 219.1 | mA | Industrial ($T_J$ = 100 °C) |

## 2.3.5.2 Output Buffer and AC Loading

The following figure shows the output buffer and AC loading.

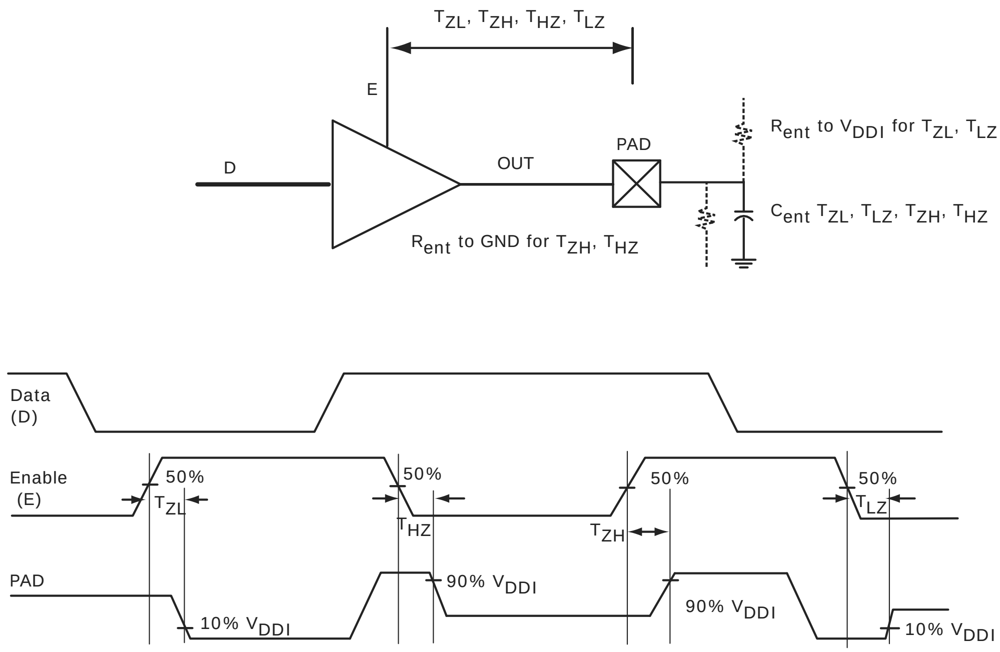
***Figure 4 •*** **Output Buffer AC Loading**



### 2.3.5.3 Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The following figure shows the methodology of characterization illustrated by the enable path test point.

***Figure 5 •*** **Tristate Buffer for Enable Path Test Point**




### 2.3.5.4 I/O Speeds

This section describes the maximum data rate summary of I/O in worst-case industrial conditions. See the individual I/O standards for operating conditions.

***Table 18 •*** **Maximum Data Rate Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions**

| I/O | MSIO | MSIOD | DDRIO | Unit |
|---|---|---|---|---|
| PCI 3.3 V | 630 | | | Mbps |
| LVTTL 3.3 V | 600 | | | Mbps |
| LVCMOS 3.3 V | 600 | | | Mbps |
| LVCMOS 2.5 V | 410 | 420 | 400 | Mbps |
| LVCMOS 1.8 V | 295 | 400 | 400 | Mbps |
| LVCMOS 1.5 V | 160 | 220 | 235 | Mbps |
| LVCMOS 1.2 V | 120 | 160 | 200 | Mbps |
| LPDDR-LVCMOS 1.8 V mode | | | 400 | Mbps |

### 2.3.5.6 Single-Ended I/O Standards

#### 2.3.5.6.1 Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)

LVCMOS is a widely used switching standard implemented in CMOS transistors. This standard is defined by JEDEC (JESD 8-5). The LVCMOS standards supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs are: LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33.

#### 2.3.5.6.2 3.3 V LVCMOS/LVTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3 V applications.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

***Table 29 •*** **LVTTL/LVCMOS 3.3 V DC Recommended DC Operating Conditions (Applicable to MSIO I/O Bank Only)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 3.15 | 3.3 | 3.45 | V |

***Table 30 •*** **LVTTL/LVCMOS 3.3 V Input Voltage Specification (Applicable to MSIO I/O Bank Only)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high | $V_{IH}$ (DC) | 2.0 | 3.45 | V |
| DC input logic low | $V_{IL}$ (DC) | –0.3 | 0.8 | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

***Table 31 •*** **LVCMOS 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC output logic high[1] | $V_{OH}$ | $V_{DDI}$ – 0.4 | | V |
| DC output logic low[1] | $V_{OL}$ | | 0.4 | V |

1. The $V_{OH}$/$V_{OL}$ test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.

***Table 32 •*** **LVTTL 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC output logic high | $V_{OH}$ | 2.4 | | V |
| DC output logic low | $V_{OL}$ | | 0.4 | V |

***Table 33 •*** **LVTTL/LVCMOS 3.3 V AC Maximum Switching Speed (Applicable to MSIO I/O Bank Only)**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 600 | Mbps | AC loading: 17 pF load, maximum drive/slew |

### 2.3.5.7 2.5 V LVCMOS

LVCMOS 2.5 V is a general standard for 2.5 V applications and is supported in IGLOO2 FPGA and SmartFusion2 SoC FPGAs that are in compliance with the JEDEC specification JESD8-5A.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

*Table 38 •* **LVCMOS 2.5 V DC Recommended DC Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 2.375 | 2.5 | 2.625 | V |

*Table 39 •* **LVCMOS 2.5 V DC Input Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high (for MSIOD and DDRIO I/O banks) | $V_{IH}$ (DC) | 1.7 | 2.625 | V |
| DC input logic high (for MSIO I/O bank) | $V_{IH}$ (DC) | 1.7 | 3.45 | V |
| DC input logic low | $V_{IL}$ (DC) | –0.3 | 0.7 | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

*Table 40 •* **LVCMOS 2.5 V DC Output Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC output logic high | $V_{OH}$[1] | $V_{DDI}$ – 0.4 | – | V |
| DC output logic low | $V_{OL}$[2] | | 0.4 | V |

1. The VOH/VOL test points selected ensure compliance with LVCMOS 2.5 V JEDEC8-5A requirements.

*Table 41 •* **LVCMOS 2.5 V AC Minimum and Maximum Switching Speed**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for DDRIO I/O bank) | $D_{MAX}$ | 400 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 410 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIOD I/O bank) | $D_{MAX}$ | 420 | Mbps | AC loading: 17 pF load, maximum drive/slew |

*Table 42 •* **LVCMOS 2.5 V AC Calibrated Impedance Option**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | Rodt_cal | 75, 60, 50, 33, 25, 20 | Ω |

***Table 46 •*** **LVCMOS 2.5 V Transmitter Characteristics for DDRIO Bank (Output and Tristate Buffers) *(continued)***

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| 4 mA | Slow | 3.095 | 3.641 | 2.705 | 3.182 | 3.088 | 3.633 | 4.738 | 5.575 | 4.348 | 5.116 | ns |
| | Medium | 2.825 | 3.324 | 2.488 | 2.927 | 2.823 | 3.321 | 4.492 | 5.285 | 4.063 | 4.781 | ns |
| | Medium fast | 2.701 | 3.178 | 2.384 | 2.804 | 2.698 | 3.173 | 4.364 | 5.135 | 3.945 | 4.642 | ns |
| | Fast | 2.69 | 3.165 | 2.377 | 2.796 | 2.687 | 3.161 | 4.359 | 5.129 | 3.94 | 4.636 | ns |
| 6 mA | Slow | 2.919 | 3.434 | 2.491 | 2.93 | 2.902 | 3.414 | 5.085 | 5.983 | 4.674 | 5.5 | ns |
| | Medium | 2.65 | 3.118 | 2.279 | 2.681 | 2.642 | 3.108 | 4.845 | 5.701 | 4.375 | 5.148 | ns |
| | Medium fast | 2.529 | 2.975 | 2.176 | 2.56 | 2.521 | 2.965 | 4.724 | 5.558 | 4.259 | 5.011 | ns |
| | Fast | 2.516 | 2.96 | 2.168 | 2.551 | 2.508 | 2.95 | 4.717 | 5.55 | 4.251 | 5.002 | ns |
| 8 mA | Slow | 2.863 | 3.368 | 2.427 | 2.855 | 2.844 | 3.346 | 5.196 | 6.114 | 4.769 | 5.612 | ns |
| | Medium | 2.599 | 3.058 | 2.217 | 2.608 | 2.59 | 3.047 | 4.952 | 5.827 | 4.471 | 5.261 | ns |
| | Medium fast | 2.483 | 2.921 | 2.114 | 2.487 | 2.473 | 2.91 | 4.832 | 5.685 | 4.364 | 5.134 | ns |
| | Fast | 2.467 | 2.902 | 2.106 | 2.478 | 2.457 | 2.89 | 4.826 | 5.678 | 4.348 | 5.116 | ns |
| 12 mA | Slow | 2.747 | 3.232 | 2.296 | 2.701 | 2.724 | 3.204 | 5.39 | 6.342 | 4.938 | 5.81 | ns |
| | Medium | 2.493 | 2.934 | 2.102 | 2.473 | 2.483 | 2.921 | 5.166 | 6.078 | 4.65 | 5.471 | ns |
| | Medium fast | 2.382 | 2.803 | 2.006 | 2.36 | 2.371 | 2.789 | 5.067 | 5.962 | 4.546 | 5.349 | ns |
| | Fast | 2.369 | 2.787 | 1.999 | 2.352 | 2.357 | 2.773 | 5.063 | 5.958 | 4.538 | 5.339 | ns |
| 16 mA | Slow | 2.677 | 3.149 | 2.213 | 2.604 | 2.649 | 3.116 | 5.575 | 6.56 | 5.08 | 5.977 | ns |
| | Medium | 2.432 | 2.862 | 2.028 | 2.386 | 2.421 | 2.848 | 5.372 | 6.32 | 4.801 | 5.649 | ns |
| | Medium fast | 2.324 | 2.734 | 1.937 | 2.278 | 2.311 | 2.718 | 5.297 | 6.233 | 4.7 | 5.531 | ns |
| | Fast | 2.313 | 2.721 | 1.929 | 2.269 | 2.3 | 2.706 | 5.296 | 6.231 | 4.699 | 5.529 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

***Table 47 •*** **LVCMOS 2.5 V Transmitter Characteristics for MSIO Bank (Output and Tristate Buffers)**

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| 2 mA | Slow | 3.48 | 4.095 | 3.855 | 4.534 | 3.785 | 4.453 | 2.12 | 2.494 | 3.45 | 4.059 | ns |
| 4 mA | Slow | 2.583 | 3.039 | 3.042 | 3.579 | 3.138 | 3.691 | 4.143 | 4.874 | 4.687 | 5.513 | ns |
| 6 mA | Slow | 2.392 | 2.815 | 2.669 | 3.139 | 2.82 | 3.317 | 4.909 | 5.775 | 5.083 | 5.98 | ns |
| 8 mA | Slow | 2.309 | 2.717 | 2.565 | 3.017 | 2.74 | 3.223 | 5.812 | 6.837 | 5.523 | 6.497 | ns |
| 12 mA | Slow | 2.333 | 2.745 | 2.437 | 2.867 | 2.626 | 3.089 | 6.131 | 7.213 | 5.712 | 6.72 | ns |
| 16 mA | Slow | 2.412 | 2.838 | 2.335 | 2.747 | 2.533 | 2.979 | 6.54 | 7.694 | 6.007 | 7.067 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

***Table 118 •*** **DDR1/SSTL2 Class II Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| Single-ended | 2.29 | 2.693 | 1.988 | 2.338 | 1.978 | 2.326 | 1.989 | 2.34 | 1.979 | 2.328 | ns |
| Differential | 2.418 | 2.846 | 2.304 | 2.711 | 2.297 | 2.702 | 2.131 | 2.506 | 2.124 | 2.499 | ns |

### 2.3.6.4 Stub-Series Terminated Logic 1.8 V (SSTL18)

SSTL18 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double date rate (DDR2) standard. IGLOO2 and SmartFusion2 SoC FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

***Table 119 •*** **SSTL18 DC Recommended DC Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 1.71 | 1.8 | 1.89 | V |
| Termination voltage | $V_{TT}$ | 0.838 | 0.900 | 0.964 | V |
| Input reference voltage | $V_{REF}$ | 0.838 | 0.900 | 0.964 | V |

***Table 120 •*** **SSTL18 DC Input Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high | $V_{IH}$ (DC) | $V_{REF}$ + 0.125 | 1.89 | V |
| DC input logic low | $V_{IL}$ (DC) | –0.3 | $V_{REF}$ – 0.125 | V |
| Input current high[1] | $I_{IH}$ (DC) | | | |
| Input current low[1] | $I_{IL}$ (DC) | | | |

1. See Table 24, page 22.

***Table 121 •*** **SSTL18 DC Output Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| **SSTL18 Class I (DDR2 Reduced Drive)** | | | | |
| DC output logic high | $V_{OH}$ | $V_{TT}$ + 0.603 | | V |
| DC output logic low | $V_{OL}$ | | $V_{TT}$– 0.603 | V |
| Output minimum source DC current (DDRIO I/O bank only) | $I_{OH}$ at $V_{OH}$ | 6.5 | | mA |
| Output minimum sink current (DDRIO I/O bank only) | $I_{OL}$ at $V_{OL}$ | –6.5 | | mA |
| **SSTL18 Class II (DDR2 Full Drive)[1]** | | | | |
| DC output logic high | $V_{OH}$ | $V_{TT}$ + 0.603 | | V |
| DC output logic low | $V_{OL}$ | | $V_{TT}$– 0.603 | V |
| Output minimum source DC current (DDRIO I/O bank only) | $I_{OH}$ at $V_{OH}$ | 13.4 | | mA |
| Output minimum sink current (DDRIO I/O bank only) | $I_{OL}$ at $V_{OL}$ | –13.4 | | mA |

1. To meet JEDEC Electrical Compliance, use DDR2 Full Drive Transmitter.

***Table 122 •*** **SSTL18 DC Differential Voltage Specification**

| Parameter | Symbol | Min | Unit |
|---|---|---|---|
| DC input differential voltage | $V_{ID}$ (DC) | 0.3 | V |

***Table 123 •*** **SSTL18 AC Differential Voltage Specifications (Applicable to DDRIO Bank Only)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| AC input differential voltage | $V_{DIFF}$ (AC) | 0.5 | | V |
| AC differential cross point voltage | $V_x$ (AC) | $0.5 \times V_{DDI} - 0.175$ | $0.5 \times V_{DDI} + 0.175$ | V |

***Table 124 •*** **SSTL18 Minimum and Maximum AC Switching Speed (Applicable to DDRIO Bank Only)**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for DDRIO I/O bank) | $D_{MAX}$ | 667 | Mbps | AC loading: per JEDEC specification |

***Table 125 •*** **SSTL18 AC Impedance Specifications (Applicable to DDRIO Bank Only)**

| Parameter | Symbol | Typ | Unit | Conditions |
|---|---|---|---|---|
| Supported output driver calibrated impedance (for DDRIO I/O bank) | $R_{REF}$ | 20, 42 | Ω | Reference resistor = 150 Ω |
| Effective impedance value (ODT) | $R_{TT}$ | 50, 75, 150 | Ω | Reference resistor = 150 Ω |

***Table 126 •*** **SSTL18 AC Test Parameter Specifications (Applicable to DDRIO Bank Only)**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | 0.9 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Reference resistance for data test path for SSTL18 Class I ($T_{DP}$) | RTT_TEST | 50 | Ω |
| Reference resistance for data test path for SSTL18 Class II ($T_{DP}$) | RTT_TEST | 25 | Ω |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | pF |

**AC Switching Characteristics**

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 1.71 V

***Table 127 •*** **DDR2/SSTL18 Receiver Characteristics for DDRIO I/O Bank with Fixed Code**

| | | $T_{PY}$ | | |
|---|---|---|---|---|
| | **On-Die Termination (ODT)** | **–1** | **–Std** | **Unit** |
| Pseudo differential | None | 1.567 | 1.844 | ns |
| True differential | None | 1.588 | 1.869 | ns |

***Table 162 •*** **LVDS DC Output Voltage Specification**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DC output logic high | $V_{OH}$ | 1.25 | 1.425 | 1.6 | V |
| DC output logic low | $V_{OL}$ | 0.9 | 1.075 | 1.25 | V |

***Table 163 •*** **LVDS DC Differential Voltage Specification**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Differential output voltage swing | $V_{OD}$ | 250 | 350 | 450 | mV |
| Output common mode voltage | $V_{OCM}$ | 1.125 | 1.25 | 1.375 | V |
| Input common mode voltage | $V_{ICM}$ | 0.05 | 1.25 | 2.35 | V |
| Input differential voltage | $V_{ID}$ | 100 | 350 | 600 | mV |

***Table 164 •*** **LVDS Minimum and Maximum AC Switching Speed**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 535 | Mbps | AC loading: 12 pF / 100 Ω differential load |
| Maximum data rate (for MSIOD I/O bank) no pre-emphasis | $D_{MAX}$ | 620 | Mbps | AC loading: 10 pF / 100 Ω differential load |
| | | 700 | Mbps | AC loading: 2 pF / 100 Ω differential load |

***Table 165 •*** **LVDS AC Impedance Specifications**

| Parameter | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Termination resistance | RT | 100 | | Ω |

***Table 166 •*** **LVDS AC Test Parameter Specifications**

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | Cross point | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |

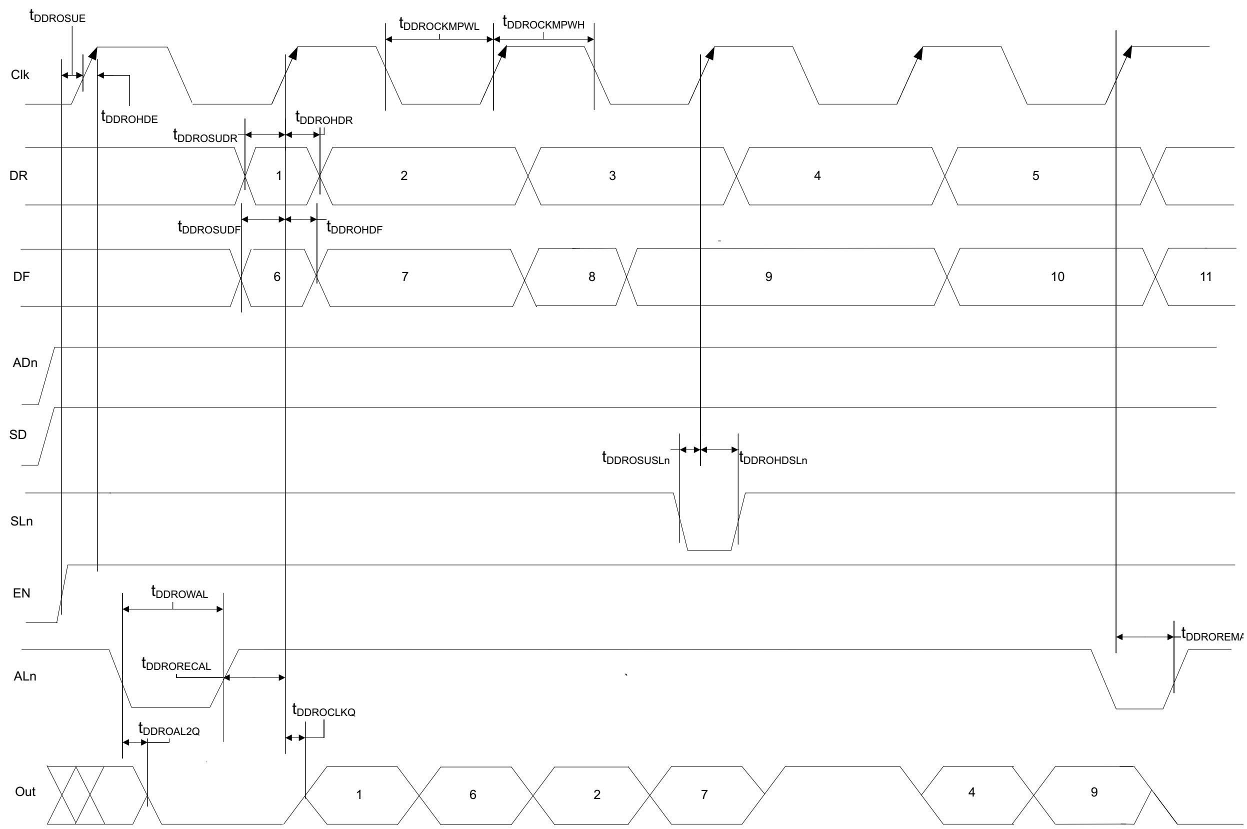
### LVDS25 AC Switching Characteristics

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 2.375 V

***Table 167 •*** **LVDS25 Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

| | $T_{PY}$ | | |
|---|---|---|---|
| **On-Die Termination (ODT)** | **–1** | **–Std** | **Unit** |
| None | 2.774 | 3.263 | ns |
| 100 | 2.775 | 3.264 | ns |

***Figure 13 •*** **Output DDR Timing Diagram**




## *2.3.9.5 Timing Characteristics*

The following table lists the output DDR propagation delays in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 222 •*** **Output DDR Propagation Delays**

| **Symbol** | **Description** | **Measuring Nodes (from, to)** | **–1** | **–Std** | **Unit** |
|---|---|---|---|---|---|
| $T_{DDROCLKQ}$ | Clock-to-out of DDR for output DDR | E, G | 0.263 | 0.309 | ns |
| $T_{DDROSUDF}$ | Data_F data setup for output DDR | F, E | 0.143 | 0.168 | ns |
| $T_{DDROSUDR}$ | Data_R data setup for output DDR | A, E | 0.19 | 0.223 | ns |
| $T_{DDROHDF}$ | Data_F data hold for output DDR | F, E | 0 | 0 | ns |
| $T_{DDROHDR}$ | Data_R data hold for output DDR | A, E | 0 | 0 | ns |
| $T_{DDROSUE}$ | Enable setup for input DDR | B, E | 0.419 | 0.493 | ns |
| $T_{DDROHE}$ | Enable hold for input DDR | B, E | 0 | 0 | ns |
| $T_{DDROSUSLN}$ | Synchronous load setup for input DDR | D, E | 0.196 | 0.231 | ns |
| $T_{DDROHSLN}$ | Synchronous load hold for input DDR | D, E | 0 | 0 | ns |
| $T_{DDROAL2Q}$ | Asynchronous load-to-out for output DDR | C, G | 0.528 | 0.621 | ns |
| $T_{DDROREMAL}$ | Asynchronous load removal time for output DDR | C, E | 0 | 0 | ns |
| $T_{DDRORECAL}$ | Asynchronous load recovery time for output DDR | C, E | 0.034 | 0.04 | ns |

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 16K × 1 in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 235 •*** **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 16K × 1**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Clock period | $T_{CY}$ | 2.5 | | 2.941 | | ns |
| Clock minimum pulse width high | $T_{CLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Clock minimum pulse width low | $T_{CLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock period | $T_{PLCY}$ | 2.5 | | 2.941 | | ns |
| Pipelined clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.32 | | 0.377 | ns |
| Read access time without pipeline register | | | 2.269 | | 2.669 | ns |
| Access time with feed-through write timing | | | 1.51 | | 1.777 | ns |
| Address setup time | $T_{ADDRSU}$ | 0.626 | | 0.737 | | ns |
| Address hold time | $T_{ADDRHD}$ | 0.274 | | 0.322 | | ns |
| Data setup time | $T_{DSU}$ | 0.322 | | 0.378 | | ns |
| Data hold time | $T_{DHD}$ | 0.082 | | 0.096 | | ns |
| Block select setup time | $T_{BLKSU}$ | 0.207 | | 0.244 | | ns |
| Block select hold time | $T_{BLKHD}$ | 0.216 | | 0.254 | | ns |
| Block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 1.51 | | 1.777 | ns |
| Block select minimum pulse width | $T_{BLKMPW}$ | 0.186 | | 0.219 | | ns |
| Read enable setup time | $T_{RDESU}$ | 0.53 | | 0.624 | | ns |
| Read enable hold time | $T_{RDEHD}$ | 0.071 | | 0.083 | | ns |
| Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLESU}$ | 0.248 | | 0.291 | | ns |
| Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLEHD}$ | 0.102 | | 0.12 | | ns |
| Asynchronous reset to output propagation delay | $T_{R2Q}$ | | 1.547 | | 1.82 | ns |
| Asynchronous reset removal time | $T_{RSTREM}$ | 0.506 | | 0.595 | | ns |
| Asynchronous reset recovery time | $T_{RSTREC}$ | 0.004 | | 0.005 | | ns |
| Asynchronous reset minimum pulse width | $T_{RSTMPW}$ | 0.301 | | 0.354 | | ns |
| Pipelined register asynchronous reset removal time | $T_{PLRSTREM}$ | –0.279 | | –0.328 | | ns |
| Pipelined register asynchronous reset recovery time | $T_{PLRSTREC}$ | 0.327 | | 0.385 | | ns |
| Pipelined register asynchronous reset minimum pulse width | $T_{PLRSTMPW}$ | 0.282 | | 0.332 | | ns |
| Synchronous reset setup time | $T_{SRSTSU}$ | 0.226 | | 0.265 | | ns |
| Synchronous reset hold time | $T_{SRSTHD}$ | 0.036 | | 0.043 | | ns |
| Write enable setup time | $T_{WESU}$ | 0.454 | | 0.534 | | ns |
| Write enable hold time | $T_{WEHD}$ | 0.048 | | 0.057 | | ns |
| Maximum frequency | $F_{MAX}$ | | 400 | | 340 | MHz |

The following table lists the RAM1K18 – two-port mode for depth × width configuration 512 × 36 in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 236 •*** **RAM1K18 – Two-Port Mode for Depth × Width Configuration 512 × 36**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Clock period | $T_{CY}$ | 2.5 | | 2.941 | | ns |
| Clock minimum pulse width high | $T_{CLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Clock minimum pulse width low | $T_{CLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock period | $T_{PLCY}$ | 2.5 | | 2.941 | | ns |
| Pipelined clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.125 | | 1.323 | | ns |
| Pipelined clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.334 | | 0.393 | ns |
| Read access time without pipeline register | | | 2.25 | | 2.647 | ns |
| Address setup time | $T_{ADDRSU}$ | 0.313 | | 0.368 | | ns |
| Address hold time | $T_{ADDRHD}$ | 0.274 | | 0.322 | | ns |
| Data setup time | $T_{DSU}$ | 0.337 | | 0.396 | | ns |
| Data hold time | $T_{DHD}$ | 0.111 | | 0.13 | | ns |
| Block select setup time | $T_{BLKSU}$ | 0.207 | | 0.244 | | ns |
| Block select hold time | $T_{BLKHD}$ | 0.201 | | 0.237 | | ns |
| Block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 2.25 | | 2.647 | ns |
| Block select minimum pulse width | $T_{BLKMPW}$ | 0.186 | | 0.219 | | ns |
| Read enable setup time | $T_{RDESU}$ | 0.449 | | 0.528 | | ns |
| Read enable hold time | $T_{RDEHD}$ | 0.167 | | 0.197 | | ns |
| Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLESU}$ | 0.248 | | 0.291 | | ns |
| Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLEHD}$ | 0.102 | | 0.12 | | ns |
| Asynchronous reset to output propagation delay | $T_{R2Q}$ | | 1.506 | | 1.772 | ns |
| Asynchronous reset removal time | $T_{RSTREM}$ | 0.506 | | 0.595 | | ns |
| Asynchronous reset recovery time | $T_{RSTREC}$ | 0.004 | | 0.005 | | ns |
| Asynchronous reset minimum pulse width | $T_{RSTMPW}$ | 0.301 | | 0.354 | | ns |
| Pipelined register asynchronous reset removal time | $T_{PLRSTREM}$ | –0.279 | | –0.328 | | ns |
| Pipelined register asynchronous reset recovery time | $T_{PLRSTREC}$ | 0.327 | | 0.385 | | ns |
| Pipelined register asynchronous reset minimum pulse width | $T_{PLRSTMPW}$ | 0.282 | | 0.332 | | ns |
| Synchronous reset setup time | $T_{SRSTSU}$ | 0.226 | | 0.265 | | ns |
| Synchronous reset hold time | $T_{SRSTHD}$ | 0.036 | | 0.043 | | ns |
| Write enable setup time | $T_{WESU}$ | 0.39 | | 0.458 | | ns |
| Write enable hold time | $T_{WEHD}$ | 0.242 | | 0.285 | | ns |
| Maximum frequency | $F_{MAX}$ | | 400 | | 340 | MHz |

The following table lists the µSRAM in 256 × 4 mode in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 241 •*** **µSRAM (RAM256x4) in 256 × 4 Mode**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Read clock period | $T_{CY}$ | 4 | | 4 | | ns |
| Read clock minimum pulse width high | $T_{CLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read clock minimum pulse width low | $T_{CLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock period | $T_{PLCY}$ | 4 | | 4 | | ns |
| Read pipeline clock minimum pulse width high | $T_{PLCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Read pipeline clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.27 | | 0.31 | ns |
| Read access time without pipeline register | | | 1.75 | | 2.06 | ns |
| Read address setup time in synchronous mode | $T_{ADDRSU}$ | 0.301 | | 0.354 | | ns |
| Read address setup time in asynchronous mode | | 1.931 | | 2.272 | | ns |
| Read address hold time in synchronous mode | $T_{ADDRHD}$ | 0.121 | | 0.142 | | ns |
| Read address hold time in asynchronous mode | | –0.65 | | –0.76 | | ns |
| Read enable setup time | $T_{RDENSU}$ | 0.278 | | 0.327 | | ns |
| Read enable hold time | $T_{RDENHD}$ | 0.057 | | 0.067 | | ns |
| Read block select setup time | $T_{BLKSU}$ | 1.839 | | 2.163 | | ns |
| Read block select hold time | $T_{BLKHD}$ | –0.65 | | –0.77 | | ns |
| Read block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 2.09 | | 2.46 | ns |
| Read asynchronous reset removal time (pipelined clock) | $T_{RSTREM}$ | –0.02 | | –0.03 | | ns |
| Read asynchronous reset removal time (non-pipelined clock) | | 0.046 | | 0.054 | | ns |
| Read asynchronous reset recovery time (pipelined clock) | $T_{RSTREC}$ | 0.507 | | 0.597 | | ns |
| Read asynchronous reset recovery time (non-pipelined clock) | | 0.236 | | 0.278 | | ns |
| Read asynchronous reset to output propagation delay (with pipelined register enabled) | $T_{R2Q}$ | | 0.83 | | 0.98 | ns |
| Read synchronous reset setup time | $T_{SRSTSU}$ | 0.271 | | 0.319 | | ns |
| Read synchronous reset hold time | $T_{SRSTHD}$ | 0.061 | | 0.071 | | ns |
| Write clock period | $T_{CCY}$ | 4 | | 4 | | ns |
| Write clock minimum pulse width high | $T_{CCLKMPWH}$ | 1.8 | | 1.8 | | ns |
| Write clock minimum pulse width low | $T_{CCLKMPWL}$ | 1.8 | | 1.8 | | ns |
| Write block setup time | $T_{BLKCSU}$ | 0.404 | | 0.476 | | ns |
| Write block hold time | $T_{BLKCHD}$ | 0.007 | | 0.008 | | ns |
| Write input data setup time | $T_{DINCSU}$ | 0.101 | | 0.118 | | ns |
| Write input data hold time | $T_{DINCHD}$ | 0.137 | | 0.161 | | ns |
| Write address setup time | $T_{ADDRCSU}$ | 0.088 | | 0.104 | | ns |

***Table 259 •*** **2 Step IAP Programming (Fabric Only)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 302672 | 4 | 39 | 6 | Sec |
| 010 | 568784 | 7 | 45 | 12 | Sec |
| 025 | 1223504 | 14 | 55 | 23 | Sec |
| 050 | 2424832 | 29 | 74 | 40 | Sec |
| 060 | 2418896 | 39 | 83 | 50 | Sec |
| 090 | 3645968 | 60 | 106 | 73 | Sec |
| 150 | 6139184 | 100 | 154 | 120 | Sec |

***Table 260 •*** **2 Step IAP Programming (eNVM Only)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 137536 | 2 | 59 | 5 | Sec |
| 010 | 274816 | 4 | 98 | 11 | Sec |
| 025 | 274816 | 4 | 100 | 10 | Sec |
| 050 | 2,78,528 | 3 | 107 | 9 | Sec |
| 060 | 268480 | 5 | 98 | 22 | Sec |
| 090 | 544496 | 10 | 174 | 43 | Sec |
| 150 | 544496 | 10 | 175 | 44 | Sec |

***Table 261 •*** **2 Step IAP Programming (Fabric and eNVM)**

| M2S/M2GL Device | Image size Bytes | Authenticate | Program | Verify | Unit |
|---|---|---|---|---|---|
| 005 | 439296 | 6 | 78 | 11 | Sec |
| 010 | 842688 | 11 | 122 | 21 | Sec |
| 025 | 1497408 | 19 | 135 | 32 | Sec |
| 050 | 2695168 | 32 | 158 | 48 | Sec |
| 060 | 2686464 | 43 | 159 | 70 | Sec |
| 090 | 4190208 | 68 | 258 | 115 | Sec |
| 150 | 6682768 | 109 | 308 | 162 | Sec |

1. The minimum output clock frequency is limited by the PLL. For more information, see *UG0449: SmartFusion2 and IGLOO2 Clocking Resources User Guide*.
2. The PLL is used in conjunction with the Clock Conditioning Circuitry. Performance is limited by the CCC output frequency.

The following table lists the CCC/PLL jitter specifications in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 283 •*** **IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Jitter Specifications**

| **CCC Output Maximum Peak-to-Peak Period Jitter $F_{OUT\_CCC}$** | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Conditions/Package Combinations** | | | | | **Unit** |
| **10 FG484, 050 FG896/FG484/FCS325 Packages**[1] | SSO = 0 | 0 < SSO <= 2 | SSO <= 4 | SSO <= 8 | SSO <= 16 | |
| 20 MHz to 100 MHz | Max(110, ± 1% x (1/$F_{OUT\_CCC}$)) | Max(150, ± 1% x (1/$F_{OUT\_CCC}$)) | | | | ps |
| 100 MHz to 400 MHz | Max(120, ± 1% x (1/$F_{OUT\_CCC}$)) | Max(150, ± 1% x (1/$F_{OUT\_CCC}$)) | | | Max(170, ± 1% x (1/$F_{OUT\_CCC}$)) | ps |
| **025 FG484/FCS325 Package**[1] | 0 < SSO <=16 | | | | | |
| 20 MHz to 74 MHz | ± 1% x (1/$F_{OUT\_CCC}$)) | | | | | ps |
| 74 MHz to 400 MHz | 210 | | | | | ps |
| **005 FG484 Package**[1] | 0 < SSO <=16 | | | | | |
| 20 MHz to 53 MHz | ± 1% x (1/$F_{OUT\_CCC}$)) | | | | | ps |
| 53 MHz to 400 MHz | 270 | | | | | ps |
| **090 FG676 and FC325 Package**[1] | 0 < SSO <=16 | | | | | |
| 20 MHz to 100 MHz | ± 1% x (1/$F_{OUT\_CCC}$)) | | | | | ps |
| 100 MHz to 400 MHz | 150 | | | | | ps |
| **060 FG676 Package**[1] | 0 < SSO <=16 | | | | | |
| 20 MHz to 100 MHz | ± 1% x (1/$F_{OUT\_CCC}$) | | | | | ps |
| 100 MHz to 400 MHz | 150 | | | | | |
| **150 FC1152 Package**[1] | 0 < SSO <=16 | | | | | |
| 20 MHz to 100 MHz | ± 1% x (1/$F_{OUT\_CCC}$)) | | | | | ps |
| 100 MHz to 400 MHz | 120 | | | | | ps |

1. SSO data is based on LVCMOS 2.5 V MSIO and/or MSIOD bank I/Os.

## 2.3.30 SerDes Electrical and Timing AC and DC Characteristics

PCIe is a high-speed, packet-based, point-to-point, low-pin-count, serial interconnect bus. The IGLOO2 and SmartFusion2 SoC FPGAs has up to four hard high-speed serial interface blocks. Each SerDes block contains a PCIe system block. The PCIe system is connected to the SerDes block.

The following table lists the transmitter parameters in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 296 •*** **Transmitter Parameters**

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| VTX-DIFF-PP | Differential swing (2.5 Gbps, 5.0 Gbps) | 0.8 | 1.2 | V |
| VTX-CM-AC-P | Output common mode voltage (2.5 Gbps) | | 20 | mV |
| VTX-CM-AC-PP | Output common mode voltage (5.0 Gbps) | | 100 | mV |
| VTX-RISE-FALL | Rise and fall time (20% to 80%, 2.5 Gbps) | 0.125 | | UI |
| | Rise and fall time (20% to 80%, 5.0 Gbps) | 0.15 | | UI |
| ZTX-DIFF-DC | Output impedance–differential | 80 | 120 | Ω |
| LTX-SKEW | Lane-to-lane TX skew within a SerDes block (2.5 Gbps) | | 500 ps + 2 UI | ps |
| | Lane-to-lane TX skew within a SerDes block (5.0 Gbps) | | 500 ps + 4 UI | ps |
| RLTX-DIFF | Return loss differential mode (2.5 Gbps) | –10 | | dB |
| | Return loss differential mode (5.0 Gbps)<br>0.05 GHz to 1.25 GHz | –10 | | dB |
| | 1.25 GHz to 2.5 GHz | –8 | | dB |
| RLTX-CM | Return loss common mode (2.5 Gbps, 5.0 Gbps) | –6 | | dB |
| TX-LOCK-RST | Transmit PLL lock time from reset | | 10 | µs |
| VTX-AMP | 100 mV setting | 90 | 150 | mV |
| | 400 mV setting | 320 | 480 | mV |
| | 800 mV setting | 660 | 940 | mV |
| | 1200 mV setting | 950 | 1400 | mV |

### 2.3.31.3 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, see Figure 22, page 128.

The following table lists the SPI characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V

***Table 305 •*** **SPI Characteristics for All Devices**

| Symbol | Description | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| SPIFMAX | Maximum operating frequency of SPI interface | | | 20 | MHz | |
| sp1 | SPI_[0\|1]_CLK minimum period | | | | | |
| | SPI_[0\|1]_CLK = PCLK/2 | 12 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/4 | 24.1 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/8 | 48.2 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/16 | 0.1 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/32 | 0.19 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/64 | 0.39 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/128 | 0.77 | | | µs | |
| sp2 | SPI_[0\|1]_CLK minimum pulse width high | | | | | |
| | SPI_[0\|1]_CLK = PCLK/2 | 6 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/4 | 12.05 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/8 | 24.1 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/16 | 0.05 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/32 | 0.095 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/64 | 0.195 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/128 | 0.385 | | | µs | |
| sp3 | SPI_[0\|1]_CLK minimum pulse width low | | | | | |
| | SPI_[0\|1]_CLK = PCLK/2 | 6 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/4 | 12.05 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/8 | 24.1 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/16 | 0.05 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/32 | 0.095 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/64 | 0.195 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/128 | 0.385 | | | µs | |
| sp4 | SPI_[0\|1]_CLK, SPI_[0\|1]_DO, SPI_[0\|1]_SS rise time (10%–90%)[1] | | 2.77 | | ns | I/O Configuration: LVCMOS 2.5 V–8 mA<br>AC loading: 35 pF<br>Test conditions: Typical voltage, 25 °C |

## 2.3.34 MMUART Characteristics

The following table lists the MMUART characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 308 •*** **MMUART Characteristics**

| Parameter | Description | –1 | –Std | Unit |
|---|---|---|---|---|
| FMMUART_REF_CLK | Internally sourced MMUART reference clock frequency. | 166 | 142 | MHz |
| BAUDMMUARTTx | Maximum transmit baud rate | 10.375 | 8.875 | Mbps |
| BAUDMMUARTRx | Maximum receive baud rate | 10.375 | 8.875 | Mbps |

## 2.3.35 IGLOO2 Specifications

### 2.3.35.1 HPMS Clock Frequency

The following table lists the maximum frequency for HPMS main clock in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 309 •*** **Maximum Frequency for HPMS Main Clock**

| Symbol | Description | –1 | –Std | Unit |
|---|---|---|---|---|
| HPMS_CLK | Maximum frequency for the HPMS main clock | 166 | 142 | MHz |

### 2.3.35.2 IGLOO2 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_0_CLK. For timing parameter definitions, see Figure 23, page 131.

The following table lists the SPI characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 310 •*** **SPI Characteristics for All Devices**

| Symbol | Description | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| SPIFMAX | Maximum operating frequency of SPI interface | | | 20 | MHz | |
| sp1 | SPI_[0\|1]_CLK minimum period | | | | | |
| | SPI_[0\|1]_CLK = PCLK/2 | 12 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/4 | 24.1 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/8 | 48.2 | | | ns | |
| | SPI_[0\|1]_CLK = PCLK/16 | 0.1 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/32 | 0.19 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/64 | 0.39 | | | µs | |
| | SPI_[0\|1]_CLK = PCLK/128 | 0.77 | | | µs | |

***Table 310 •*** **SPI Characteristics for All Devices *(continued)***

| Symbol | Description | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| SPI master configuration (applicable for 060, 090, and 150 devices) | | | | | | |
| sp6m | SPI_[0\|1]_DO setup time[2] | (SPI_x_CLK_period/2) – 7.0 | | | ns | |
| sp7m | SPI_[0\|1]_DO hold time[2] | (SPI_x_CLK_period/2) – 9.5 | | | ns | |
| sp8m | SPI_[0\|1]_DI setup time[2] | 15 | | | ns | |
| sp9m | SPI_[0\|1]_DI hold time[2] | –2.5 | | | ns | |
| SPI slave configuration (applicable for 060, 090, and 150 devices) | | | | | | |
| sp6s | SPI_[0\|1]_DO setup time[2] | (SPI_x_CLK_period/2) – 16.0 | | | ns | |
| sp7s | SPI_[0\|1]_DO hold time[2] | (SPI_x_CLK_period/2) - 3.5 | | | ns | |
| sp8s | SPI_[0\|1]_DI setup time[2] | 3 | | | ns | |
| sp9s | SPI_[0\|1]_DI hold time[2] | 2.5 | | | ns | |

1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.
2. For allowable pclk configurations, see the Serial Peripheral Interface Controller section in the *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.

***Figure 23 •*** **SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)**