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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	27696
Total RAM Bits	1130496
Number of I/O	138
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LFBGA
Supplier Device Package	256-FPBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2gl025-1vfg256

Contents

1	Revision History	1
1.1	Revision 11.0	1
1.2	Revision 10.0	1
1.3	Revision 9.0	1
1.4	Revision 8.0	2
1.5	Revision 7.0	2
1.6	Revision 6.0	2
1.7	Revision 5.0	2
1.8	Revision 4.0	2
1.9	Revision 3.0	3
1.10	Revision 2.0	3
1.11	Revision 1.0	3
2	IGLOO2 FPGA and SmartFusion2 SoC FPGA	4
2.1	Device Status	4
2.2	References	5
2.3	Electrical Specifications	5
2.3.1	Operating Conditions	5
2.3.2	Power Consumption	12
2.3.3	Average Fabric Temperature and Voltage Derating Factors	14
2.3.4	Timing Model	15
2.3.5	User I/O Characteristics	17
2.3.6	Logic Element Specifications	75
2.3.7	Global Resource Characteristics	78
2.3.8	FPGA Fabric SRAM	79
2.3.9	Programming Times	94
2.3.10	Math Block Timing Characteristics	103
2.3.11	Embedded NVM (eNVM) Characteristics	104
2.3.12	SRAM PUF	105
2.3.13	Non-Deterministic Random Bit Generator (NRBG) Characteristics	106
2.3.14	Cryptographic Block Characteristics	106
2.3.15	Crystal Oscillator	107
2.3.16	On-Chip Oscillator	109
2.3.17	Clock Conditioning Circuits (CCC)	110
2.3.18	JTAG	112
2.3.19	System Controller SPI Characteristics	113
2.3.20	Power-up to Functional Times	114
2.3.21	DEVRST_N Characteristics	116
2.3.22	DEVRST_N to Functional Times	116
2.3.23	Flash*Freeze Timing Characteristics	119
2.3.24	DDR Memory Interface Characteristics	120
2.3.25	SFP Transceiver Characteristics	120
2.3.26	SerDes Electrical and Timing AC and DC Characteristics	121
2.3.27	SmartFusion2 Specifications	123
2.3.28	CAN Controller Characteristics	128
2.3.29	USB Characteristics	128
2.3.30	MMUART Characteristics	129
2.3.31	IGLOO2 Specifications	129

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 11.0

The following is a summary of the changes in revision 11.0 of this document.

- Updated [Table 24](#), page 22 with minimum and maximum values for input current low and high (SAR 73114 and 80314).
- Added [Non-Deterministic Random Bit Generator \(NRBG\) Characteristics](#), page 106 (SAR 73114 and 79517).
- Added 060 device in [Table 282](#), page 110 (SAR 79860).
- Added [DEVRST_N to Functional Times](#), page 116 (SAR 73114).
- Added [Cryptographic Block Characteristics](#), page 106 (SAR 73114 and 79516).
- Update [Table 296](#), page 121 with VTX-AMP details (SAR 81756).
- Update note in [Table 297](#), page 122 (SAR 74570 and 80677).
- Update [Table 298](#), page 122 with generic EPCS details (SAR 75307).
- Added [Table 308](#), page 129 (SAR 50424).

1.2 Revision 10.0

The following is a summary of the changes in revision 10.0 of this document.

- The Surge Current on VDD during DEVRST_B Assertion and Surge Current on VDD during Digest Check using System Services tables were deleted and added reference to [AC393: Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs Application Note](#). (SAR 76865 and 76623).
- Added 060 device in [Table 4](#), page 6 (SAR 76383).
- Updated [Table 24](#), page 22 for ramp time input (SAR 72103).
- Added 060 device details in [Table 284](#), page 112 (SAR 74927).
- Updated [Table 290](#), page 116 for name change (SAR 74925).
- Updated [Table 283](#), page 111 for 060 FG676 Package details (SAR 78849).
- Updated [Table 305](#), page 126 for SmartFusion2 and [Table 310](#), page 129 for IGLOO2 for SPI timing and Fmax (SAR 56645, 75331).
- Updated [Table 293](#), page 119 for Flash*Freeze entry and exit times (SAR 75329, 75330).
- Updated [Table 297](#), page 122 for RX-CID information (SAR 78271).
- Added [Table 8](#), page 8 and [Figure 1](#), page 9 (SAR 78932).
- Updated [Table 223](#), page 76 for timing characteristics and [Table 224](#), page 77 (SAR 75998).
- Added [SRAM PUF](#), page 105 (SAR 64406).
- Added a footnote on digest cycle in [Table 5](#), page 7 (SAR 79812).

1.3 Revision 9.0

The following is a summary of the changes in revision 9.0 of this document.

- Added a note in [Table 5](#), page 7 (SAR 71506).
- Added a note in [Table 6](#), page 8 (SAR 74616).
- Added a note in [Figure 3](#), page 17 (SAR 71506).
- Updated Quiescent Supply Current for 060 in [Table 11](#), page 12 and [Table 12](#), page 13 (SAR 74483).
- Updated programming currents for 060 in [Table 13](#), page 13, [Table 14](#), page 13, and [Table 15](#), page 14.
- Added DEVRST_B assertion tables (SAR 74708).
- Updated I/O speeds for LVDS 3.3 V in [Table 18](#), page 19 and [Table 21](#), page 20 (SAR 69829).
- Updated [Table 24](#), page 22 (SAR 69418).
- Updated [Table 25](#), page 22, [Table 26](#), page 23, [Table 27](#), page 23 (SAR 74570).
- Updated all AC/DC table to link to the [Input Capacitance, Leakage Current, and Ramp Time](#), page 22 for reference (SAR 69418).

where

- θ_{JA} = Junction-to-air thermal resistance
- θ_{JB} = Junction-to-board thermal resistance
- θ_{JC} = Junction-to-case thermal resistance
- T_J = Junction temperature
- T_A = Ambient temperature
- T_B = Board temperature (measured 1.0 mm away from the package edge)
- T_C = Case temperature
- P = Total power dissipated by the device

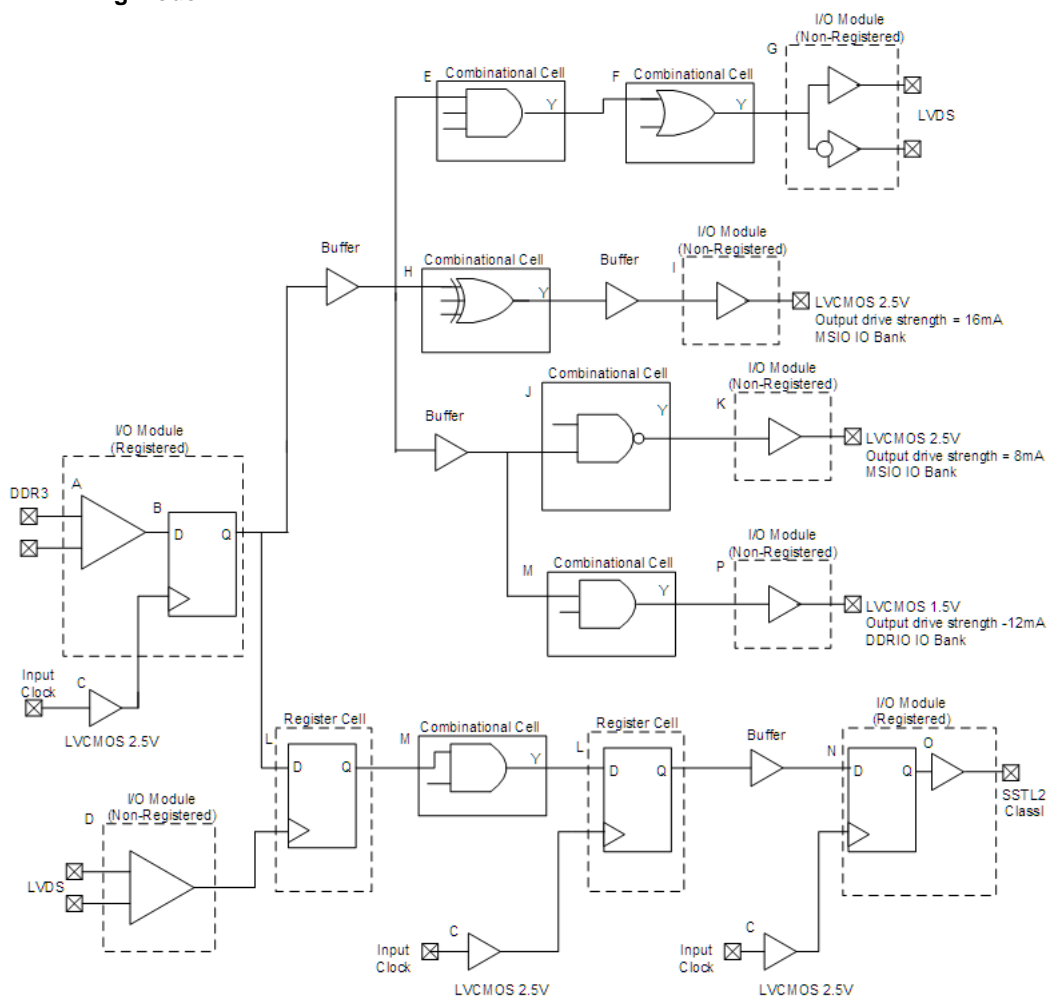
Table 9 • Package Thermal Resistance of SmartFusion2 and IGLOO2 Devices

Device	Still Air	1.0 m/s	2.5 m/s	θ_{JB}	θ_{JC}	Unit
	θ_{JA}					
005						
FG484	19.36	15.81	14.63	9.74	5.27	°C/W
VF256	41.30	38.16	35.30	28.41	3.94	°C/W
VF400	20.19	16.94	15.41	8.86	4.95	°C/W
TQ144	42.80	36.80	34.50	37.20	10.80	°C/W
010						
FG484	18.22	14.83	13.62	8.83	4.92	°C/W
VF256	37.36	34.26	31.45	24.84	7.89	°C/W
VF400	19.40	15.75	14.22	8.11	4.22	°C/W
TQ144	38.60	32.60	30.30	31.80	8.60	°C/W
025						
FG484	17.03	13.66	12.45	7.66	4.18	°C/W
VF256	33.85	30.59	27.85	21.63	6.13	°C/W
VF400	18.36	14.89	13.36	7.12	3.41	°C/W
FCS325	29.17	24.87	23.12	14.44	2.31	°C/W
050						
FG484	15.29	12.19	10.99	6.27	3.24	°C/W
FG896	14.70	12.50	10.90	7.20	4.90	°C/W
VF400	17.53	14.17	12.63	6.32	2.81	°C/W
FCS325	27.38	23.18	21.41	12.47	1.59	°C/W
060						
FG484	15.40	12.06	10.85	6.14	3.15	°C/W
FG676	15.49	12.21	11.06	7.07	3.87	°C/W
VF400	17.45	14.01	12.47	6.22	2.69	°C/W
FCS325	27.03	22.91	21.25	12.33	1.54	°C/W
090						
FG484	14.64	11.37	10.16	5.43	2.77	°C/W
FG676	14.52	11.19	10.37	6.17	3.24	°C/W
FCS325	26.63	22.26	20.13	14.24	2.50	°C/W

2.3.4 Timing Model

This section describes timing model and timing parameters.

Figure 2 • Timing Model



The following table lists the timing model parameters in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 17 • Timing Model Parameters

Index	Symbol	Description	-1	Unit	For More Information
A	T_{PY}	Propagation delay of DDR3 receiver	1.605	ns	See Table 137, page 50
B	T_{ICLKQ}	Clock-to-Q of the input data register	0.16	ns	See Table 221, page 71
	T_{ISUD}	Setup time of the input data register	0.357	ns	See Table 221, page 71
C	T_{RCKH}	Input high delay for global clock	1.53	ns	See Table 227, page 78
	T_{RCKL}	Input low delay for global clock	0.897	ns	See Table 227, page 78
D	T_{PY}	Input propagation delay of LVDS receiver	2.774	ns	See Table 167, page 56
E	T_{DP}	Propagation delay of a three-input AND gate	0.198	ns	See Table 223, page 76

Table 17 • Timing Model Parameters (continued)

Index	Symbol	Description	-1	Unit	For More Information
F	T_{DP}	Propagation delay of an OR gate	0.179	ns	See Table 223 , page 76
G	T_{DP}	Propagation delay of an LVDS transmitter	2.136	ns	See Table 169 , page 57
H	T_{DP}	Propagation delay of a three-input XOR Gate	0.241	ns	See Table 223 , page 76
I	T_{DP}	Propagation delay of LVCMOS 2.5 V transmitter, drive strength of 16 mA on the MSIO bank	2.412	ns	See Table 46 , page 27
J	T_{DP}	Propagation delay of a two-input NAND gate	0.179	ns	See Table 223 , page 76
K	T_{DP}	Propagation delay of LVCMOS 2.5 V transmitter, drive strength of 8 mA on the MSIO bank	2.309	ns	See Table 46 , page 27
L	T_{CLKQ}	Clock-to-Q of the data register	0.108	ns	See Table 224 , page 77
	T_{SUD}	Setup time of the data register	0.254	ns	See Table 224 , page 77
M	T_{DP}	Propagation delay of a two-input AND gate	0.179	ns	See Table 223 , page 76
N	T_{OCLKQ}	Clock-to-Q of the output data register	0.263	ns	See Table 220 , page 69
	T_{OSUD}	Setup time of the output data register	0.19	ns	See Table 220 , page 69
O	T_{DP}	Propagation delay of SSTL2, Class I transmitter on the MSIO bank	2.055	ns	See Table 114 , page 45
P	T_{DP}	Propagation delay of LVCMOS 1.5 V transmitter, drive strength of 12 mA, fast slew on the DDRIO bank	3.316	ns	See Table 70 , page 34

2.3.5.5 Detailed I/O Characteristics

Table 24 • Input Capacitance, Leakage Current, and Ramp Time

Symbol	Description	Maximum	Unit	Conditions
C_{IN}	Input capacitance	10	pF	
I_{IL} (dc)	Input current low (Applicable to HSTL/SSTL inputs only)	400	μ A	$V_{DDI} = 2.5$ V
		500	μ A	$V_{DDI} = 1.8$ V
		600	μ A	$V_{DDI} = 1.5$ V ¹
	Input current low (Applicable to all other digital inputs)	10	μ A	
I_{IH} (dc)	Input current high (Applicable to HSTL/SSTL inputs only)	400	μ A	$V_{DDI} = 2.5$ V
		500	μ A	$V_{DDI} = 1.8$ V
		600	μ A	$V_{DDI} = 1.5$ V ¹
	Input current high (Applicable to all other digital inputs)	10	μ A	
T_{RAMPIN} ²	Input ramp time (Applicable to all digital inputs)	50	ns	

1. Applicable when I/O pair is programmed with an HSTL/SSTL I/O type on IOP and an un-terminated I/O type (LVCMOS, for example) on ION pad.
2. Voltage ramp must be monotonic.

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of DDRIO I/O bank at V_{OH}/V_{OL} Level.

Table 25 • I/O Weak Pull-up/Pull-down Resistances for DDRIO I/O Bank

V_{DDI} Domain	R(WEAK PULL-UP) at V_{OH} (Ω)		R(WEAK PULL-DOWN) at V_{OL} (Ω)	
	Min	Max	Min	Max
2.5 V ^{1, 2}	10K	17.8K	9.98K	18K
1.8 V ^{1, 2}	10.3K	19.1K	10.3K	19.5K
1.5 V ^{1, 2}	10.6K	20.2K	10.6K	21.1K
1.2 V ^{1, 2}	11.1K	22.7K	11.2K	24.6K

1. $R(\text{WEAK PULL-DOWN}) = (V_{OLspec})/I(\text{WEAK PULL-DOWN MAX})$.
2. $R(\text{WEAK PULL-UP}) = (V_{DDImax} - V_{OHspec})/I(\text{WEAK PULL-UP MIN})$.

Table 53 • LVCMOS 1.8 V AC Calibrated Impedance Option

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	Rodt_cal	75, 60, 50, 33, 25, 20	Ω

Table 54 • LVCMOS 1.8 V AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V _{TRIP}	0.9	V
Resistance for enable path (T _{ZH} , T _{ZL} , T _{HZ} , T _{LZ})	R _{ENT}	2k	Ω
Capacitive loading for enable path (T _{ZH} , T _{ZL} , T _{HZ} , T _{LZ})	C _{ENT}	5	pF
Capacitive loading for data path (T _{DP})	C _{LOAD}	5	pF

Table 55 • LVCMOS 1.8 V Transmitter Drive Strength Specifications

Output Drive Selection			V _{OH} (V)	V _{OL} (V)	IOH (at V _{OH})	IOL (at V _{OL})
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min	Max	mA	mA
2 mA	2 mA	2 mA	V _{DDI} - 0.45	0.45	2	2
4 mA	4 mA	4 mA	V _{DDI} - 0.45	0.45	4	4
6 mA	6 mA	6 mA	V _{DDI} - 0.45	0.45	6	6
8 mA	8 mA	8 mA	V _{DDI} - 0.45	0.45	8	8
10 mA	10 mA	10 mA	V _{DDI} - 0.45	0.45	10	10
12 mA		12 mA	V _{DDI} - 0.45	0.45	12	12
		16 mA ¹	V _{DDI} - 0.45	0.45	16	16

1. 16 mA drive strengths, all slews, meets LPDDR JEDEC electrical compliance.

AC Switching Characteristics

Worst commercial-case conditions: T_J = 85 °C, V_{DD} = 1.14 V, V_{DDI} = 1.71 V

Table 56 • LVCMOS 1.8 V Receiver Characteristics (Input Buffers)

	On-Die Termination (ODT)	T _{py}		T _{pys}		Unit
		-1	-Std	-1	-Std	
LVCMOS 1.8 V (for DDRIO I/O bank with Fixed Codes)	None	1.968	2.315	2.099	2.47	ns
	None	2.898	3.411	2.883	3.393	ns
	50	3.05	3.59	3.044	3.583	ns
LVCMOS 1.8 V (for MSIO I/O bank)	75	2.999	3.53	2.987	3.516	ns
	150	2.947	3.469	2.933	3.452	ns
	None	2.611	3.071	2.598	3.057	ns
LVCMOS 1.8 V (for MSIOD I/O bank)	50	2.775	3.264	2.775	3.265	ns
	75	2.72	3.2	2.712	3.19	ns
	150	2.666	3.137	2.655	3.123	ns
	None	2.611	3.071	2.598	3.057	ns

Table 58 • LVCMOS 1.8 V Transmitter Characteristics for MSIO I/O Bank

Output Drive Selection	Slew Control	T _{DP}		T _{ZL}		T _{ZH}		T _{HZ} ¹		T _{LZ} ¹		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	3.441	4.047	4.165	4.9	4.413	5.192	4.891	5.755	5.138	6.044	ns
4 mA	Slow	3.218	3.786	3.642	4.284	3.941	4.636	5.665	6.665	5.568	6.551	ns
6 mA	Slow	3.141	3.694	3.501	4.118	3.823	4.498	6.587	7.75	6.032	7.096	ns
8 mA	Slow	3.165	3.723	3.319	3.904	3.654	4.298	6.898	8.115	6.216	7.313	ns
10 mA	Slow	3.202	3.767	3.278	3.857	3.616	4.254	7.25	8.529	6.435	7.571	ns
12 mA	Slow	3.277	3.855	3.175	3.736	3.519	4.139	7.392	8.697	6.538	7.692	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 59 • LVCMOS 1.8 V Transmitter Characteristics for MSIOD I/O Bank

Output Drive Selection	Slew Control	T _{DP}		T _{ZL}		T _{ZH}		T _{HZ} ¹		T _{LZ} ¹		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	2.725	3.206	3.316	3.901	3.484	4.099	5.204	6.123	4.997	5.88	ns
4 mA	Slow	2.242	2.638	2.777	3.267	2.947	3.466	5.729	6.74	5.448	6.41	ns
6 mA	Slow	1.995	2.347	2.466	2.901	2.63	3.094	6.372	7.496	5.987	7.043	ns
8 mA	Slow	2.001	2.354	2.44	2.87	2.6	3.058	6.633	7.804	6.193	7.286	ns
10 mA	Slow	2.025	2.382	2.312	2.719	2.47	2.906	6.94	8.165	6.412	7.544	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

2.3.5.9 1.5 V LVCMOS

LVCMOS 1.5 is a general standard for 1.5 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-11A.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 60 • LVCMOS 1.5 V DC Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{DDI}	1.425	1.5	1.575	V

Table 61 • LVCMOS 1.5 V DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC input logic high for (MSIOD and DDRIO I/O banks)	V _{IH} (DC)	0.65 × V _{DDI}	1.575	V
DC input logic high (for MSIO I/O bank)	V _{IH} (DC)	0.65 × V _{DDI}	3.45	V
DC input logic low	V _{IL} (DC)	-0.3	0.35 × V _{DDI}	V
Input current high ¹	I _{IH} (DC)			-
Input current low ¹	I _{IL} (DC)			-

1. See Table 24, page 22.

2.3.6.6 Low Power Double Data Rate (LPDDR)

LPDDR reduced and full drive low power double data rate standards are supported in IGLOO2 FPGA and SmartFusion2 SoC FPGA I/Os. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 139 • LPDDR DC Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max
Supply voltage	V_{DDI}	1.71	1.8	1.89
Termination voltage	V_{TT}	0.838	0.900	0.964
Input reference voltage	V_{REF}	0.838	0.900	0.964

Table 140 • LPDDR DC Input Voltage Specification

Parameter	Symbol	Min	Max
DC input logic high	V_{IH} (DC)	$0.7 \times V_{DDI}$	1.89
DC input logic low	V_{IL} (DC)	-0.3	$0.3 \times V_{DDI}$
Input current high ¹	I_{IH} (DC)		
Input current low ¹	I_{IL} (DC)		

1. See Table 24, page 22.

Table 141 • LPDDR DC Output Voltage Specification Reduced Drive

Parameter	Symbol	Min	Max
DC output logic high	V_{OH}	$0.9 \times V_{DDI}$	
DC output logic low	V_{OL}		$0.1 \times V_{DDI}$
Output minimum source DC current	I_{OH} at V_{OH}	0.1	
Output minimum sink current	I_{OL} at V_{OL}	-0.1	

Table 142 • LPDDR DC Output Voltage Specification Full Drive¹

Parameter	Symbol	Min	Max
DC output logic high	V_{OH}	$0.9 \times V_{DDI}$	
DC output logic low	V_{OL}		$0.1 \times V_{DDI}$
Output minimum source DC current	I_{OH} at V_{OH}	0.1	
Output minimum sink current	I_{OL} at V_{OL}	-0.1	

1. To meet JEDEC Electrical Compliance, use LPDDR Full Drive Transmitter.

Table 143 • LPDDR DC Differential Voltage Specification

Parameter	Symbol	Min
DC input differential voltage	V_{ID} (DC)	$0.4 \times V_{DDI}$

Table 185 • M-LVDS DC Voltage Specification Output Voltage Specification (for MSIO I/O Bank Only)

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V_{OH}	1.25	1.425	1.6	V
DC output logic low	V_{OL}	0.9	1.075	1.25	V

Table 186 • M-LVDS Differential Voltage Specification

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing (for MSIO I/O bank only)	V_{OD}	300	650	mV
Output common mode voltage (for MSIO I/O bank only)	V_{OCM}	0.3	2.1	V
Input common mode voltage	V_{ICM}	0.3	1.2	V
Input differential voltage	V_{ID}	50	2400	mV

Table 187 • M-LVDS Minimum and Maximum AC Switching Speed for MSIO I/O Bank

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	D_{MAX}	500	Mbps	AC loading: 2 pF / 100 Ω differential load

Table 188 • M-LVDS AC Impedance Specifications

Parameter	Symbol	Typ	Unit
Termination resistance	R_T	50	Ω

Table 189 • M-LVDS AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	Cross point	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF

AC Switching Characteristics

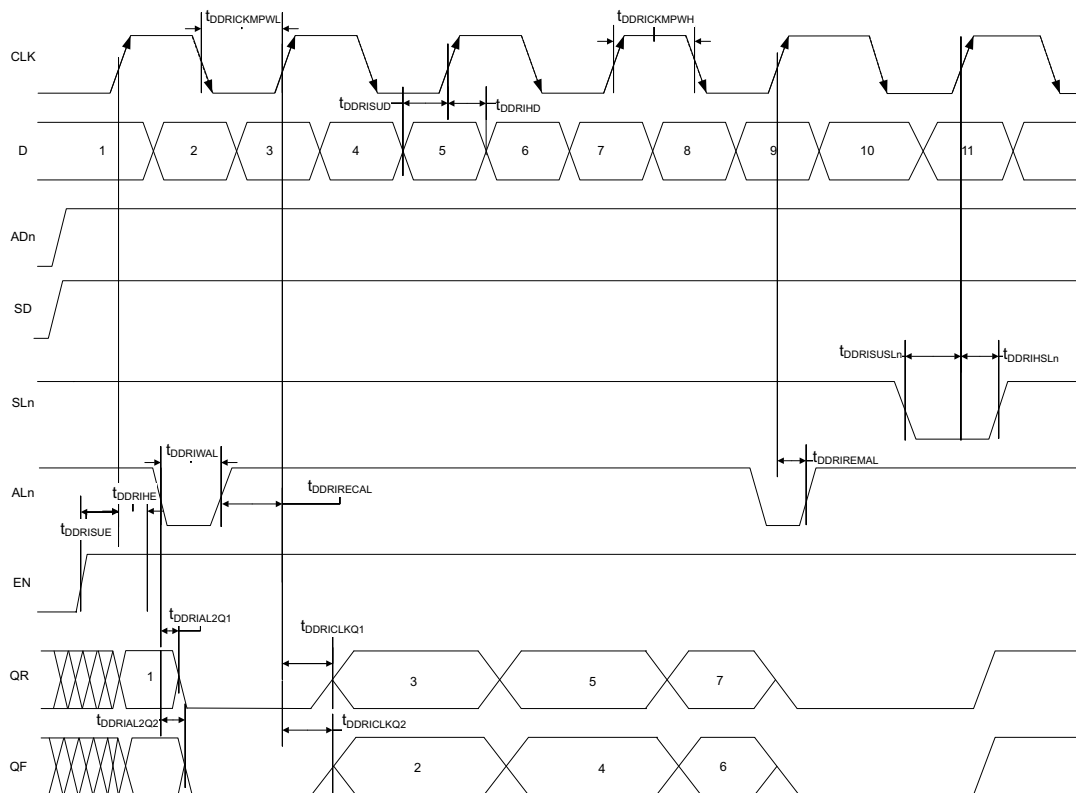
Worst commercial-case conditions: $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

Table 190 • M-LVDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)

On-Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.738	3.221	ns
100	2.735	3.218	ns

2.3.9.2 Input DDR Timing Diagram

Figure 11 • Input DDR Timing Diagram



2.3.9.3 Timing Characteristics

The following table lists the input DDR propagation delays in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 221 • Input DDR Propagation Delays

Symbol	Description	Measuring Nodes (from, to)	-1	-Std	Unit
$T_{DDRICKQ1}$	Clock-to-Out Out_QR for input DDR	B, C	0.16	0.188	ns
$T_{DDRICKQ2}$	Clock-to-Out Out_QF for input DDR	B, D	0.166	0.195	ns
$T_{DDRISUD}$	Data setup for input DDR	A, B	0.357	0.421	ns
T_{DDRHD}	Data hold for input DDR	A, B	0	0	ns
$T_{DDRISUE}$	Enable setup for input DDR	E, B	0.46	0.542	ns
T_{DDRHE}	Enable hold for input DDR	E, B	0	0	ns
$T_{DDRISUSL}$	Synchronous load setup for input DDR	G, B	0.46	0.542	ns
T_{DDRHSL}	Synchronous load hold for input DDR	G, B	0	0	ns
$T_{DDRIAL2Q1}$	Asynchronous load-to-out QR for input DDR	F, C	0.587	0.69	ns
$T_{DDRIAL2Q2}$	Asynchronous load-to-out QF for input DDR	F, D	0.541	0.636	ns
$T_{DDRIREMAL}$	Asynchronous load removal time for input DDR	F, B	0	0	ns
$T_{DDRIRECAL}$	Asynchronous load recovery time for input DDR	F, B	0.074	0.087	ns

2.3.10.2 Timing Characteristics

The following table lists the combinatorial cell propagation delays in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

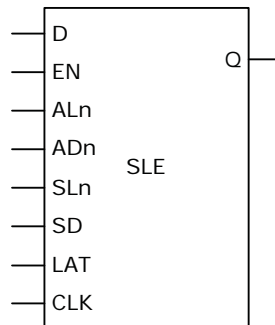
Table 223 • Combinatorial Cell Propagation Delays

Combinatorial Cell	Equation	Symbol	-1	-Std	Unit
INV	$Y = !A$	T_{PD}	0.1	0.118	ns
AND2	$Y = A \cdot B$	T_{PD}	0.164	0.193	ns
NAND2	$Y = !(A \cdot B)$	T_{PD}	0.147	0.173	ns
OR2	$Y = A + B$	T_{PD}	0.164	0.193	ns
NOR2	$Y = !(A + B)$	T_{PD}	0.147	0.173	ns
XOR2	$Y = A \oplus B$	T_{PD}	0.164	0.193	ns
XOR3	$Y = A \oplus B \oplus C$	T_{PD}	0.225	0.265	ns
AND3	$Y = A \cdot B \cdot C$	T_{PD}	0.209	0.246	ns
AND4	$Y = A \cdot B \cdot C \cdot D$	T_{PD}	0.287	0.338	ns

2.3.10.3 Sequential Module

IGLOO2 and SmartFusion2 SoC FPGAs offer a separate flip-flop which can be used independently from the LUT. The flip-flop can be configured as a register or a latch and has a data input and optional enable, synchronous load (clear or preset), and asynchronous load (clear or preset).

Figure 15 • Sequential Module



The following table lists the 010 device global resources in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 229 • 010 Device Global Resource

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	T_{RCKL}	0.626	0.669	0.627	0.668	ns
Input high delay for global clock	T_{RCKH}	1.112	1.182	1.308	1.393	ns
Maximum skew for global clock	T_{RCKSW}		0.07		0.085	ns

The following table lists the 005 device global resources in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 230 • 005 Device Global Resource

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input low delay for global clock	T_{RCKL}	0.625	0.66	0.628	0.66	ns
Input high delay for global clock	T_{RCKH}	1.126	1.187	1.325	1.397	ns
Maximum skew for global clock	T_{RCKSW}		0.061		0.072	ns

2.3.12 FPGA Fabric SRAM

See [UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide](#) for more information.

2.3.12.1 FPGA Fabric Large SRAM (LSRAM)

The following table lists the RAM1K18 – dual-port mode for depth \times width configuration $1\text{K} \times 18$ in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 231 • RAM1K18 – Dual-Port Mode for Depth \times Width Configuration $1\text{K} \times 18$

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Clock period	T_{CY}	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	T_{PLCY}	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register				0.334	0.393	ns
Read access time without pipeline register	T_{CLK2Q}			2.273	2.674	ns
Access time with feed-through write timing				1.529	1.799	ns
Address setup time	T_{ADDRSU}	0.441		0.519		ns
Address hold time	T_{ADDRHD}	0.274		0.322		ns
Data setup time	T_{DSU}	0.341		0.401		ns
Data hold time	T_{DHD}	0.107		0.126		ns
Block select setup time	T_{BLKSU}	0.207		0.244		ns

Table 245 • JTAG Programming (eNVM Only)

M2S/M2GL				
Device	Image size Bytes	Program	Verify	Unit
005	137536	39	4	Sec
010	274816	78	9	Sec
025	274816	78	9	Sec
050	278528	84	8	Sec
060	268480	76	8	Sec
090	544496	154	15	Sec
150	544496	155	15	Sec

Table 246 • JTAG Programming (Fabric and eNVM)

M2S/M2GL				
Device	Image size Bytes	Program	Verify	Unit
005	439296	59	11	Sec
010	842688	107	20	Sec
025	1497408	120	35	Sec
050	2695168	162	59	Sec
060	2686464	158	70	Sec
090	4190208	266	147	Sec
150	6682768	316	231	Sec

Table 247 • 2 Step IAP Programming (Fabric Only)

M2S/M2GL					
Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	302672	4	17	6	Sec
010	568784	7	23	12	Sec
025	1223504	14	33	23	Sec
050	2424832	29	52	40	Sec
060	2418896	39	61	50	Sec
090	3645968	60	84	73	Sec
150	6139184	100	132	120	Sec

The following table lists the math blocks with input register used and output in bypass mode in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 270 • Math Block with Input Register Used and Output in Bypass Mode

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input register setup time	T_{MISU}	0.149		0.176		ns
Input register hold time	T_{MIHD}	0.185		0.218		ns
Synchronous reset/enable setup time	$T_{MSRSTENSU}$	0.08		0.094		ns
Synchronous reset/enable hold time	$T_{MSRSTENHD}$	-0.012		-0.014		ns
Asynchronous reset removal time	$T_{MARSTREM}$	-0.005		-0.005		ns
Asynchronous reset recovery time	$T_{MARSTREC}$	0.088		0.104		ns
Input register clock to output delay	T_{MICQ}		2.52		2.964	ns
CDIN to output delay	$T_{MCDIN2Q}$		1.951		2.295	ns

The following table lists the math blocks with input and output in bypass mode in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 271 • Math Block with Input and Output in Bypass Mode

Parameter	Symbol	-1	-Std	Unit
		Max	Max	
Input to output delay	T_{MIQ}	2.568	3.022	ns
CDIN to output delay	$T_{MCDIN2Q}$	1.951	2.295	ns

2.3.15 Embedded NVM (eNVM) Characteristics

The following table lists the eNVM read performance in worst-case conditions when $V_{DD} = 1.14\text{ V}$, $V_{PPNVM} = V_{PP} = 2.375\text{ V}$.

Table 272 • eNVM Read Performance

Symbol	Description	Operating Temperature Range						Unit
		-1	-Std	-1	-Std	-1	-Std	
T_J	Junction temperature range	-55 °C to 125 °C		-40 °C to 100 °C		0 °C to 85 °C		°C
$F_{MAXREAD}$	eNVM maximum read frequency	25	25	25	25	25	25	MHz

The following table lists the eNVM page programming in worst-case conditions when $V_{DD} = 1.14\text{ V}$, $V_{PPNVM} = V_{PP} = 2.375\text{ V}$.

Table 273 • eNVM Page Programming

Symbol	Description	Operating Temperature Range						Unit
		-1	-Std	-1	-Std	-1	-Std	
T_J	Junction temperature range	-55 °C to 125 °C		-40 °C to 100 °C		0 °C to 85 °C		°C
$T_{PAGEPGM}$	eNVM page programming time	40	40	40	40	40	40	ms

The following table lists the system controller characteristics in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 286 • System Controller SPI Characteristics for All Devices

Symbol	Description	Conditions	Min	Typ	Unit
sp1	SC_SPI_SCK minimum period		20		ns
sp2	SC_SPI_SCK minimum pulse width high		10		ns
sp3	SC_SPI_SCK minimum pulse width low		10		ns
sp4 ¹	SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS rise time (10%–90%) 1	I/O configuration: LVTTTL 3.3 V–20 mA AC loading: 35 pF Test conditions: Typical voltage, 25 °C		1.239	ns
sp5 ¹	SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS fall time (10%–90%) 1	I/O configuration: LVTTTL 3.3 V–20 mA AC loading: 35 pF Test conditions: Typical voltage, 25 °C		1.245	ns
sp6	Data from master (SC_SPI_SDO) setup time		160		ns
sp7	Data from master (SC_SPI_SDO) hold time		160		ns
sp8	SC_SPI_SDI setup time		20		ns
sp9	SC_SPI_SDI hold time		20		ns

1. For specific Rise/Fall Times, board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>. Use the supported I/O Configurations for the System Controller SPI in the following table.

Table 287 • Supported I/O Configurations for System Controller SPI (for MSIO Bank Only)

Voltage Supply	I/O Drive Configuration	Unit
3.3 V	20	mA
2.5 V	16	mA
1.8 V	12	mA
1.5 V	8	mA
1.2 V	4	mA

2.3.24 Power-up to Functional Times

The following table lists the SmartFusion2 power-up to functional times in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 288 • Power-up to Functional Times for SmartFusion2

Symbol	From	To	Description	Maximum Power-up to Functional Time for SmartFusion2 (uS)						
				005	010	025	050	060	090	150
$T_{POR2OUT}$	POWER_ON_RESET_N	Output available at I/O	Fabric to output	647	500	531	483	474	524	647
$T_{POR2MSSRST}$	POWER_ON_RESET_N	MSS_RESE T_N_M2F	Fabric to MSS	644	497	528	480	468	518	641
$T_{MSSRST2OUT}$	MSS_RESET_N_M2F	Output available at I/O	MSS to output	3.6	3.6	3.6	3.4	4.9	4.8	4.8
$T_{VDD2OUT}$	V_{DD}	Output available at I/O	V_{DD} at its minimum threshold level to output	3096	2975	3012	2959	2869	2992	3225
$T_{VDD2POR}$	V_{DD}	POWER_ON_RESET_N	V_{DD} at its minimum threshold level to fabric	2476	2487	2496	2486	2406	2563	2602
$T_{VDD2MSSRST}$	V_{DD}	MSS_RESE T_N_M2F	V_{DD} at its minimum threshold level to MSS	3093	2972	3008	2956	2864	2987	3220
$T_{VDD2WPU}$	DEVRST_N	DDRIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2500	2487	2509	2475	2507	2519	2617
	DEVRST_N	MSIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	2504	2491	2510	2478	2517	2525	2620
	DEVRST_N	MSIOD Inbuf weak pull	DEVRST_N to Inbuf weak pull	2479	2468	2493	2458	2486	2499	2595

Note: For more information about power-up times, see [UG0331: SmartFusion2 Microcontroller Subsystem User Guide](#).

The following table lists the receiver pa in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 297 • Receiver Parameters

Symbol	Description	Min	Typ	Max	Unit
VRX-IN-PP-CC	Differential input peak-to-peak sensitivity (2.5 Gbps)	0.238		1.2	V
	Differential input peak-to-peak sensitivity (2.5 Gbps, de-emphasized)	0.219		1.2	V
	Differential input peak-to-peak sensitivity (5.0 Gbps)	0.300		1.2	V
	Differential input peak-to-peak sensitivity (5.0 Gbps, de-emphasized)	0.300		1.2	V
VRX-CM-AC-P	Input common mode range (AC coupled)			150	mV
ZRX-DIFF-DC	Differential input termination	80	100	120	Ω
REXT	External calibration resistor	1,188	1,200	1,212	Ω
CDR-LOCK-RST	CDR relock time from reset			15	μs
RLRX-DIFF	Return loss differential mode (2.5 Gbps)	-10			dB
	Return loss differential mode (5.0 Gbps)				
	0.05 GHz to 1.25 GHz	-10			dB
	1.25 GHz to 2.5 GHz	-8			dB
RLRX-CM	Return loss common mode (2.5 Gbps, 5.0 Gbps)	-6			dB
RX-CID ¹	CID limit PCIe Gen1/2			200	UI
VRX-IDLE-DET-DIFF-PP	Signal detect limit	65		175	mV

1. AC-coupled, BER = e^{-12} , using synchronous clock.

Table 298 • SerDes Protocol Compliance

Protocol	Maximum Data Rate (Gbps)	-1	-Std
PCIe Gen 1	2.5	Yes	Yes
PCIe Gen 2	5.0	Yes	
XAUI	3.125	Yes	
Generic EPCS	3.2	Yes	
Generic EPCS	2.5	Yes	Yes

The following table lists the SerDes reference clock AC specifications in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 299 • SerDes Reference Clock AC Specifications

Parameter	Symbol	Min	Max	Unit
Reference clock frequency	F_{REFCLK}	100	160	MHz
Reference clock rise time	T_{RISE}	0.6	4	V/ns
Reference clock fall time	T_{FALL}	0.6	4	V/ns
Reference clock duty cycle	T_{CYC}	40	60	%
Reference clock mismatch	$M_{MREFCLK}$	-300	300	ppm
Reference spread spectrum clock	SSC_{ref}	0	5000	ppm

Table 300 • HCSL Minimum and Maximum DC Input Levels (Applicable to SerDes REFCLK Only)

Parameter	Symbol	Min	Typ	Max	Unit
Recommended DC Operating Conditions					
Supply voltage	V_{DDI}	2.375	2.5	2.625	V
HCSL DC Input Voltage Specification					
DC Input voltage	V_I	0		2.625	V
HCSL Differential Voltage Specification					
Input common mode voltage	V_{ICM}	0.05		2.4	V
Input differential voltage	V_{IDIFF}	100		1100	mV

Table 301 • HCSL Minimum and Maximum AC Switching Speeds (Applicable to SerDes REFCLK Only)

Parameter	Symbol	Min	Typ	Max	Unit
HCSL AC Specifications					
Maximum data rate (for MSIO I/O bank)	F_{MAX}			350	Mbps
HCSL Impedance Specifications					
Termination resistance	R_t		100		Ω

2.3.31 SmartFusion2 Specifications

2.3.31.1 MSS Clock Frequency

The following table lists the maximum frequency for MSS main clock in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 302 • Maximum Frequency for MSS Main Clock

Symbol	Description	-1	-Std	Unit
M3_CLK	Maximum frequency for the MSS main clock	166	142	MHz

2.3.31.2 SmartFusion2 Inter-Integrated Circuit (I²C) Characteristics

This section describes the DC and switching of the I²C interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, see [Figure 21](#), page 125.

The following table lists the I²C characteristics in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Table 303 • I²C Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input low voltage	V_{IL}	-0.3		0.8	V	See Single-Ended I/O Standards , page 24 for more information. I/O standard used for illustration: MSIO bank-LVTTL 8 mA low drive.
Input high voltage	V_{IH}	2		3.45	V	See Single-Ended I/O Standards , page 24 for more information. I/O standard used for illustration: MSIO bank-LVTTL 8 mA low drive.
Hysteresis of schmitt triggered inputs for $V_{DDI} > 2\text{ V}$	V_{HYS}	$0.05 \times V_{DDI}$			V	See Table 28 , page 23 for more information.
Input current high	I_{IL}			10	μA	See Single-Ended I/O Standards , page 24 for more information.
Input current low	I_{IH}			10	μA	See Single-Ended I/O Standards , page 24 for more information.
Input rise time	T_{ir}			1000	ns	Standard mode
				300	ns	Fast mode
Input fall time	T_{if}			300	ns	Standard mode
				300	ns	Fast mode
Maximum output voltage low (open drain) at 3 mA sink current for $V_{DDI} > 2\text{ V}$	V_{OL}			0.4	V	See Single-Ended I/O Standards , page 24 for more information. I/O standard used for illustration: MSIO bank-LVTTL 8 mA low drive.
Pin capacitance	C_{in}			10	pF	$V_{IN} = 0$, $f = 1.0\text{ MHz}$
Output fall time from V_{IHMin} to V_{ILMax}^1	t_{OF}^1		21.04		ns	V_{IHmin} to V_{ILMax} , $C_{LOAD} = 400\text{ pF}$
			5.556		ns	V_{IHmin} to V_{ILMax} , $C_{LOAD} = 100\text{ pF}$
Output rise time from V_{ILMax} to V_{IHMin}^1	t_{OR}^1		19.887		ns	V_{ILMax} to V_{IHmin} , $C_{LOAD} = 400\text{ pF}$
			5.218		ns	V_{ILMax} to V_{IHmin} , $C_{LOAD} = 100\text{ pF}$
Output buffer maximum pull-down resistance ^{2,3}	$R_{pull-up}^{2,3}$			50	Ω	
Output buffer maximum pull-up resistance ^{2,4}	$R_{pull-down}^{2,4}$			131.25	Ω	