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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	27696
Total RAM Bits	1130496
Number of I/O	138
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LFBGA
Supplier Device Package	256-FPBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2gl025-1vfg256i

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2.2 References

The following documents are recommended references:

- *PB0121: IGLOO2 Product Brief*
- *DS0124: IGLOO2 Pin Descriptions*
- *PB0115: SmartFusion2 SoC FPGA Product Brief*
- *DS0115: SmartFusion2 Pin Descriptions*

All product documentation for IGLOO2 and SmartFusion2 is available at:

<http://www.microsemi.com/products/fpga-soc/fpga/igloo2-fpga>

<http://www.microsemi.com/products/fpga-soc/soc-fpga/smartfusion2#overview>

2.3 Electrical Specifications

2.3.1 Operating Conditions

The following table lists the stress limits. Stress applied above the specified limit may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in the following table are not implied.

Table 3 • Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
DC core supply voltage. Must always power this pin.	V_{DD}	-0.3	1.32	V
Power supply for charge pumps (for normal operation and programming). Must always power this pin.	V_{PP}	-0.3	3.63	V
Analog power pad for MDDR PLL	MSS_MDDR_PLL_VDDA	-0.3	3.63	V
Analog power pad for MDDR PLL	HPMS_MDDR_PLL_VDDA	-0.3	3.63	V
Analog power pad for FDDR PLL	FDDR_PLL_VDDA	-0.3	3.63	V
Analog power pad for MDDR PLL	PLL0_PLL1_MSS_MDDR_VDDA	-0.3	3.63	V
Analog power pad for MDDR PLL	PLL0_PLL1_HPMS_MDDR_VDDA	-0.3	3.63	V
Analog power pad for PLL0-5	CCC_XX[01]_PLL_VDDA	-0.3	3.63	V
High supply voltage for PLL SerDes[01]	SERDES_[01]_PLL_VDDA	-0.3	3.63	V
Analog power for SerDes[01] PLL lane0 to lane3. This is a 2.5 V SerDes internal PLL supply.	SERDES_[01]_L[0123]_VDDAPLL	-0.3	2.75	V
TX/RX analog I/O voltage. Low voltage power for the lanes of SerDesIF0. This is a 1.2 V SerDes PMA supply.	SERDES_[01]_L[0123]_VDDAIO	-0.3	1.32	V
PCIe/PCS power supply	SERDES_[01]_VDD	-0.3	1.32	V
DC FPGA I/O buffer supply voltage for MSIO I/O bank	V_{DDIx}	-0.3	3.63	V
DC FPGA I/O buffer supply voltage for MSIOD/DDRIO I/O banks	V_{DDIx}	-0.3	2.75	V
I/O Input voltage for MSIO I/O bank	V_I	-0.3	3.63	V
I/O Input voltage for MSIOD/DDRIO I/O bank	V_I	-0.3	2.75	V
Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to V_{PP} .	V_{PPNVM}	-0.3	3.63	V
Storage temperature ¹	T_{STG}	-65	150	°C
Junction temperature	T_J	-55	135	°C

2.3.4 Timing Model

This section describes timing model and timing parameters.

Figure 2 • Timing Model

The following table lists the timing model parameters in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 17 • Timing Model Parameters

Index	Symbol	Description	-1	Unit	For More Information
A	T_{PY}	Propagation delay of DDR3 receiver	1.605	ns	See Table 137, page 50
B	T_{ICLKQ}	Clock-to-Q of the input data register	0.16	ns	See Table 221, page 71
	T_{ISUD}	Setup time of the input data register	0.357	ns	See Table 221, page 71
C	T_{RCKH}	Input high delay for global clock	1.53	ns	See Table 227, page 78
	T_{RCKL}	Input low delay for global clock	0.897	ns	See Table 227, page 78
D	T_{PY}	Input propagation delay of LVDS receiver	2.774	ns	See Table 167, page 56
E	T_{DP}	Propagation delay of a three-input AND gate	0.198	ns	See Table 223, page 76

Table 17 • Timing Model Parameters (continued)

Index	Symbol	Description	-1	Unit	For More Information
F	T_{DP}	Propagation delay of an OR gate	0.179	ns	See Table 223, page 76
G	T_{DP}	Propagation delay of an LVDS transmitter	2.136	ns	See Table 169, page 57
H	T_{DP}	Propagation delay of a three-input XOR Gate	0.241	ns	See Table 223, page 76
I	T_{DP}	Propagation delay of LVCMOS 2.5 V transmitter, drive strength of 16 mA on the MSIO bank	2.412	ns	See Table 46, page 27
J	T_{DP}	Propagation delay of a two-input NAND gate	0.179	ns	See Table 223, page 76
K	T_{DP}	Propagation delay of LVCMOS 2.5 V transmitter, drive strength of 8 mA on the MSIO bank	2.309	ns	See Table 46, page 27
L	T_{CLKQ}	Clock-to-Q of the data register	0.108	ns	See Table 224, page 77
	T_{SUD}	Setup time of the data register	0.254	ns	See Table 224, page 77
M	T_{DP}	Propagation delay of a two-input AND gate	0.179	ns	See Table 223, page 76
N	T_{OCLKQ}	Clock-to-Q of the output data register	0.263	ns	See Table 220, page 69
	T_{OSUD}	Setup time of the output data register	0.19	ns	See Table 220, page 69
O	T_{DP}	Propagation delay of SSTL2, Class I transmitter on the MSIO bank	2.055	ns	See Table 114, page 45
P	T_{DP}	Propagation delay of LVCMOS 1.5 V transmitter, drive strength of 12 mA, fast slew on the DDRIO bank	3.316	ns	See Table 70, page 34

Table 19 • Maximum Data Rate Summary Table for Voltage-Referenced I/O in Worst-Case Industrial Conditions

I/O	MSIO	MSIOD	DDRIO	Unit
LPDDR			400	Mbps
HSTL1.5 V			400	Mbps
SSTL 2.5 V	510	700	400	Mbps
SSTL 1.8 V			667	Mbps
SSTL 1.5 V			667	Mbps

Table 20 • Maximum Data Rate Summary Table for Differential I/O in Worst-Case Industrial Conditions

I/O	MSIO	MSIOD	Unit
LVPECL (input only)	900		Mbps
LVDS 3.3 V	535		Mbps
LVDS 2.5 V	535	700	Mbps
RSDS	520	700	Mbps
BLVDS	500		Mbps
MLVDS	500		Mbps
Mini-LVDS	520	700	Mbps

Table 21 • Maximum Frequency Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions

I/O	MSIO	MSIOD	DDRIO	Unit
PCI 3.3 V	315			MHz
LVTTTL 3.3 V	300			MHz
LVC MOS 3.3 V	300			MHz
LVC MOS 2.5 V	205	210	200	MHz
LVC MOS 1.8 V	147.5	200	200	MHz
LVC MOS 1.5 V	80	110	118	MHz
LVC MOS 1.2 V	60	80	100	MHz
LPDDR– LVC MOS 1.8 V mode			200	MHz

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of MSIO I/O bank at V_{OH}/V_{OL} Level.

Table 26 • I/O Weak Pull-Up/Pull-Down Resistances for MSIO I/O Bank

V_{DDI} Domain	R(WEAK PULL-UP) at V_{OH} (Ω)		R(WEAK PULL-DOWN) at V_{OL} (Ω)	
	Min	Max	Min	Max
3.3 V	9.9K	17.1K	9.98K	17.5K
2.5 V ^{1,2}	10K	17.6K	10.1K	18.4K
1.8 V ^{1,2}	10.4K	19.1K	10.4K	20.4K
1.5 V ^{1,2}	10.7K	20.4K	10.8K	22.2K
1.2 V ^{1,2}	11.3K	23.2K	11.5K	26.7K

1. $R(\text{WEAK PULL-DOWN}) = (V_{OL\text{spec}})/I(\text{WEAK PULL-DOWN MAX})$.
2. $R(\text{WEAK PULL-UP}) = (V_{DDI\text{max}} - V_{OH\text{spec}})/I(\text{WEAK PULL-UP MIN})$.

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of MSIOD I/O bank at V_{OH}/V_{OL} Level.

Table 27 • I/O Weak Pull-up/Pull-down Resistances for MSIOD I/O Bank

V_{DDI} Domain	R(WEAK PULL-UP) at V_{OH} (Ω)		R(WEAK PULL-DOWN) at V_{OL} (Ω)	
	Min	Max	Min	Max
2.5 V ^{1,2}	9.6K	16.6K	9.5K	16.4K
1.8 V ^{1,2}	9.7K	17.3K	9.7K	17.1K
1.5 V ^{1,2}	9.9K	18K	9.8K	17.6K
1.2 V ^{1,2}	10.3K	19.6K	10K	19.1K

1. $R(\text{WEAK PULL-DOWN}) = (V_{OL\text{spec}})/I(\text{WEAK PULL-DOWN MAX})$.
2. $R(\text{WEAK PULL-UP}) = (V_{DDI\text{max}} - V_{OH\text{spec}})/I(\text{WEAK PULL-UP MIN})$.

The following table lists the hysteresis voltage value for schmitt trigger mode input buffers.

Table 28 • Schmitt Trigger Input Hysteresis

Input Buffer Configuration	Hysteresis Value (Typical, unless otherwise noted)
3.3 V LVTTTL/LVCMOS/ PCI/PCI-X	$0.05 \times V_{DDI}$ (worst-case)
2.5 V LVCMOS	$0.05 \times V_{DDI}$ (worst-case)
1.8 V LVCMOS	$0.1 \times V_{DDI}$ (worst-case)
1.5 V LVCMOS	60 mV
1.2 V LVCMOS	20 mV

2.3.5.6 Single-Ended I/O Standards

2.3.5.6.1 Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)

LVCMOS is a widely used switching standard implemented in CMOS transistors. This standard is defined by JEDEC (JESD 8-5). The LVCMOS standards supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs are: LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33.

2.3.5.6.2 3.3 V LVCMOS/LVTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3 V applications.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 29 • LVTTL/LVCMOS 3.3 V DC Recommended DC Operating Conditions (Applicable to MSIO I/O Bank Only)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	3.15	3.3	3.45	V

Table 30 • LVTTL/LVCMOS 3.3 V Input Voltage Specification (Applicable to MSIO I/O Bank Only)

Parameter	Symbol	Min	Max	Unit
DC input logic high	V_{IH} (DC)	2.0	3.45	V
DC input logic low	V_{IL} (DC)	-0.3	0.8	V
Input current high ¹	I_{IH} (DC)			
Input current low ¹	I_{IL} (DC)			

1. See Table 24, page 22.

Table 31 • LVCMOS 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)

Parameter	Symbol	Min	Max	Unit
DC output logic high ¹	V_{OH}	$V_{DDI} - 0.4$		V
DC output logic low ¹	V_{OL}		0.4	V

1. The V_{OH}/V_{OL} test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.

Table 32 • LVTTL 3.3 V DC Output Voltage Specification (Applicable to MSIO I/O Bank Only)

Parameter	Symbol	Min	Max	Unit
DC output logic high	V_{OH}	2.4		V
DC output logic low	V_{OL}		0.4	V

Table 33 • LVTTL/LVCMOS 3.3 V AC Maximum Switching Speed (Applicable to MSIO I/O Bank Only)

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	D_{MAX}	600	Mbps	AC loading: 17 pF load, maximum drive/slew

Table 162 • LVDS DC Output Voltage Specification

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V_{OH}	1.25	1.425	1.6	V
DC output logic low	V_{OL}	0.9	1.075	1.25	V

Table 163 • LVDS DC Differential Voltage Specification

Parameter	Symbol	Min	Typ	Max	Unit
Differential output voltage swing	V_{OD}	250	350	450	mV
Output common mode voltage	V_{OCM}	1.125	1.25	1.375	V
Input common mode voltage	V_{ICM}	0.05	1.25	2.35	V
Input differential voltage	V_{ID}	100	350	600	mV

Table 164 • LVDS Minimum and Maximum AC Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	D_{MAX}	535	Mbps	AC loading: 12 pF / 100 Ω differential load
Maximum data rate (for MSIOD I/O bank) no pre-emphasis	D_{MAX}	620	Mbps	AC loading: 10 pF / 100 Ω differential load
		700	Mbps	AC loading: 2 pF / 100 Ω differential load

Table 165 • LVDS AC Impedance Specifications

Parameter	Symbol	Typ	Max	Unit
Termination resistance	R_T	100		Ω

Table 166 • LVDS AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	Cross point	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF

LVDS25 AC Switching Characteristics

 Worst commercial-case conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$
Table 167 • LVDS25 Receiver Characteristics for MSIO I/O Bank (Input Buffers)

On-Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.774	3.263	ns
100	2.775	3.264	ns

Table 168 • LVDS25 Receiver Characteristics for MSIOD I/O Bank (Input Buffers)

On-Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.554	3.004	ns
100	2.549	2.999	ns

Table 169 • LVDS25 Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2.136	2.513	2.416	2.842	2.402	2.825	2.423	2.85	2.409	2.833	ns

Table 170 • LVDS25 Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
No pre-emphasis	1.61	1.893	1.749	2.058	1.735	2.041	1.897	2.231	1.866	2.195	ns
Min pre-emphasis	1.527	1.796	1.757	2.067	1.744	2.052	1.905	2.241	1.876	2.207	ns
Med pre-emphasis	1.496	1.76	1.765	2.077	1.751	2.06	1.914	2.252	1.884	2.216	ns

LVDS33 AC Switching Characteristics
Table 171 • LVDS33 Receiver Characteristics for MSIO I/O Bank (Input Buffers)

On Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.572	3.025	ns
100	2.569	3.023	ns

Table 172 • LVDS33 Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
1.942	2.284	1.98	2.33	1.97	2.318	1.953	2.298	1.96	2.307	ns

Table 185 • M-LVDS DC Voltage Specification Output Voltage Specification (for MSIO I/O Bank Only)

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V_{OH}	1.25	1.425	1.6	V
DC output logic low	V_{OL}	0.9	1.075	1.25	V

Table 186 • M-LVDS Differential Voltage Specification

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing (for MSIO I/O bank only)	V_{OD}	300	650	mV
Output common mode voltage (for MSIO I/O bank only)	V_{OCM}	0.3	2.1	V
Input common mode voltage	V_{ICM}	0.3	1.2	V
Input differential voltage	V_{ID}	50	2400	mV

Table 187 • M-LVDS Minimum and Maximum AC Switching Speed for MSIO I/O Bank

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	D_{MAX}	500	Mbps	AC loading: 2 pF / 100 Ω differential load

Table 188 • M-LVDS AC Impedance Specifications

Parameter	Symbol	Typ	Unit
Termination resistance	R_T	50	Ω

Table 189 • M-LVDS AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	Cross point	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

Table 190 • M-LVDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)

On-Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.738	3.221	ns
100	2.735	3.218	ns

Table 191 • M-LVDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)

On-Die Termination (ODT)	T _{PY}		Unit
	-1	-Std	
None	2.495	2.934	ns
100	2.495	2.935	ns

Table 192 • M-LVDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)

T _{DP}		T _{ZL}		T _{ZH}		T _{HZ}		T _{LZ}		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2.258	2.656	2.348	2.762	2.334	2.746	2.123	2.497	2.125	2.5	ns

2.3.7.4 Mini-LVDS

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

Mini-LVDS Minimum and Maximum Input and Output Levels

Table 193 • Mini-LVDS Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{DDI}	2.375	2.5	2.625	V

Table 194 • Mini-LVDS DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC Input voltage	V _I	0	2.925	V

Table 195 • Mini-LVDS DC Output Voltage Specification

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V _{OH}	1.25	1.425	1.6	V
DC output logic low	V _{OL}	0.9	1.075	1.25	V

Table 196 • Mini-LVDS DC Differential Voltage Specification

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing	V _{OD}	300	600	mV
Output common mode voltage	V _{OCM}	1	1.4	V
Input common mode voltage	V _{ICM}	0.3	1.2	V
Input differential voltage	V _{ID}	100	600	mV

Table 197 • Mini-LVDS Minimum and Maximum AC Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	D _{MAX}	520	Mbps	AC loading: 2 pF / 100 Ω differential load
Maximum data rate (for MSIOD I/O bank)	D _{MAX}	700	Mbps	AC loading: 2 pF / 100 Ω differential load

The following table lists the input data register propagation delays in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

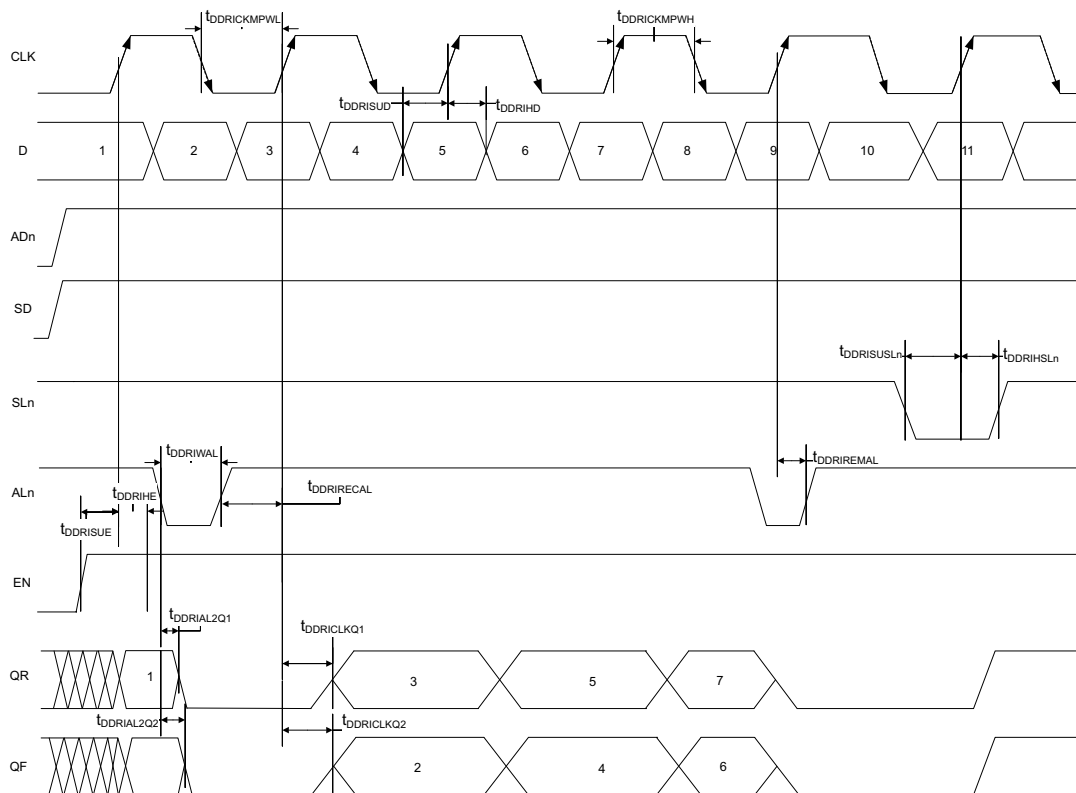
Table 219 • Input Data Register Propagation Delays

Parameter	Symbol	Measuring Nodes (from, to) ¹	-1		Unit
			-1	-Std	
Bypass delay of the input register	T_{IBYP}	F, G	0.353	0.415	ns
Clock-to-Q of the input register	T_{ICLKQ}	E, G	0.16	0.188	ns
Data setup time for the input register	T_{ISUD}	A, E	0.357	0.421	ns
Data hold time for the input register	T_{IHD}	A, E	0	0	ns
Enable setup time for the input register	T_{ISUE}	B, E	0.46	0.542	ns
Enable hold time for the input register	T_{IHE}	B, E	0	0	ns
Synchronous load setup time for the input register	T_{ISUSL}	D, E	0.46	0.542	ns
Synchronous load hold time for the input register	T_{IHSL}	D, E	0	0	ns
Asynchronous clear-to-Q of the input register (ADn=1)	T_{IALN2Q}	C, G	0.625	0.735	ns
Asynchronous preset-to-Q of the input register (ADn=0)		C, G	0.587	0.69	ns
Asynchronous load removal time for the input register	$T_{IREMALN}$	C, E	0	0	ns
Asynchronous load recovery time for the input register	$T_{IRECALN}$	C, E	0.074	0.087	ns
Asynchronous load minimum pulse width for the input register	T_{IWALN}	C, C	0.304	0.357	ns
Clock minimum pulse width high for the input register	$T_{ICKMPWH}$	E, E	0.075	0.088	ns
Clock minimum pulse width low for the input register	$T_{ICKMPWL}$	E, E	0.159	0.187	ns

1. For the derating values at specific junction temperature and voltage supply levels, see Table 16, page 14 for derating values.

2.3.9.2 Input DDR Timing Diagram

Figure 11 • Input DDR Timing Diagram



2.3.9.3 Timing Characteristics

The following table lists the input DDR propagation delays in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 221 • Input DDR Propagation Delays

Symbol	Description	Measuring Nodes (from, to)	-1	-Std	Unit
$T_{DDRICKQ1}$	Clock-to-Out Out_QR for input DDR	B, C	0.16	0.188	ns
$T_{DDRICKQ2}$	Clock-to-Out Out_QF for input DDR	B, D	0.166	0.195	ns
$T_{DDRISUD}$	Data setup for input DDR	A, B	0.357	0.421	ns
T_{DDRHD}	Data hold for input DDR	A, B	0	0	ns
$T_{DDRISUE}$	Enable setup for input DDR	E, B	0.46	0.542	ns
T_{DDRHE}	Enable hold for input DDR	E, B	0	0	ns
$T_{DDRISUSL}$	Synchronous load setup for input DDR	G, B	0.46	0.542	ns
T_{DDRISL}	Synchronous load hold for input DDR	G, B	0	0	ns
$T_{DDRIRIAL2Q1}$	Asynchronous load-to-out QR for input DDR	F, C	0.587	0.69	ns
$T_{DDRIRIAL2Q2}$	Asynchronous load-to-out QF for input DDR	F, D	0.541	0.636	ns
$T_{DDRIREMAL}$	Asynchronous load removal time for input DDR	F, B	0	0	ns
$T_{DDRIRECAL}$	Asynchronous load recovery time for input DDR	F, B	0.074	0.087	ns

2.3.10.2 Timing Characteristics

The following table lists the combinatorial cell propagation delays in worst commercial-case conditions when $T_J = 85\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 223 • Combinatorial Cell Propagation Delays

Combinatorial Cell	Equation	Symbol	-1	-Std	Unit
INV	$Y = !A$	T_{PD}	0.1	0.118	ns
AND2	$Y = A \cdot B$	T_{PD}	0.164	0.193	ns
NAND2	$Y = !(A \cdot B)$	T_{PD}	0.147	0.173	ns
OR2	$Y = A + B$	T_{PD}	0.164	0.193	ns
NOR2	$Y = !(A + B)$	T_{PD}	0.147	0.173	ns
XOR2	$Y = A \oplus B$	T_{PD}	0.164	0.193	ns
XOR3	$Y = A \oplus B \oplus C$	T_{PD}	0.225	0.265	ns
AND3	$Y = A \cdot B \cdot C$	T_{PD}	0.209	0.246	ns
AND4	$Y = A \cdot B \cdot C \cdot D$	T_{PD}	0.287	0.338	ns

2.3.10.3 Sequential Module

IGLOO2 and SmartFusion2 SoC FPGAs offer a separate flip-flop which can be used independently from the LUT. The flip-flop can be configured as a register or a latch and has a data input and optional enable, synchronous load (clear or preset), and asynchronous load (clear or preset).

Figure 15 • Sequential Module

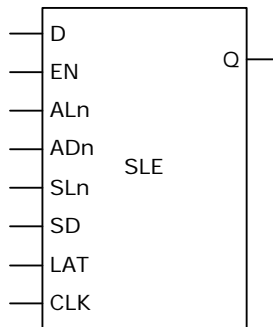


Table 233 • RAM1K18 – Dual-Port Mode for Depth x Width Configuration 4K x 4 (continued)

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register			0.323		0.38	ns
Read access time without pipeline register	T_{CLK2Q}		2.273		2.673	ns
Access time with feed-through write timing			1.511		1.778	ns
Address setup time	T_{ADDRSU}	0.543		0.638		ns
Address hold time	T_{ADDRHD}	0.274		0.322		ns
Data setup time	T_{DSU}	0.334		0.393		ns
Data hold time	T_{DHD}	0.082		0.096		ns
Block select setup time	T_{BLKSU}	0.207		0.244		ns
Block select hold time	T_{BLKHD}	0.216		0.254		ns
Block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		1.511		1.778	ns
Block select minimum pulse width	T_{BLKMPW}	0.186		0.219		ns
Read enable setup time	T_{RDESU}	0.516		0.607		ns
Read enable hold time	T_{RDEHD}	0.071		0.083		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLESU}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEHD}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	T_{R2Q}		1.507		1.773	ns
Asynchronous reset removal time	T_{RSTREM}	0.506		0.595		ns
Asynchronous reset recovery time	T_{RSTREC}	0.004		0.005		ns
Asynchronous reset minimum pulse width	T_{RSTMPW}	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTREM}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTREC}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	T_{SRSTSU}	0.226		0.265		ns
Synchronous reset hold time	T_{SRSTHD}	0.036		0.043		ns
Write enable setup time	T_{WESU}	0.458		0.539		ns
Write enable hold time	T_{WEHD}	0.048		0.057		ns
Maximum frequency	F_{MAX}		400		340	MHz

Table 240 • μ SRAM (RAM128x8) in 128 x 8 Mode (continued)

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read address hold time in synchronous mode	T_{ADDRHD}	0.091		0.107		ns
Read address hold time in asynchronous mode		-0.778		-0.915		ns
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	-0.65		-0.765		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.036		2.396	ns
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	-0.023		-0.027		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.835		0.982	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.115		0.135		ns
Write input data hold time	T_{DINCHD}	0.15		0.177		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	-0.026		-0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

The following table lists the programming times in worst-case conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$. External SPI flash part# AT25DF641-s3H is used during this measurement.

Table 256 • JTAG Programming (Fabric Only)

M2S/M2GL Device	Image size		Program	Verify	Unit
	Bytes				
005	302672		44	10	Sec
010	568784		50	18	Sec
025	1223504		73	26	Sec
050	2424832		88	54	Sec
060	2418896		99	54	Sec
090	3645968		135	126	Sec
150	6139184		177	193	Sec

Table 257 • JTAG Programming (eNVM Only)

M2S/M2GL Device	Image size		Program	Verify	Unit
	Bytes				
005	137536		61	4	Sec
010	274816		100	9	Sec
025	274816		100	9	Sec
050	2,78,528		106	8	Sec
060	268480		98	8	Sec
090	544496		176	15	Sec
150	544496		177	15	Sec

Table 258 • JTAG Programming (Fabric and eNVM)

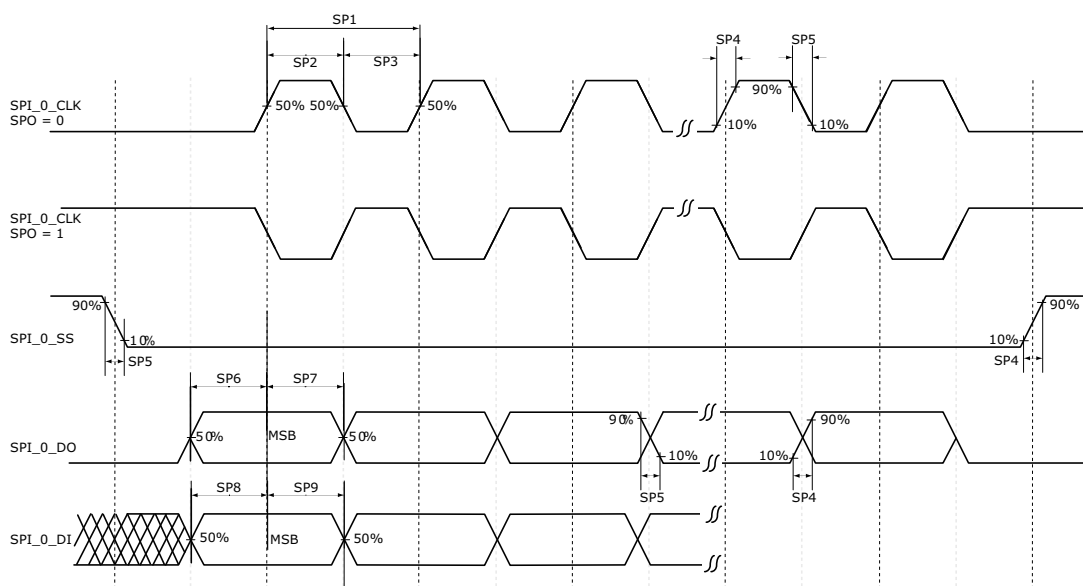
M2S/M2GL Device	Image size		Program	Verify	Unit
	Bytes				
005	439296		71	11	Sec
010	842688		129	20	Sec
025	1497408		142	35	Sec
050	2695168		184	59	Sec
060	2686464		180	70	Sec
090	4190208		288	147	Sec
150	6682768		338	231	Sec

Table 305 • SPI Characteristics for All Devices (continued)

Symbol	Description	Min	Typ	Max	Unit	Conditions
sp5	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS fall time (10%–90%) ¹		2.906		ns	IO Configuration: LVCMOS 2.5 V-8 mA AC Loading: 35 pF Test Conditions: Typical Voltage, 25 °C
SPI master configuration (applicable for 005, 010, 025, and 050 devices)						
sp6m	SPI_[0 1]_DO setup time ²	(SPI_x_CLK_period/2) – 8.0			ns	
sp7m	SPI_[0 1]_DO hold time ²	(SPI_x_CLK_period/2) – 2.5			ns	
sp8m	SPI_[0 1]_DI setup time ²	12			ns	
sp9m	SPI_[0 1]_DI hold time ²	2.5			ns	
SPI slave configuration (applicable for 005, 010, 025, and 050 devices)						
sp6s	SPI_[0 1]_DO setup time ²	(SPI_x_CLK_period/2) – 17.0			ns	
sp7s	SPI_[0 1]_DO hold time ²	(SPI_x_CLK_period/2) + 3.0			ns	
sp8s	SPI_[0 1]_DI setup time ²	2			ns	
sp9s	SPI_[0 1]_DI hold time ²	7			ns	
SPI master configuration (applicable for 060, 090, and 150 devices)						
sp6m	SPI_[0 1]_DO setup time ²	(SPI_x_CLK_period/2) – 7.0			ns	
sp7m	SPI_[0 1]_DO hold time ²	(SPI_x_CLK_period/2) – 9.5			ns	
sp8m	SPI_[0 1]_DI setup time ²	15			ns	
sp9m	SPI_[0 1]_DI hold time ²	–2.5			ns	
SPI slave configuration (applicable for 060, 090, and 150 devices)						
sp6s	SPI_[0 1]_DO setup time ²	(SPI_x_CLK_period/2) – 16.0			ns	
sp7s	SPI_[0 1]_DO hold time ²	(SPI_x_CLK_period/2) – 3.5			ns	
sp8s	SPI_[0 1]_DI setup time ²	3			ns	
sp9s	SPI_[0 1]_DI hold time ²	2.5			ns	

1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. For allowable pclk configurations, see Serial Peripheral Interface Controller section in the *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.

Figure 22 • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)



2.3.32 CAN Controller Characteristics

The following table lists the CAN controller characteristics in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 306 • CAN Controller Characteristics

Parameter	Description	-1	-Std	Unit
FCANREFCLK ¹	Internally sourced CAN reference clock frequency	160	136	MHz
BAUDCANMAX	Maximum CAN performance baud rate	1	1	Mbps
BAUDCANMIN	Minimum CAN performance baud rate	0.05	0.05	Mbps

1. PCLK to CAN controller must be a multiple of 8 MHz.

2.3.33 USB Characteristics

The following table lists the USB characteristics in worst-case industrial conditions when $T_J = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 307 • USB Characteristics

Parameter	Description	-1	-Std	Unit
FUSBREFCLK	Internally sourced USB reference clock frequency	166	142	MHz
TUSBCLK	USB clock period	16.66	16.66	ns
TUSBPD	Clock to USB data propagation delay	9.0	9.0	ns
TUSBSU	Setup time for USB data	6.0	6.0	ns
TUSBHD	Hold time for USB data	0	0	ns