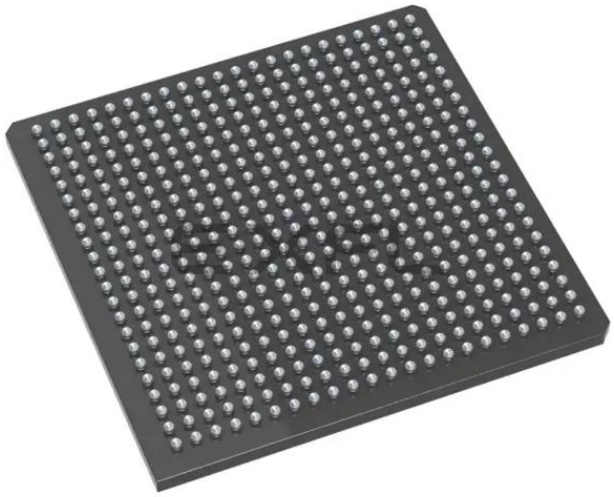

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 27696 |
| Total RAM Bits | 1130496 |
| Number of I/O | 267 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 484-BGA |
| Supplier Device Package | 484-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m2gl025-fg484i |

- Added Table 244, page 94 and Table 256, page 99 (SAR 73971).
- Updated the SerDes Electrical and Timing AC and DC Characteristics, page 121 (SAR 71171).
- Added the DEVRST_N Characteristics, page 116 (SAR 64100, 72103).
- Added Table 298, page 122 (SAR 71897).
- Updated Table 25, page 22, Table 26, page 23, and Table 27, page 23 (SAR 74570).
- Added 060 devices in Table 277, page 107, Table 278, page 108, and Table 279, page 108 (SAR 57898).
- Updated duty cycle parameter of crystal in Table 280, page 109 and Table 281, page 109 (SAR 57898).
- Added 32 KHz mode PLL acquisition time in Table 282, page 110 (SAR 68281).
- Updated Table 293, page 119 for 060 devices (SAR 57828).
- Updated Table 297, page 122 for CID value (SAR 70878).

## 1.4 Revision 8.0

The following is a summary of the changes in revision 8.0 of this document.

- Updated Table 11, page 12 (SAR 69218).
- Updated Table 12, page 13 (SAR 69218).
- Updated Table 283, page 111 (SAR 69000).

## 1.5 Revision 7.0

The following is a summary of the changes in revision 7.0 of this document.

- Updated Table 1, page 4(SAR 68620).

## 1.6 Revision 6.0

The following is a summary of the changes in revision 6.0 of this document.

- Updated Table 5, page 7 (SAR 65949).
- Updated Table 9, page 10 (SAR 62995).
- Updated Table 123, page 47 and Table 133, page 49 (SAR 67210).
- Added Embedded NVM (eNVM) Characteristics, page 104 (SAR 52509).
- Updated Table 277, page 107 (SAR 64855).
- Updated Table 282, page 110 (SAR 65958 and SAR 56666).
- Added DDR Memory Interface Characteristics, page 120 (SAR 66223).
- Added SFP Transceiver Characteristics, page 120 (SAR 63105).
- Updated Table 302, page 123 and Table 309, page 129 (SAR 66314).

## 1.7 Revision 5.0

The following is a summary of the changes in revision 5.0 of this document.

- Updated Table 1, page 4.
- Updated Table 4, page 6 for $T_J$ symbol information.
- Updated Table 5, page 7 (SAR 63109).
- Updated Table 9, page 10.
- Updated Table 282, page 110 (SAR 62012).
- Added Table 290, page 116 (SAR 64100).
- Added Table 306, page 128, Table 307, page 128 (SAR 50424).

## 1.8 Revision 4.0

The following is a summary of the changes in revision 4.0 of this document.

- Updated Table 1, page 4. Changed the Status of 090 devices to "Production" (SAR 62750).
- Updated Figure 10, page 70. Removed inverter bubble from DDR_IN latch (SAR 61418).
- Updated SerDes Electrical and Timing AC and DC Characteristics, page 121 (SAR 62836).

## 2.2 References

The following documents are recommended references:

- *PB0121: IGLOO2 Product Brief*
- *DS0124: IGLOO2 Pin Descriptions*
- *PB0115: SmartFusion2 SoC FPGA Product Brief*
- *DS0115: SmartFusion2 Pin Descriptions*

All product documentation for IGLOO2 and SmartFusion2 is available at:
http://www.microsemi.com/products/fpga-soc/fpga/igloo2-fpga
http://www.microsemi.com/products/fpga-soc/soc-fpga/smartfusion2#overview

## 2.3 Electrical Specifications

### 2.3.1 Operating Conditions

The following table lists the stress limits. Stress applied above the specified limit may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in the following table are not implied.

***Table 3 •*** **Absolute Maximum Ratings**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC core supply voltage. Must always power this pin. | $V_{DD}$ | –0.3 | 1.32 | V |
| Power supply for charge pumps (for normal operation and programming). Must always power this pin. | $V_{PP}$ | –0.3 | 3.63 | V |
| Analog power pad for MDDR PLL | MSS_MDDR_PLL_VDDA | –0.3 | 3.63 | V |
| Analog power pad for MDDR PLL | HPMS_MDDR_PLL_VDDA | –0.3 | 3.63 | V |
| Analog power pad for FDDR PLL | FDDR_PLL_VDDA | –0.3 | 3.63 | V |
| Analog power pad for MDDR PLL | PLL0_PLL1_MSS_MDDR_VDDA | –0.3 | 3.63 | V |
| Analog power pad for MDDR PLL | PLL0_PLL1_HPMS_MDDR_VDDA | –0.3 | 3.63 | V |
| Analog power pad for PLL0–5 | CCC_XX[01]_PLL_VDDA | –0.3 | 3.63 | V |
| High supply voltage for PLL SerDes[01] | SERDES_[01]_PLL_VDDA | –0.3 | 3.63 | V |
| Analog power for SerDes[01] PLL lane0 to lane3. This is a 2.5 V SerDes internal PLL supply. | SERDES_[01]_L[0123]_VDDAPLL | –0.3 | 2.75 | V |
| TX/RX analog I/O voltage. Low voltage power for the lanes of SerDesIF0. This is a 1.2 V SerDes PMA supply. | SERDES_[01]_L[0123]_VDDAIO | –0.3 | 1.32 | V |
| PCIe/PCS power supply | SERDES_[01]_VDD | –0.3 | 1.32 | V |
| DC FPGA I/O buffer supply voltage for MSIO I/O bank | $V_{DDIx}$ | –0.3 | 3.63 | V |
| DC FPGA I/O buffer supply voltage for MSIOD/DDRIO I/O banks | $V_{DDIx}$ | –0.3 | 2.75 | V |
| I/O Input voltage for MSIO I/O bank | $V_I$ | –0.3 | 3.63 | V |
| I/O Input voltage for MSIOD/DDRIO I/O bank | $V_I$ | –0.3 | 2.75 | V |
| Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to $V_{PP}$. | $V_{PPNVM}$ | –0.3 | 3.63 | V |
| Storage temperature[1] | $T_{STG}$ | –65 | 150 | °C |
| Junction temperature | $T_J$ | –55 | 135 | °C |

***Table 9 •*** **Package Thermal Resistance of SmartFusion2 and IGLOO2 Devices *(continued)***

| Device | Still Air $\theta_{JA}$ | 1.0 m/s $\theta_{JA}$ | 2.5 m/s $\theta_{JA}$ | $\theta_{JB}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|---|---|---|
| **150** | | | | | | |
| FC1152 | 9.08 | 6.81 | 5.87 | 2.56 | 0.38 | °C/W |
| FCS536 | 15.01 | 12.06 | 10.76 | 3.69 | 1.55 | °C/W |
| FCV484 | 16.21 | 13.11 | 11.84 | 6.73 | 0.10 | °C/W |

#### 2.3.1.2.1 Theta-JA

Junction-to-ambient thermal resistance ($\theta_{JA}$) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in the actual performance of the product. It must be used with caution, but it is useful for comparing the thermal performance of one package with another.

The maximum power dissipation allowed is calculated using EQ4.

$$\text{Maximum power allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

*EQ 4*

The absolute maximum junction temperature is 100 °C. EQ5 shows a sample calculation of the absolute maximum power dissipation allowed for the M2GL050T-FG896 package at commercial temperature and in still air, where:

$\theta_{JA}$ = 14.7 °C/W (taken from Table 9, page 10).

$T_A$ = 85 °C

$$\text{Maximum power allowed} = \frac{100\ °C - 85\ °C}{14.7\ °C/W} = 1.088\ W$$

*EQ 5*

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package.

If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink may be attached to the top of the case, or the airflow inside the system must be increased.

#### 2.3.1.2.2 Theta-JB

Junction-to-board thermal resistance ($\theta_{JB}$) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from the junction to the board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

#### 2.3.1.2.3 Theta-JC

Junction-to-case thermal resistance ($\theta_{JC}$) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable to packages used with external heat sinks. Constant temperature is applied to the surface, which acts as a boundary condition.

This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

### 2.3.1.3 ESD Performance

See *RT0001: Microsemi Corporation - SoC Products Reliability Report* for information about ESD.

### 2.3.5.5 Detailed I/O Characteristics

***Table 24 •*** **Input Capacitance, Leakage Current, and Ramp Time**

| Symbol | Description | Maximum | Unit | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | 10 | pF | |
| $I_{IL}$ (dc) | Input current low (Applicable to HSTL/SSTL inputs only) | 400 | µA | $V_{DDI}$ = 2.5 V |
| | | 500 | µA | $V_{DDI}$ = 1.8 V |
| | | 600 | µA | $V_{DDI}$ = 1.5 V[1] |
| | Input current low (Applicable to all other digital inputs) | 10 | µA | |
| $I_{IH}$ (dc) | Input current high (Applicable to HSTL/SSTL inputs only) | 400 | µA | $V_{DDI}$ = 2.5 V |
| | | 500 | µA | $V_{DDI}$ = 1.8 V |
| | | 600 | µA | $V_{DDI}$ = 1.5 V[1] |
| | Input current high (Applicable to all other digital inputs) | 10 | µA | |
| $T_{RAMPIN}$[2] | Input ramp time (Applicable to all digital inputs) | 50 | ns | |

1. Applicable when I/O pair is programmed with an HSTL/SSTL I/O type on IOP and an un-terminated I/O type (LVCMOS, for example) on ION pad.
2. Voltage ramp must be monotonic.

The following table lists the minimum and maximum I/O weak pull-up/pull-down resistance values of DDRIO I/O bank at $V_{OH}$/$V_{OL}$ Level.

***Table 25 •*** **I/O Weak Pull-up/Pull-down Resistances for DDRIO I/O Bank**

| | R(WEAK PULL-UP) at $V_{OH}$ (Ω) | | R(WEAK PULL-DOWN) at $V_{OL}$ (Ω) | |
|---|---|---|---|---|
| **$V_{DDI}$ Domain** | **Min** | **Max** | **Min** | **Max** |
| 2.5 V[1, 2] | 10K | 17.8K | 9.98K | 18K |
| 1.8 V[1, 2] | 10.3K | 19.1K | 10.3K | 19.5K |
| 1.5 V[1, 2] | 10.6K | 20.2K | 10.6K | 21.1K |
| 1.2 V[1, 2] | 11.1K | 22.7K | 11.2K | 24.6K |

1. R(WEAK PULL-DOWN) = (VOLspec)/I(WEAK PULL-DOWN MAX).
2. R(WEAK PULL-UP) = (VDDImax – VOHspec)/I(WEAK PULL-UP MIN).

***Table 46 •*** **LVCMOS 2.5 V Transmitter Characteristics for DDRIO Bank (Output and Tristate Buffers) *(continued)***

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | |
| 4 mA | Slow | 3.095 | 3.641 | 2.705 | 3.182 | 3.088 | 3.633 | 4.738 | 5.575 | 4.348 | 5.116 | ns |
| | Medium | 2.825 | 3.324 | 2.488 | 2.927 | 2.823 | 3.321 | 4.492 | 5.285 | 4.063 | 4.781 | ns |
| | Medium fast | 2.701 | 3.178 | 2.384 | 2.804 | 2.698 | 3.173 | 4.364 | 5.135 | 3.945 | 4.642 | ns |
| | Fast | 2.69 | 3.165 | 2.377 | 2.796 | 2.687 | 3.161 | 4.359 | 5.129 | 3.94 | 4.636 | ns |
| 6 mA | Slow | 2.919 | 3.434 | 2.491 | 2.93 | 2.902 | 3.414 | 5.085 | 5.983 | 4.674 | 5.5 | ns |
| | Medium | 2.65 | 3.118 | 2.279 | 2.681 | 2.642 | 3.108 | 4.845 | 5.701 | 4.375 | 5.148 | ns |
| | Medium fast | 2.529 | 2.975 | 2.176 | 2.56 | 2.521 | 2.965 | 4.724 | 5.558 | 4.259 | 5.011 | ns |
| | Fast | 2.516 | 2.96 | 2.168 | 2.551 | 2.508 | 2.95 | 4.717 | 5.55 | 4.251 | 5.002 | ns |
| 8 mA | Slow | 2.863 | 3.368 | 2.427 | 2.855 | 2.844 | 3.346 | 5.196 | 6.114 | 4.769 | 5.612 | ns |
| | Medium | 2.599 | 3.058 | 2.217 | 2.608 | 2.59 | 3.047 | 4.952 | 5.827 | 4.471 | 5.261 | ns |
| | Medium fast | 2.483 | 2.921 | 2.114 | 2.487 | 2.473 | 2.91 | 4.832 | 5.685 | 4.364 | 5.134 | ns |
| | Fast | 2.467 | 2.902 | 2.106 | 2.478 | 2.457 | 2.89 | 4.826 | 5.678 | 4.348 | 5.116 | ns |
| 12 mA | Slow | 2.747 | 3.232 | 2.296 | 2.701 | 2.724 | 3.204 | 5.39 | 6.342 | 4.938 | 5.81 | ns |
| | Medium | 2.493 | 2.934 | 2.102 | 2.473 | 2.483 | 2.921 | 5.166 | 6.078 | 4.65 | 5.471 | ns |
| | Medium fast | 2.382 | 2.803 | 2.006 | 2.36 | 2.371 | 2.789 | 5.067 | 5.962 | 4.546 | 5.349 | ns |
| | Fast | 2.369 | 2.787 | 1.999 | 2.352 | 2.357 | 2.773 | 5.063 | 5.958 | 4.538 | 5.339 | ns |
| 16 mA | Slow | 2.677 | 3.149 | 2.213 | 2.604 | 2.649 | 3.116 | 5.575 | 6.56 | 5.08 | 5.977 | ns |
| | Medium | 2.432 | 2.862 | 2.028 | 2.386 | 2.421 | 2.848 | 5.372 | 6.32 | 4.801 | 5.649 | ns |
| | Medium fast | 2.324 | 2.734 | 1.937 | 2.278 | 2.311 | 2.718 | 5.297 | 6.233 | 4.7 | 5.531 | ns |
| | Fast | 2.313 | 2.721 | 1.929 | 2.269 | 2.3 | 2.706 | 5.296 | 6.231 | 4.699 | 5.529 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

***Table 47 •*** **LVCMOS 2.5 V Transmitter Characteristics for MSIO Bank (Output and Tristate Buffers)**

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | |
| 2 mA | Slow | 3.48 | 4.095 | 3.855 | 4.534 | 3.785 | 4.453 | 2.12 | 2.494 | 3.45 | 4.059 | ns |
| 4 mA | Slow | 2.583 | 3.039 | 3.042 | 3.579 | 3.138 | 3.691 | 4.143 | 4.874 | 4.687 | 5.513 | ns |
| 6 mA | Slow | 2.392 | 2.815 | 2.669 | 3.139 | 2.82 | 3.317 | 4.909 | 5.775 | 5.083 | 5.98 | ns |
| 8 mA | Slow | 2.309 | 2.717 | 2.565 | 3.017 | 2.74 | 3.223 | 5.812 | 6.837 | 5.523 | 6.497 | ns |
| 12 mA | Slow | 2.333 | 2.745 | 2.437 | 2.867 | 2.626 | 3.089 | 6.131 | 7.213 | 5.712 | 6.72 | ns |
| 16 mA | Slow | 2.412 | 2.838 | 2.335 | 2.747 | 2.533 | 2.979 | 6.54 | 7.694 | 6.007 | 7.067 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

***Table 48 •*** **LVCMOS 2.5 V Transmitter Characteristics for MSIOD Bank (Output and Tristate Buffers)**

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | Unit |
| 2 mA | Slow | 2.206 | 2.596 | 2.678 | 3.15 | 2.64 | 3.106 | 4.935 | 5.805 | 4.74 | 5.576 | ns |
| 4 mA | Slow | 1.835 | 2.159 | 2.242 | 2.637 | 2.256 | 2.654 | 5.413 | 6.368 | 5.15 | 6.059 | ns |
| 6 mA | Slow | 1.709 | 2.01 | 2.132 | 2.508 | 2.167 | 2.549 | 5.813 | 6.838 | 5.499 | 6.469 | ns |
| 8 mA | Slow | 1.63 | 1.918 | 1.958 | 2.303 | 2.012 | 2.367 | 6.226 | 7.324 | 5.816 | 6.842 | ns |
| 12 mA | Slow | 1.648 | 1.939 | 1.86 | 2.187 | 1.921 | 2.259 | 6.519 | 7.669 | 6.027 | 7.09 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

### *2.3.5.8 1.8 V LVCMOS*

LVCMOS 1.8 is a general standard for 1.8 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-7A.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

***Table 49 •*** **LVCMOS 1.8 V DC Recommended Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **LVCMOS 1.8 V DC Recommended Operating Conditions** | | | | | |
| Supply voltage | $V_{DDI}$ | 1.710 | 1.8 | 1.89 | V |

***Table 50 •*** **LVCMOS 1.8 V DC Input Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high (for MSIOD and DDRIO I/O banks) | $V_{IH}$ (DC) | 0.65 × $V_{DDI}$ | 1.89 | V |
| DC input logic high (for MSIO I/O bank) | $V_{IH}$ (DC) | 0.65 × $V_{DDI}$ | 3.45 | V |
| DC input logic low | $V_{IL}$ (DC) | –0.3 | 0.35 × $V_{DDI}$ | V |
| Input current high[1] | $I_{IH}$ (DC) | | | – |
| Input current low[1] | $I_{IL}$ (DC) | | | – |

1. See Table 24, page 22.

***Table 51 •*** **LVCMOS 1.8 V DC Output Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC output logic high | $V_{OH}$ | $V_{DDI}$ – 0.45 | | V |
| DC output logic low | $V_{OL}$ | | 0.45 | V |

***Table 52 •*** **LVCMOS 1.8 V Minimum and Maximum AC Switching Speed**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for DDRIO I/O bank)[1] | $D_{MAX}$ | 400 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 295 | Mbps | AC loading: 17 pF load, maximum drive/slew |
| Maximum data rate (for MSIOD I/O bank)[1] | $D_{MAX}$ | 400 | Mbps | AC loading: 17 pF load, maximum drive/slew |

1. Maximum Data Rate applies for Drive Strength 8 mA and above, All Slews.

***Table 57 •*** **LVCMOS 1.8 V Transmitter Characteristics for DDRIO I/O Bank with Fixed Code (Output and Tristate Buffers)**

| Output Drive Selection | Slew Control | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$[1] | | $T_{LZ}$[1] | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | –1 | –Std | |
| 2 mA | Slow | 4.234 | 4.981 | 3.646 | 4.29 | 4.245 | 4.995 | 4.908 | 5.774 | 4.434 | 5.216 | ns |
| | Medium | 3.824 | 4.498 | 3.282 | 3.861 | 3.834 | 4.511 | 4.625 | 5.441 | 4.116 | 4.843 | ns |
| | Medium fast | 3.627 | 4.267 | 3.111 | 3.66 | 3.637 | 4.279 | 4.481 | 5.272 | 3.984 | 4.687 | ns |
| | Fast | 3.605 | 4.241 | 3.097 | 3.644 | 3.615 | 4.253 | 4.472 | 5.262 | 3.973 | 4.674 | ns |
| 4 mA | Slow | 3.923 | 4.615 | 3.314 | 3.9 | 3.918 | 4.61 | 5.403 | 6.356 | 4.894 | 5.757 | ns |
| | Medium | 3.518 | 4.138 | 2.961 | 3.484 | 3.515 | 4.135 | 5.121 | 6.025 | 4.561 | 5.366 | ns |
| | Medium fast | 3.321 | 3.907 | 2.783 | 3.275 | 3.317 | 3.903 | 4.966 | 5.843 | 4.426 | 5.206 | ns |
| | Fast | 3.301 | 3.883 | 2.77 | 3.259 | 3.296 | 3.878 | 4.957 | 5.831 | 4.417 | 5.196 | ns |
| 6 mA | Slow | 3.71 | 4.364 | 3.104 | 3.652 | 3.702 | 4.355 | 5.62 | 6.612 | 5.08 | 5.977 | ns |
| | Medium | 3.333 | 3.921 | 2.779 | 3.27 | 3.325 | 3.913 | 5.346 | 6.289 | 4.777 | 5.62 | ns |
| | Medium fast | 3.155 | 3.712 | 2.62 | 3.083 | 3.146 | 3.702 | 5.21 | 6.13 | 4.657 | 5.479 | ns |
| | Fast | 3.134 | 3.688 | 2.608 | 3.068 | 3.125 | 3.677 | 5.202 | 6.12 | 4.648 | 5.468 | ns |
| 8 mA | Slow | 3.619 | 4.258 | 3.007 | 3.538 | 3.607 | 4.244 | 5.815 | 6.841 | 5.249 | 6.175 | ns |
| | Medium | 3.246 | 3.819 | 2.686 | 3.16 | 3.236 | 3.807 | 5.542 | 6.52 | 4.936 | 5.807 | ns |
| | Medium fast | 3.066 | 3.607 | 2.525 | 2.971 | 3.054 | 3.593 | 5.405 | 6.359 | 4.811 | 5.66 | ns |
| | Fast | 3.046 | 3.584 | 2.513 | 2.957 | 3.034 | 3.57 | 5.401 | 6.353 | 4.803 | 5.651 | ns |
| 10 mA | Slow | 3.498 | 4.115 | 2.878 | 3.386 | 3.481 | 4.096 | 6.046 | 7.113 | 5.444 | 6.404 | ns |
| | Medium | 3.138 | 3.692 | 2.569 | 3.023 | 3.126 | 3.678 | 5.782 | 6.803 | 5.129 | 6.034 | ns |
| | Medium fast | 2.966 | 3.489 | 2.414 | 2.841 | 2.951 | 3.472 | 5.666 | 6.665 | 5.013 | 5.897 | ns |
| | Fast | 2.945 | 3.464 | 2.401 | 2.826 | 2.93 | 3.448 | 5.659 | 6.658 | 5.003 | 5.886 | ns |
| 12 mA | Slow | 3.417 | 4.02 | 2.807 | 3.303 | 3.401 | 4.002 | 6.083 | 7.156 | 5.464 | 6.428 | ns |
| | Medium | 3.076 | 3.618 | 2.519 | 2.964 | 3.063 | 3.604 | 5.828 | 6.856 | 5.176 | 6.089 | ns |
| | Medium fast | 2.913 | 3.427 | 2.376 | 2.795 | 2.898 | 3.41 | 5.725 | 6.736 | 5.072 | 5.966 | ns |
| | Fast | 2.894 | 3.405 | 2.362 | 2.78 | 2.879 | 3.388 | 5.715 | 6.724 | 5.064 | 5.957 | ns |
| 16 mA | Slow | 3.366 | 3.96 | 2.751 | 3.237 | 3.348 | 3.939 | 6.226 | 7.324 | 5.576 | 6.56 | ns |
| | Medium | 3.03 | 3.565 | 2.47 | 2.906 | 3.017 | 3.55 | 5.981 | 7.036 | 5.282 | 6.214 | ns |
| | Medium fast | 2.87 | 3.377 | 2.328 | 2.739 | 2.854 | 3.358 | 5.895 | 6.935 | 5.18 | 6.094 | ns |
| | Fast | 2.853 | 3.357 | 2.314 | 2.723 | 2.837 | 3.338 | 5.889 | 6.929 | 5.177 | 6.09 | ns |

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

***Table 131 •*** **SSTL15 DC Output Voltage Specification (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| **DDR3/SSTL15 Class I (DDR3 Reduced Drive)** | | | | |
| DC output logic high | $V_{OH}$ | 0.8 × $V_{DDI}$ | | V |
| DC output logic low | $V_{OL}$ | | 0.2 × $V_{DDI}$ | V |
| Output minimum source DC current | $I_{OH}$ at $V_{OH}$ | 6.5 | | mA |
| Output minimum sink current | $I_{OL}$ at $V_{OL}$ | –6.5 | | mA |
| **DDR3/SSTL15 Class II (DDR3 Full Drive)** | | | | |
| DC output logic high | $V_{OH}$ | 0.8 × $V_{DDI}$ | | V |
| DC output logic low | $V_{OL}$ | | 0.2 × $V_{DDI}$ | V |
| Output minimum source DC current | $I_{OH}$ at $V_{OH}$ | 7.6 | | mA |
| Output minimum sink current | $I_{OL}$ at $V_{OL}$ | –7.6 | | mA |

***Table 132 •*** **SSTL15 DC Differential Voltage Specification (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Min | Unit |
|---|---|---|---|
| DC input differential voltage | $V_{ID}$ | 0.2 | V |

**Note:** To meet JEDEC electrical compliance, use DDR3 full drive transmitter.

***Table 133 •*** **SSTL15 AC SSTL15 Minimum and Maximum AC Switching Speed (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| AC input differential voltage | $V_{DIFF}$ (AC) | 0.3 | | V |
| AC differential cross point voltage | $V_x$ (AC) | 0.5 × $V_{DDI}$ – 0.150 | 0.5 × $V_{DDI}$ + 0.150 | V |

***Table 134 •*** **SSTL15 Minimum and Maximum AC Switching Speed (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate | $D_{MAX}$ | 667 | Mbps | AC loading: per JEDEC specifications |

***Table 135 •*** **SSTL15 AC Calibrated Impedance Option (for DDRIO I/O Bank Only)**

| Parameter | Symbol | Typ | Unit | Conditions |
|---|---|---|---|---|
| Supported output driver calibrated impedance | $R_{REF}$ | 34, 40 | Ω | Reference resistor = 240 Ω |
| Effective impedance value (ODT) | $R_{TT}$ | 20, 30, 40, 60, 120 | Ω | Reference resistor = 240 Ω |

### 2.3.6.6 Low Power Double Data Rate (LPDDR)

LPDDR reduced and full drive low power double data rate standards are supported in IGLOO2 FPGA and SmartFusion2 SoC FPGA I/Os. This standard requires a differential amplifier input buffer and a push-pull output buffer.

**Minimum and Maximum DC/AC Input and Output Levels Specification**

***Table 139 •*** **LPDDR DC Recommended DC Operating Conditions**

| Parameter | Symbol | Min | Typ | Max |
|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 1.71 | 1.8 | 1.89 |
| Termination voltage | $V_{TT}$ | 0.838 | 0.900 | 0.964 |
| Input reference voltage | $V_{REF}$ | 0.838 | 0.900 | 0.964 |

***Table 140 •*** **LPDDR DC Input Voltage Specification**

| Parameter | Symbol | Min | Max |
|---|---|---|---|
| DC input logic high | $V_{IH}$ (DC) | 0.7 × $V_{DDI}$ | 1.89 |
| DC input logic low | $V_{IL}$ (DC) | –0.3 | 0.3 × $V_{DDI}$ |
| Input current high[1] | $I_{IH}$ (DC) | | |
| Input current low[1] | $I_{IL}$ (DC) | | |

1. See Table 24, page 22.

***Table 141 •*** **LPDDR DC Output Voltage Specification Reduced Drive**

| Parameter | Symbol | Min | Max |
|---|---|---|---|
| DC output logic high | $V_{OH}$ | 0.9 × $V_{DDI}$ | |
| DC output logic low | $V_{OL}$ | | 0.1 × $V_{DDI}$ |
| Output minimum source DC current | $I_{OH}$ at $V_{OH}$ | 0.1 | |
| Output minimum sink current | $I_{OL}$ at $V_{OL}$ | –0.1 | |

***Table 142 •*** **LPDDR DC Output Voltage Specification Full Drive[1]**

| Parameter | Symbol | Min | Max |
|---|---|---|---|
| DC output logic high | $V_{OH}$ | 0.9 × $V_{DDI}$ | |
| DC output logic low | $V_{OL}$ | | 0.1 × $V_{DDI}$ |
| Output minimum source DC current | $I_{OH}$ at $V_{OH}$ | 0.1 | |
| Output minimum sink current | $I_{OL}$ at $V_{OL}$ | –0.1 | |

1. To meet JEDEC Electrical Compliance, use LPDDR Full Drive Transmitter.

***Table 143 •*** **LPDDR DC Differential Voltage Specification**

| Parameter | Symbol | Min |
|---|---|---|
| DC input differential voltage | $V_{ID}$ (DC) | 0.4 × $V_{DDI}$ |

**Table 168 • LVDS25 Receiver Characteristics for MSIOD I/O Bank (Input Buffers)**

| | $T_{PY}$ | | |
|---|---|---|---|
| **On-Die Termination (ODT)** | **–1** | **–Std** | **Unit** |
| None | 2.554 | 3.004 | ns |
| 100 | 2.549 | 2.999 | ns |

**Table 169 • LVDS25 Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

| $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| 2.136 | 2.513 | 2.416 | 2.842 | 2.402 | 2.825 | 2.423 | 2.85 | 2.409 | 2.833 | ns |

**Table 170 • LVDS25 Transmitter Characteristics for MSIOD I/O Bank (Output and Tristate Buffers)**

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| No pre-emphasis | 1.61 | 1.893 | 1.749 | 2.058 | 1.735 | 2.041 | 1.897 | 2.231 | 1.866 | 2.195 | ns |
| Min pre-emphasis | 1.527 | 1.796 | 1.757 | 2.067 | 1.744 | 2.052 | 1.905 | 2.241 | 1.876 | 2.207 | ns |
| Med pre-emphasis | 1.496 | 1.76 | 1.765 | 2.077 | 1.751 | 2.06 | 1.914 | 2.252 | 1.884 | 2.216 | ns |

### LVDS33 AC Switching Characteristics

**Table 171 • LVDS33 Receiver Characteristics for MSIO I/O Bank (Input Buffers)**

| | $T_{PY}$ | | |
|---|---|---|---|
| **On Die Termination (ODT)** | **–1** | **–Std** | **Unit** |
| None | 2.572 | 3.025 | ns |
| 100 | 2.569 | 3.023 | ns |

**Table 172 • LVDS33 Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**

| $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| 1.942 | 2.284 | 1.98 | 2.33 | 1.97 | 2.318 | 1.953 | 2.298 | 1.96 | 2.307 | ns |

**Table 215 • LVPECL DC Input Voltage Specification**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input voltage | $V_I$ | 0 | 3.45 | V |

**Table 216 • LVPECL DC Differential Voltage Specification**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input common mode voltage | $V_{ICM}$ | 0.3 | | 2.8 | V |
| Input differential voltage | $V_{IDIFF}$ | 100 | 300 | 1,000 | mV |

**Table 217 • LVPECL Minimum and Maximum AC Switching Speeds**

| Parameter | Symbol | Max | Unit |
|---|---|---|---|
| Maximum data rate | $D_{MAX}$ | 900 | Mbps |

**AC Switching Characteristics**

Worst commercial-case conditions: $T_J$ = 85 °C, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 2.375 V.

**Table 218 • LVPECL Receiver Characteristics for MSIO I/O Bank**

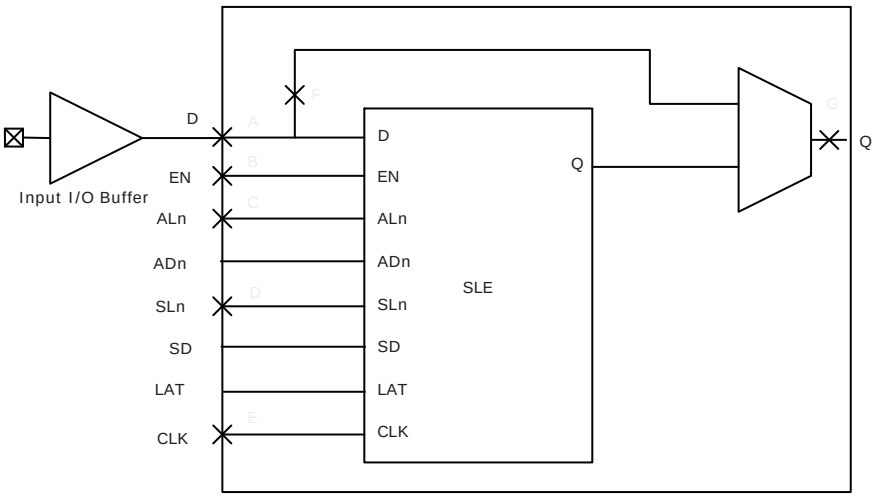
| | $T_{PY}$ | | |
|---|---|---|---|
| On-Die Termination (ODT) | –1 | –Std | Unit |
| None | 2.572 | 3.025 | ns |
| 100 | 2.569 | 3.023 | ns |

## 2.3.8 I/O Register Specifications

This section describes input and output register specifications.

### 2.3.8.1 Input Register

**Figure 6 • Timing Model for Input Register**



### 2.3.9.4 Output DDR Module

**Figure 12 • Output DDR Module**

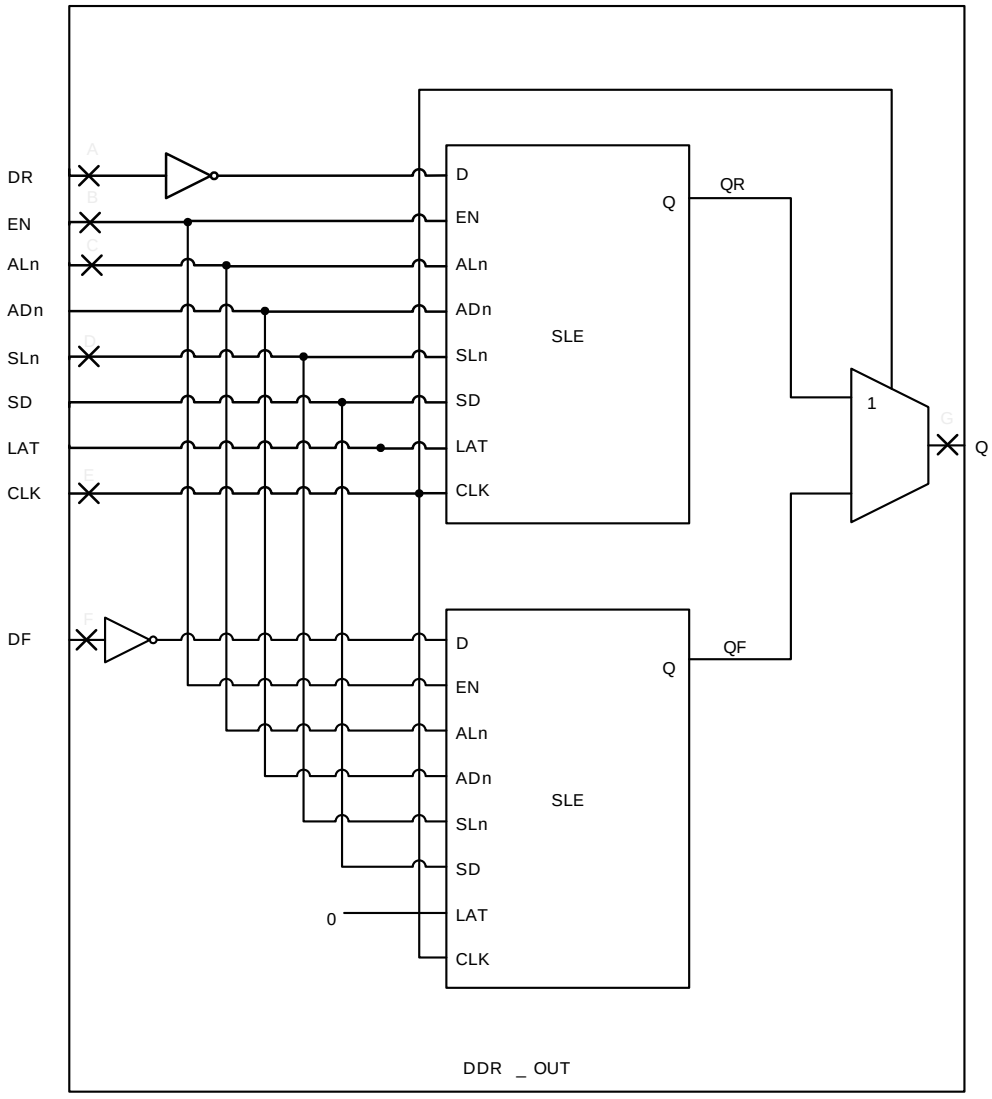
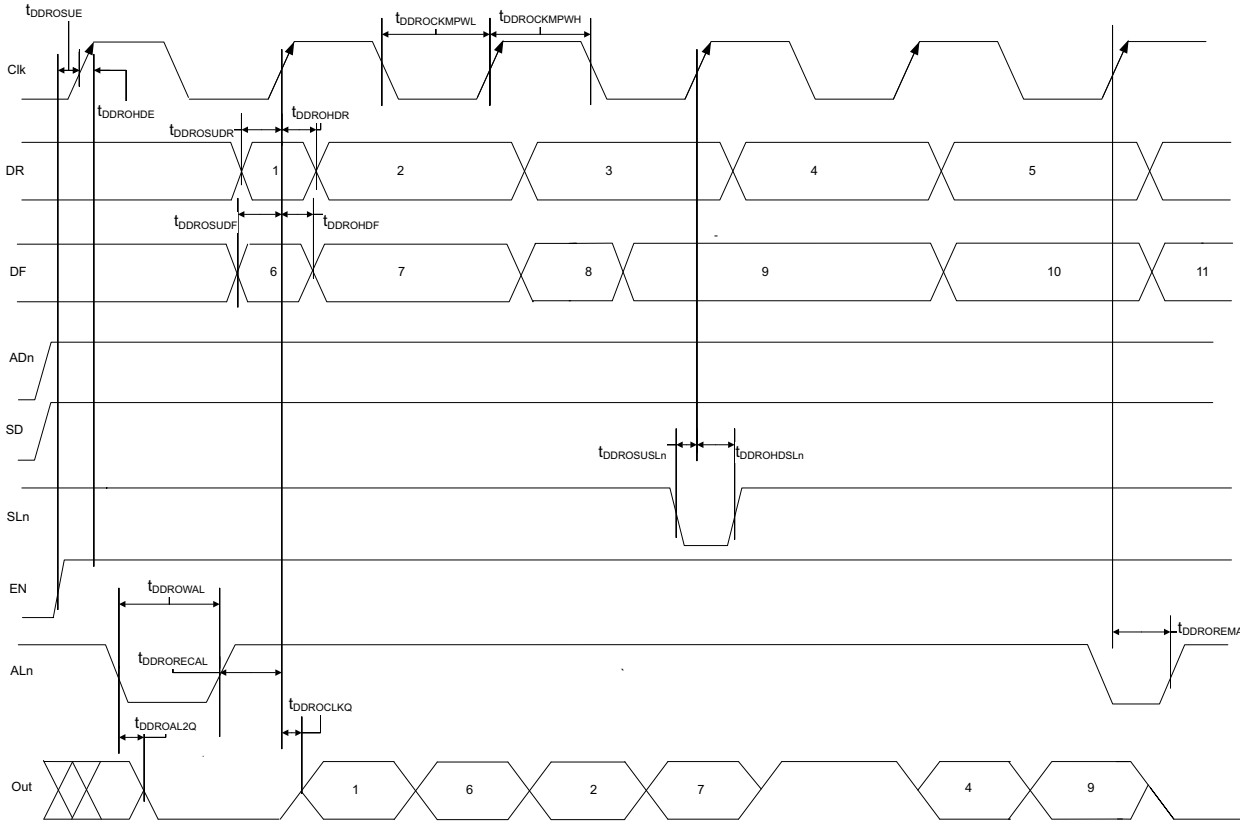


***Figure 13 •*** **Output DDR Timing Diagram**




### *2.3.9.5 Timing Characteristics*

The following table lists the output DDR propagation delays in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 222 •*** **Output DDR Propagation Delays**

| Symbol | Description | Measuring Nodes (from, to) | –1 | –Std | Unit |
|---|---|---|---|---|---|
| $T_{DDROCLKQ}$ | Clock-to-out of DDR for output DDR | E, G | 0.263 | 0.309 | ns |
| $T_{DDROSUDF}$ | Data_F data setup for output DDR | F, E | 0.143 | 0.168 | ns |
| $T_{DDROSUDR}$ | Data_R data setup for output DDR | A, E | 0.19 | 0.223 | ns |
| $T_{DDROHDF}$ | Data_F data hold for output DDR | F, E | 0 | 0 | ns |
| $T_{DDROHDR}$ | Data_R data hold for output DDR | A, E | 0 | 0 | ns |
| $T_{DDROSUE}$ | Enable setup for input DDR | B, E | 0.419 | 0.493 | ns |
| $T_{DDROHE}$ | Enable hold for input DDR | B, E | 0 | 0 | ns |
| $T_{DDROSUSLN}$ | Synchronous load setup for input DDR | D, E | 0.196 | 0.231 | ns |
| $T_{DDROHSLN}$ | Synchronous load hold for input DDR | D, E | 0 | 0 | ns |
| $T_{DDROAL2Q}$ | Asynchronous load-to-out for output DDR | C, G | 0.528 | 0.621 | ns |
| $T_{DDROREMAL}$ | Asynchronous load removal time for output DDR | C, E | 0 | 0 | ns |
| $T_{DDRORECAL}$ | Asynchronous load recovery time for output DDR | C, E | 0.034 | 0.04 | ns |

***Table 233 •*** **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4K × 4 *(continued)***

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Pipelined clock minimum pulse width low | $T_{PLCLKMPWL}$ | 1.125 | | 1.323 | | ns |
| Read access time with pipeline register | $T_{CLK2Q}$ | | 0.323 | | 0.38 | ns |
| Read access time without pipeline register | | | 2.273 | | 2.673 | ns |
| Access time with feed-through write timing | | | 1.511 | | 1.778 | ns |
| Address setup time | $T_{ADDRSU}$ | 0.543 | | 0.638 | | ns |
| Address hold time | $T_{ADDRHD}$ | 0.274 | | 0.322 | | ns |
| Data setup time | $T_{DSU}$ | 0.334 | | 0.393 | | ns |
| Data hold time | $T_{DHD}$ | 0.082 | | 0.096 | | ns |
| Block select setup time | $T_{BLKSU}$ | 0.207 | | 0.244 | | ns |
| Block select hold time | $T_{BLKHD}$ | 0.216 | | 0.254 | | ns |
| Block select to out disable time (when pipelined register is disabled) | $T_{BLK2Q}$ | | 1.511 | | 1.778 | ns |
| Block select minimum pulse width | $T_{BLKMPW}$ | 0.186 | | 0.219 | | ns |
| Read enable setup time | $T_{RDESU}$ | 0.516 | | 0.607 | | ns |
| Read enable hold time | $T_{RDEHD}$ | 0.071 | | 0.083 | | ns |
| Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLESU}$ | 0.248 | | 0.291 | | ns |
| Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN) | $T_{RDPLEHD}$ | 0.102 | | 0.12 | | ns |
| Asynchronous reset to output propagation delay | $T_{R2Q}$ | | 1.507 | | 1.773 | ns |
| Asynchronous reset removal time | $T_{RSTREM}$ | 0.506 | | 0.595 | | ns |
| Asynchronous reset recovery time | $T_{RSTREC}$ | 0.004 | | 0.005 | | ns |
| Asynchronous reset minimum pulse width | $T_{RSTMPW}$ | 0.301 | | 0.354 | | ns |
| Pipelined register asynchronous reset removal time | $T_{PLRSTREM}$ | –0.279 | | –0.328 | | ns |
| Pipelined register asynchronous reset recovery time | $T_{PLRSTREC}$ | 0.327 | | 0.385 | | ns |
| Pipelined register asynchronous reset minimum pulse width | $T_{PLRSTMPW}$ | 0.282 | | 0.332 | | ns |
| Synchronous reset setup time | $T_{SRSTSU}$ | 0.226 | | 0.265 | | ns |
| Synchronous reset hold time | $T_{SRSTHD}$ | 0.036 | | 0.043 | | ns |
| Write enable setup time | $T_{WESU}$ | 0.458 | | 0.539 | | ns |
| Write enable hold time | $T_{WEHD}$ | 0.048 | | 0.057 | | ns |
| Maximum frequency | $F_{MAX}$ | | 400 | | 340 | MHz |

The following table lists the math blocks with input register used and output in bypass mode in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 270 •*** **Math Block with Input Register Used and Output in Bypass Mode**

| | | –1 | | –Std | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| Input register setup time | $T_{MISU}$ | 0.149 | | 0.176 | | ns |
| Input register hold time | $T_{MIHD}$ | 0.185 | | 0.218 | | ns |
| Synchronous reset/enable setup time | $T_{MSRSTENSU}$ | 0.08 | | 0.094 | | ns |
| Synchronous reset/enable hold time | $T_{MSRSTENHD}$ | –0.012 | | –0.014 | | ns |
| Asynchronous reset removal time | $T_{MARSTREM}$ | –0.005 | | –0.005 | | ns |
| Asynchronous reset recovery time | $T_{MARSTREC}$ | 0.088 | | 0.104 | | ns |
| Input register clock to output delay | $T_{MICQ}$ | | 2.52 | | 2.964 | ns |
| CDIN to output delay | $T_{MCDIN2Q}$ | | 1.951 | | 2.295 | ns |

The following table lists the math blocks with input and output in bypass mode in worst commercial-case conditions when $T_J$ = 85 °C, $V_{DD}$ = 1.14 V.

***Table 271 •*** **Math Block with Input and Output in Bypass Mode**

| | | –1 | –Std | |
|---|---|---|---|---|
| **Parameter** | **Symbol** | **Max** | **Max** | **Unit** |
| Input to output delay | $T_{MIQ}$ | 2.568 | 3.022 | ns |
| CDIN to output delay | $T_{MCDIN2Q}$ | 1.951 | 2.295 | ns |

## 2.3.15 Embedded NVM (eNVM) Characteristics

The following table lists the eNVM read performance in worst-case conditions when $V_{DD}$ = 1.14 V, $V_{PPNVM}$ = $V_{PP}$ = 2.375 V.

***Table 272 •*** **eNVM Read Performance**

| | | Operating Temperature Range | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Description** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| $T_J$ | Junction temperature range | –55 °C to 125 °C | | –40 °C to 100 °C | | 0 °C to 85 °C | | °C |
| $F_{MAXREAD}$ | eNVM maximum read frequency | 25 | 25 | 25 | 25 | 25 | 25 | MHz |

The following table lists the eNVM page programming in worst-case conditions when $V_{DD}$ = 1.14 V, $V_{PPNVM}$ = $V_{PP}$ = 2.375 V.

***Table 273 •*** **eNVM Page Programming**

| | | Operating Temperature Range | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Description** | **–1** | **–Std** | **–1** | **–Std** | **–1** | **–Std** | **Unit** |
| $T_J$ | Junction temperature range | –55 °C to 125 °C | | –40 °C to 100 °C | | 0 °C to 85 °C | | °C |
| $T_{PAGEPGM}$ | eNVM page programming time | 40 | 40 | 40 | 40 | 40 | 40 | ms |

***Table 291 •*** **DEVRST_N to Functional Times for SmartFusion2 *(continued)***

| | | | | Maximum Power-up to Functional Time for SmartFusion2 (uS) | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **From** | **To** | **Description** | **005** | **010** | **025** | **050** | **060** | **090** | **150** |
| $T_{DEVRST2POR}$ | DEVRST_N | POWER_ON_RESET_N | $V_{DD}$ at its minimum threshold level to fabric | 233 | 289 | 216 | 213 | 237 | 234 | 219 |
| $T_{DEVRST2MSSRST}$ | DEVRST_N | MSS_RESET_N_M2F | $V_{DD}$ at its minimum threshold level to MSS | 702 | 765 | 712 | 688 | 636 | 630 | 866 |
| $T_{DEVRST2WPU}$ | DEVRST_N | DDRIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |
| | DEVRST_N | MSIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |
| | DEVRST_N | MSIOD Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |

***Figure 19 •*** **DEVRST_N to Functional Timing Diagram for SmartFusion2**

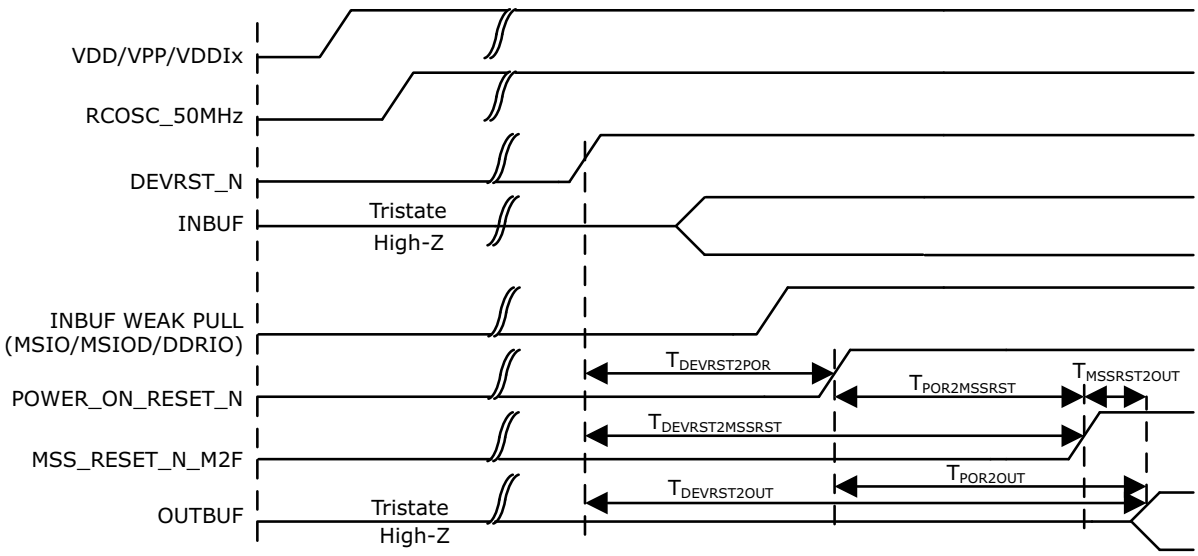


***Table 293 •*** **Flash*Freeze Entry and Exit Times *(continued)***

| | | Entry/Exit Timing FCLK = 100MHz | | Entry/Exit Timing FCLK = 3 MHz | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **005, 010, 025, 060, 090, and 150** | **050** | **All Devices** | **Unit** | **Conditions** |
| Exit time with respect to the fabric PLL lock[1] | TFF_EXIT | 1.5 | 1.5 | 1.5 | ms | eNVM and MSS/HPMS PLL = ON during F*F |
| | | 1.5 | 1.5 | 1.5 | ms | eNVM and MSS/HPMS PLL = OFF during F*F and both are turned back on at exit |
| Exit time with respect to the fabric buffer output | TFF_EXIT | 21 | 15 | 21 | µs | eNVM and MSS/HPMS PLL = ON during F*F |
| | | 65 | 55 | 65 | µs | eNVM and MSS/HPMS PLL = OFF during F*F and both are turned back on at exit |

1. PLL Lock Delay set to 1024 cycles (default).

## 2.3.28 DDR Memory Interface Characteristics

The following table lists the DDR memory interface characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 294 •*** **DDR Memory Interface Characteristics**

| | Supported Data Rate | | |
|---|---|---|---|
| **Standard** | **Min** | **Max** | **Unit** |
| DDR3 | 667 | 667 | Mbps |
| DDR2 | 667 | 667 | Mbps |
| LPDDR | 50 | 400 | Mbps |

## 2.3.29 SFP Transceiver Characteristics

IGLOO2 and SmartFusion2 SerDes complies with small form-factor pluggable (SFP) requirements as specified in SFP INF-80741. The following table provides the electrical characteristics.

The following table lists the SFP transceiver electrical characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 295 •*** **SFP Transceiver Electrical Characteristics**

| | | Differential Peak-Peak Voltage | | |
|---|---|---|---|---|
| **Pin** | **Direction** | **Min** | **Max** | **Unit** |
| RD+/-[1] | Output | 1600 | 2400 | mV |
| TD+/-[2] | Input | 350 | 2400 | mV |

1. Based on default SerDes transmitter settings for PCIe Gen1. Lower amplitudes are available through programming changes to TX_AMP setting.
2. Based on Input Voltage Common-Mode (VICM) = 0 V. Requires AC Coupling.

The following table lists the receiver pa in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V.

***Table 297 •*** **Receiver Parameters**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VRX-IN-PP-CC | Differential input peak-to-peak sensitivity (2.5 Gbps) | 0.238 | | 1.2 | V |
| | Differential input peak-to-peak sensitivity (2.5 Gbps, de-emphasized) | 0.219 | | 1.2 | V |
| | Differential input peak-to-peak sensitivity (5.0 Gbps) | 0.300 | | 1.2 | V |
| | Differential input peak-to-peak sensitivity (5.0 Gbps, de-emphasized) | 0.300 | | 1.2 | V |
| VRX-CM-AC-P | Input common mode range (AC coupled) | | | 150 | mV |
| ZRX-DIFF-DC | Differential input termination | 80 | 100 | 120 | Ω |
| REXT | External calibration resistor | 1,188 | 1,200 | 1,212 | Ω |
| CDR-LOCK-RST | CDR relock time from reset | | | 15 | µs |
| RLRX-DIFF | Return loss differential mode (2.5 Gbps) | –10 | | | dB |
| | Return loss differential mode (5.0 Gbps) | | | | |
| | 0.05 GHz to 1.25 GHz | –10 | | | dB |
| | 1.25 GHz to 2.5 GHz | –8 | | | dB |
| RLRX-CM | Return loss common mode (2.5 Gbps, 5.0 Gbps) | –6 | | | dB |
| RX-CID[1] | CID limit PCIe Gen1/2 | | | 200 | UI |
| VRX-IDLE-DET-DIFF-PP | Signal detect limit | 65 | | 175 | mV |

1. AC-coupled, BER = $e^{-12}$, using synchronous clock.

***Table 298 •*** **SerDes Protocol Compliance**

| Protocol | Maximum Data Rate (Gbps) | –1 | –Std |
|---|---|---|---|
| PCIe Gen 1 | 2.5 | Yes | Yes |
| PCIe Gen 2 | 5.0 | Yes | |
| XAUI | 3.125 | Yes | |
| Generic EPCS | 3.2 | Yes | |
| Generic EPCS | 2.5 | Yes | Yes |

***Table 303 •*** **I2C Characteristics *(continued)***

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Maximum data rate | $D_{MAX}$ | | | 400 | Kbps | Fast mode |
| | | | | 100 | Kbps | Standard mode |
| Pulse width of spikes which must be suppressed by the input filter | $T_{FILT}$ | | 50 | | ns | Fast mode |

1. These values are provided for MSIO Bank–LVTTL 8 mA Low Drive at 25 °C, typical conditions. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.
2. These maximum values are provided for information only. Minimum output buffer resistance values depend on $V_{DDIx}$, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.
3. R(PULL-DOWN-MAX) = (VOLspec)/IOLspec.
4. R(PULL-UP-MAX) = (VDDImax–VOHspec)/IOHspec.

The following table lists the $I^2C$ switching characteristics in worst-case industrial conditions when $T_J$ = 100 °C, $V_{DD}$ = 1.14 V

***Table 304 •*** **I2C Switching Characteristics**

| | | –1 | Std | |
|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Min** | **Unit** |
| Low period of I2C_x_SCL | $T_{LOW}$ | 1 | 1 | PCLK cycles |
| High period of I2C_x_SCL | $T_{HIGH}$ | 1 | 1 | PCLK cycles |
| START hold time | $T_{HD;STA}$ | 1 | 1 | PCLK cycles |
| START setup time | $T_{SU;STA}$ | 1 | 1 | PCLK cycles |
| DATA hold time | $T_{HD;DAT}$ | 1 | 1 | PCLK cycles |
| DATA setup time | $T_{SU;DAT}$ | 1 | 1 | PCLK cycles |
| STOP setup time | $T_{SU;STO}$ | 1 | 1 | PCLK cycles |

***Figure 21 •*** **$I^2C$ Timing Parameter Definition**

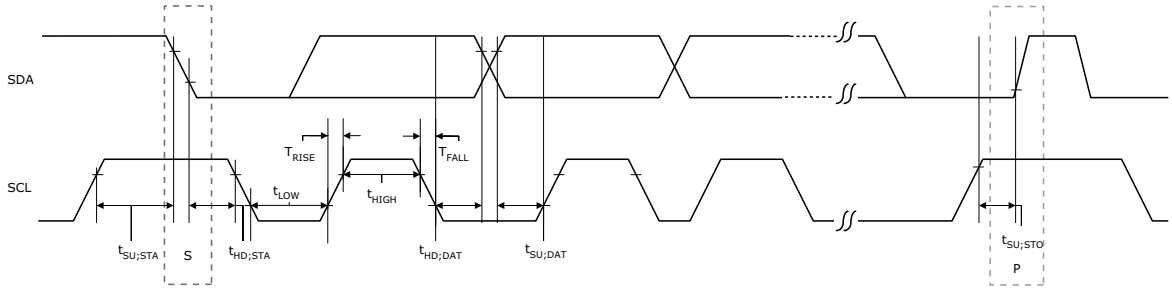


***Table 310 •*** **SPI Characteristics for All Devices *(continued)***

| Symbol | Description | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| SPI master configuration (applicable for 060, 090, and 150 devices) | | | | | | |
| sp6m | SPI_[0\|1]_DO setup time[2] | (SPI_x_CLK_period/2) – 7.0 | | | ns | |
| sp7m | SPI_[0\|1]_DO hold time[2] | (SPI_x_CLK_period/2) – 9.5 | | | ns | |
| sp8m | SPI_[0\|1]_DI setup time[2] | 15 | | | ns | |
| sp9m | SPI_[0\|1]_DI hold time[2] | –2.5 | | | ns | |
| SPI slave configuration (applicable for 060, 090, and 150 devices) | | | | | | |
| sp6s | SPI_[0\|1]_DO setup time[2] | (SPI_x_CLK_period/2) – 16.0 | | | ns | |
| sp7s | SPI_[0\|1]_DO hold time[2] | (SPI_x_CLK_period/2) - 3.5 | | | ns | |
| sp8s | SPI_[0\|1]_DI setup time[2] | 3 | | | ns | |
| sp9s | SPI_[0\|1]_DI hold time[2] | 2.5 | | | ns | |

1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.
2. For allowable pclk configurations, see the Serial Peripheral Interface Controller section in the *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.

***Figure 23 •*** **SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)**