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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 27696 |
| Total RAM Bits | 1130496 |
| Number of I/O | 180 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 325-TFBGA, FCBGA |
| Supplier Device Package | 325-FCBGA (11x11) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m2gl025ts-1fcs325i |

***Table 136 •*** SSTL15 AC Test Parameter Specifications (for DDRIO I/O Bank Only)

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | 0.75 | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |
| Reference resistance for data test path for SSTL15 Class I ($T_{DP}$) | RTT_TEST | 50 | Ω |
| Reference resistance for data test path for SSTL15 Class II ($T_{DP}$) | RTT_TEST | 25 | Ω |
| Capacitive loading for data path ($T_{DP}$) | $C_{LOAD}$ | 5 | pF |

AC Switching Characteristics

Worst commercial-case conditions: $T_J$ = 85 ºC, $V_{DD}$ = 1.14 V, $V_{DDI}$ = 1.425 V

***Table 137 •*** DDR3/SSTL15 Receiver Characteristics for DDRIO I/O Bank with Calibration Only

| | | $T_{PY}$ | | |
|---|---|---|---|---|
| | On-Die Termination (ODT) | 1 | Std | Unit |
| Pseudo differential | None | 1.605 | 1.888 | ns |
| | 20 | 1.616 | 1.901 | ns |
| | 30 | 1.613 | 1.897 | ns |
| | 40 | 1.611 | 1.895 | ns |
| | 60 | 1.609 | 1.893 | ns |
| | 120 | 1.607 | 1.89 | ns |
| True differential | None | 1.623 | 1.91 | ns |
| | 20 | 1.637 | 1.926 | ns |
| | 30 | 1.63 | 1.918 | ns |
| | 40 | 1.626 | 1.914 | ns |
| | 60 | 1.622 | 1.91 | ns |
| | 120 | 1.619 | 1.905 | ns |

***Table 138 •*** DDR3/SSTL15 Transmitter Characteristics (Output and Tristate Buffers)

| | $T_{DP}$ | | $T_{ZL}$ | | $T_{ZH}$ | | $T_{HZ}$ | | $T_{LZ}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | Std | 1 | Std | 1 | Std | 1 | Std | 1 | Std | Unit |
| DDR3 Reduced Drive/SSTL15 Class I (for DDRIO I/O Bank) | | | | | | | | | | | |
| Single-ended | 2.533 | 2.98 | 2.522 | 2.967 | 2.523 | 2.968 | 2.427 | 2.855 | 2.428 | 2.856 | ns |
| Differential | 2.555 | 3.005 | 3.073 | 3.615 | 3.073 | 3.615 | 2.416 | 2.843 | 2.416 | 2.843 | ns |
| DDR3 Full Drive/SSTL15 Class II (for DDRIO I/O Bank) | | | | | | | | | | | |
| Single-ended | 2.53 | 2.977 | 2.514 | 2.958 | 2.516 | 2.96 | 2.422 | 2.849 | 2.425 | 2.852 | ns |
| Differential | 2.552 | 3.002 | 2.591 | 3.048 | 2.59 | 3.047 | 2.882 | 3.391 | 2.881 | 3.39 | ns |

### 2.3.7.5 RSDS

Reduced Swing Differential Signaling (RSDS) is similar to an LVDS high-speed interface using differential signaling. RSDS has a similar implementation to LVDS devices and is only intended for point-to-point applications.

Minimum and Maximum Input and Output Levels

**Table 203 •** RSDS Recommended DC Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDI}$ | 2.375 | 2.5 | 2.625 | V |

**Table 204 •** RSDS DC Input Voltage Specification

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input voltage | $V_I$ | 0 | 2.925 | V |

**Table 205 •** RSDS DC Output Voltage Specification

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DC output logic high | $V_{OH}$ | 1.25 | 1.425 | 1.6 | V |
| DC output logic low | $V_{OL}$ | 0.9 | 1.075 | 1.25 | V |

**Table 206 •** RSDS Differential Voltage Specification

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Differential output voltage swing | $V_{OD}$ | 100 | 600 | mV |
| Output common mode voltage | $V_{OCM}$ | 0.5 | 1.5 | V |
| Input common mode voltage | $V_{ICM}$ | 0.3 | 1.5 | V |
| Input differential voltage | $V_{ID}$ | 100 | 600 | mV |

**Table 207 •** RSDS Minimum and Maximum AC Switching Speed

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Maximum data rate (for MSIO I/O bank) | $D_{MAX}$ | 520 | Mbps | AC loading: 2 pF / 100 Ω differential load |
| Maximum data rate (for MSIOD I/O bank) | $D_{MAX}$ | 700 | Mbps | AC loading: 2 pF / 100 Ω differential load |

**Table 208 •** RSDS AC Impedance Specifications

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Termination resistance | RT | 100 | Ω |

**Table 209 •** RSDS AC Test Parameter Specifications

| Parameter | Symbol | Typ | Unit |
|---|---|---|---|
| Measuring/trip point for data path | $V_{TRIP}$ | Cross point | V |
| Resistance for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $R_{ENT}$ | 2K | Ω |
| Capacitive loading for enable path ($T_{ZH}$, $T_{ZL}$, $T_{HZ}$, $T_{LZ}$) | $C_{ENT}$ | 5 | pF |

## 2.3.9 DDR Module Specification

This section describes input and output DDR module and timing specifications.

### 2.3.9.1 Input DDR Module

***Figure 10 •*** Input DDR Module

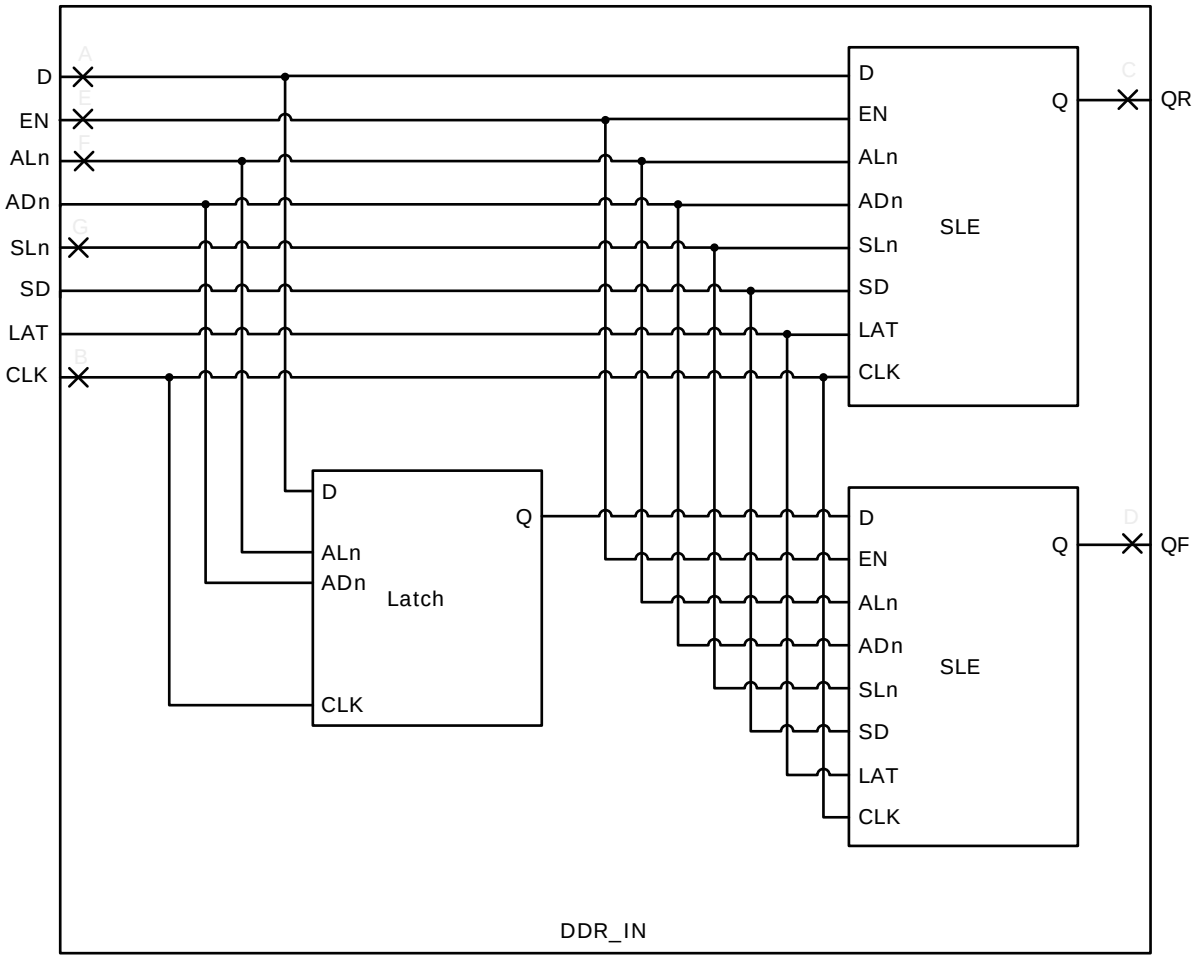
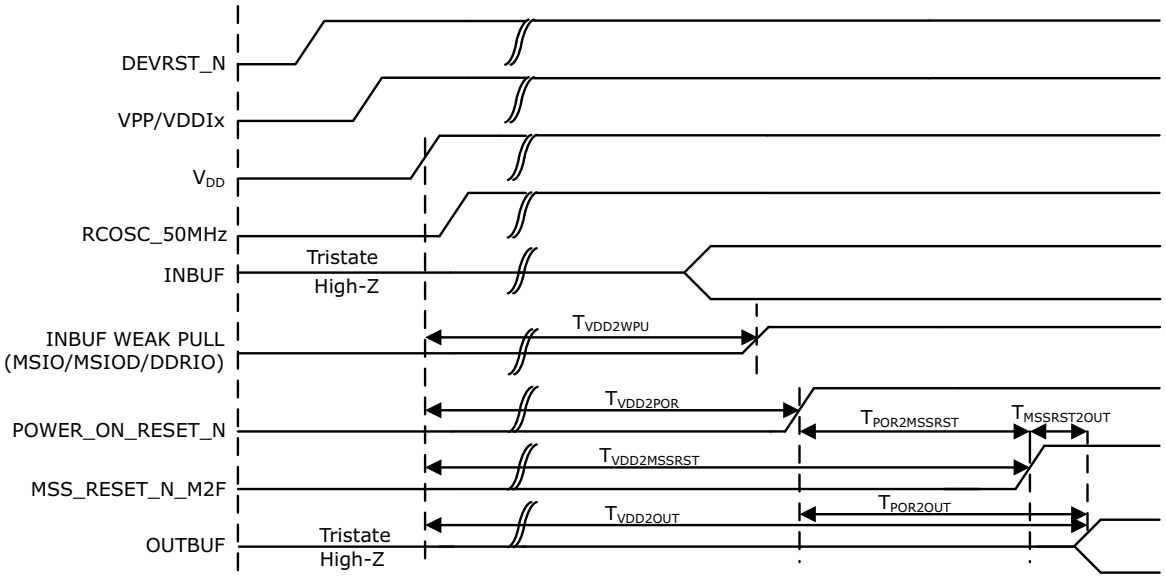


***Figure 17 •*** Power-up to Functional Timing Diagram for SmartFusion2




The following table lists the IGLOO2 power-up to functional times in worst-case industrial conditions when $T_J$ = 100 ℃, $V_{DD}$ = 1.14 V.

***Table 289 •*** Power-up to Functional Times for IGLOO2

| | | | | Maximum Power-up to Functional Time for IGLOO2 (uS) | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Symbol | From | To | Description | 005 | 010 | 025 | 050 | 060 | 090 | 150 |
| $T_{POR2OUT}$ | POWER_ON_RESET_N | Output available at I/O | Fabric to output | 114 | 114 | 114 | 113 | 114 | 114 | 114 |
| $T_{VDD2OUT}$ | $V_{DD}$ | Output available at I/O | $V_{DD}$ at its minimum threshold level to output | 2587 | 2600 | 2607 | 2558 | 2591 | 2600 | 2699 |
| $T_{VDD2POR}$ | $V_{DD}$ | POWER_ON_RESET_N | $V_{DD}$ at its minimum threshold level to fabric | 2474 | 2486 | 2493 | 2445 | 2477 | 2486 | 2585 |
| $T_{VDD2WPU}$ | DEVRST_N | DDRIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 2500 | 2487 | 2509 | 2475 | 2507 | 2519 | 2617 |
| | DEVRST_N | MSIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 2504 | 2491 | 2510 | 2478 | 2517 | 2525 | 2620 |
| | DEVRST_N | MSIOD Inbuf weak pull | DEVRST_N to Inbuf weak pull | 2479 | 2468 | 2493 | 2458 | 2486 | 2499 | 2595 |

Note: For more information about power-up times, see *UG0448: IGLOO2 FPGA High Performance Memory Subsystem User Guide*.

***Table 291 •*** DEVRST_N to Functional Times for SmartFusion2 ***(continued)***

| | | | | Maximum Power-up to Functional Time for SmartFusion2 (uS) | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Symbol | From | To | Description | 005 | 010 | 025 | 050 | 060 | 090 | 150 |
| $T_{DEVRST2POR}$ | DEVRST_N | POWER_ON_RESET_N | $V_{DD}$ at its minimum threshold level to fabric | 233 | 289 | 216 | 213 | 237 | 234 | 219 |
| $T_{DEVRST2MSSRST}$ | DEVRST_N | MSS_RESET_N_M2F | $V_{DD}$ at its minimum threshold level to MSS | 702 | 765 | 712 | 688 | 636 | 630 | 866 |
| $T_{DEVRST2WPU}$ | DEVRST_N | DDRIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |
| | DEVRST_N | MSIO Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |
| | DEVRST_N | MSIOD Inbuf weak pull | DEVRST_N to Inbuf weak pull | 208 | 202 | 197 | 193 | 216 | 215 | 215 |

***Figure 19 •*** DEVRST_N to Functional Timing Diagram for SmartFusion2